

FSB50450US

Motion SPM® 5 FRFET® Series

April 2013

Features

- 500 V R_{DS(on)}= 2.4 Ω (Max) FRFET MOSFET 3-Phase Inverter Including HVICs
- Three Separate Negative DC-Link Terminals for Inverter Current Sensing Applications
- · HVIC for Gate Driving and Undervoltage Protection
- Active-High Interface, Can Work With 3.3 V / 5 V Logic
- · Optimized for Low Electromagnetic Interference
- · Isolation Voltage Rating of 1500 Vrms for 1 min.
- · Surface Mounted Device Package
- · Moisture Sensitive Level (MSL) 3

Applications

 3-Phase Inverter Driver for Small Power AC Motor Drives

General Description

FSB50450US is an Advanced Motion SPM5 Series Based on Fast-Recovery MOSFET(FRFET) Technology as a Compact Inverter Solution for Small Power Motor Drive Applications Such as Fans and Pumps. It is Composed of Six FRFET MOSFETs and Three Half-Bridge Gate Drive HVICs. FSB50450US Provides Low Electromagnetic Interference(EMI) Characteristics with Optimizing Switching Speed. Moreover, Since It Employs MOSFETs as Power Switches, It has Greater Ruggedness and a Larger Safe Operating Area(SOA) than IGBT-Based Power Modules. The Pakage is Optimized for Thermal Performance and Compactness for use in Applications Where Space is Limited. FSB50450US is the Right Solution for Inverters Requiring Energy Efficiency, Compactness, and Low Electromanetic Interference.

Related Source

- · AN9042: Motion SPM5 Series Ver.1 User's Guide
- AN-9082 : Motion SPM5 Series Thermal Performance by Contact Pressure



Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSB50450US	FSB50450US	SPM5H-023	330 mm	TAPE & REEL	450

Absolute Maximum Ratings

Inverter Part (Each MOSFET® Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
V _{PN}	DC Link Input Voltage, Drain-Source Voltage of Each MOSFET		500	V
*I _{D 25}	Each MOSFET Drain Current, Continuous	T _C = 25°C	1.5	Α
*I _{D 80}	Each MOSFET Drain Current, Continuous	T _C = 80°C	1.1	Α
*I _{DP}	Each MOSFET Drain Current, Peak	T _C = 25°C, PW < 100 μs	3.8	Α
*I _{DRMS}	Each MOSFET Drain Current, Rms	T _C = 80°C, F _{PWM} < 20 KHz	0.8	A _{rms}
*P _D	Maximum Power Dissipation	T _C = 25°C, For Each MOSFET	14	W

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions	Rating	Unit
V _{CC}	Control Supply Voltage	Applied Between V _{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied Between V _B and V _S	20	V
V _{IN}	Input Signal Voltage	Applied Between IN and COM	-0.3 ~ V _{CC} +0.3	V

Thermal Resistance

Symbol	Parameter Conditions		Rating	Unit
$R_{ heta JC}$	Junction to Case Thermal Resistance	Each MOSFET under Inverter Operating Condition (Note 1)	8.9	°C/W

Total System

Symbol	Parameter	Conditions	Rating	Unit
T_J	Operating Junction Temperature		-40 ~ 150	°C
T _{STG}	Storage Temperature		-50 ~ 150	°C
V _{ISO}	Isolation Voltage	60 Hz, Sinusoidal, 1 minute, Connection Pins to Heatsink	1500	V_{rms}

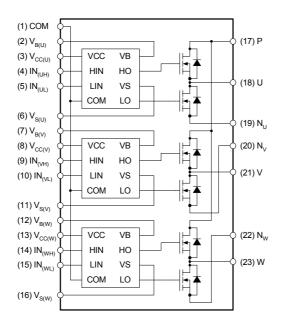
Note

^{1.} For the Measurement Point of Case Temperature $T_{\mathbb{C}}$, Please refer to Figure 4.

^{2.} Marking " * " Is Calculation Value or Design Factor.

Pin descriptions

Pin Number	Pin Name	Pin Description	
1	СОМ	IC Common Supply Ground	
2	V _{B(U)}	Bias Voltage for U Phase High Side MOSFET® Driving	
3	V _{CC(U)}	Bias Voltage for U Phase IC and Low Side MOSFET Driving	
4	IN _(UH)	Signal Input for U Phase High-Side	
5	IN _(UL)	Signal Input for U Phase Low-Side	
6	V _{S(U)}	Bias Voltage Ground for U Phase High Side MOSFET Driving	
7	V _{B(V)}	Bias Voltage for V Phase High Side MOSFET Driving	
8	V _{CC(V)}	Bias Voltage for V Phase IC and Low Side MOSFET Driving	
9	IN _(VH)	Signal Input for V Phase High-Side	
10	IN _(VL)	Signal Input for V Phase Low-Side	
11	V _{S(V)}	Bias Voltage Ground for V Phase High Side MOSFET Driving	
12	V _{B(W)}	Bias Voltage for W Phase High Side MOSFET Driving	
13	V _{CC(W)}	Bias Voltage for W Phase IC and Low Side MOSFET Driving	
14	IN _(WH)	Signal Input for W Phase High-Side	
15	IN _(WL)	Signal Input for W Phase Low-Side	
16	V _{S(W)}	Bias Voltage Ground for W Phase High Side MOSFET Driving	
17	Р	Positive DC-Link Input	
18	U	Output for U Phase	
19	N _U	Negative DC-Link Input for U Phase	
20	N _V	Negative DC-Link Input for V Phase	
21	V	Output for V Phase	
22	N _W	Negative DC-Link Input for W Phase	
23	W	Output for W Phase	



Note:

Source Terminal of Each Low-Side MOSFET is Not Connected to Supply Ground or Bias Voltage Ground Inside Motion SPM®. External Connections Should be Made as Indicated in Figure 3

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Electrical Characteristics ($T_J = 25$ °C, $V_{CC} = V_{BS} = 15$ V Unless Otherwise Specified)

Inverter Part (Each MOSFET® Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{IN} = 0V, I _D = 1 mA (Note 1)		-	-	V
$\Delta BV_{DSS}/$ ΔT_{J}	Breakdown Voltage Temperature Coefficient	I _D = 250μA, Referenced to 25°C	-	0.53	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0V, V _{DS} = 500 V		-	250	μΑ
R _{DS(on)}	Static Drain-Source On-Resistance	V _{CC} = V _{BS} = 15 V, V _{IN} = 5 V, I _D = 0.5 A		1.9	2.4	Ω
V _{SD}	Drain-Source Diode Forward Voltage	V _{CC} = V _{BS} = 15V, V _{IN} = 0V, I _D = -0.5 A		-	1.2	V
t _{ON}			-	1250	-	ns
t _{OFF}		V_{PN} = 300 V, V_{CC} = V_{BS} = 15 V, I_{D} = 1.0 A V_{IN} = 0 V \leftrightarrow 5 V, Inductive Load L= 3 mH High- and Low-Side MOSFET Switching	-	500	-	ns
t _{rr}	Switching Times		-	200	-	ns
E _{ON}		(Note 2)	-	80	-	μJ
E _{OFF}				10	-	μJ
RBSOA Reverse-Bias Safe Oper-		V_{PN} = 400 V, V_{CC} = V_{BS} = 15 V, I_{D} = I_{DP} , V_{DS} =BV _{DSS} , T_{J} = 150°C High- and Low-Side MOSFET Switching (Note 3)	DSS, Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

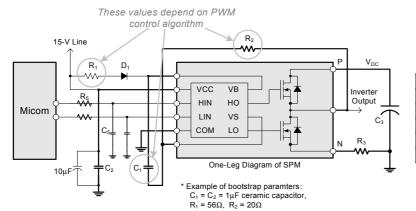
Symbol	Parameter		Conditions	Min	Тур	Max	Unit
I _{QCC}	Quiescent V _{CC} Current	V _{CC} =15 V, V _{IN} =0V	Applied Between V _{CC} and COM	-	-	160	μΑ
I _{QBS}	Quiescent V _{BS} Current	V _{BS} =15 V, V _{IN} =0V	Applied Between $V_{B(U)}$ -U, $V_{B(V)}$ -V, $V_{B(W)}$ -W	-	-	100	μΑ
UV _{CCD}	Low-Side Undervoltage	V _{CC} Undervoltage	V _{CC} Undervoltage Protection Detection Level		8.0	9.4	V
UV _{CCR}	Protection (Figure 6)	V _{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV _{BSD}	High-Side Undervoltage	V _{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{BSR}	Protection (Figure 7)	V _{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V _{IH}	ON Threshold Voltage	Logic High Level	Applied between IN and COM	3.0	-	-	V
V _{IL}	OFF Threshold Voltage	Logic Low Level	Applied between in and COM	-	-	0.8	V
I _{IH}	Input Bias Current	V _{IN} = 5V	Applied between IN and COM	-	10	20	μΑ
I _{IL}	iliput bias Current	V _{IN} = 0V	Applied between IN and COM	-	-	2	μА

Note

- 1. BV_{DSS} is the Absolute Maximum Voltage Rating Between Drain and Source Terminal of Each MOSFET Inside Motion SPM[®]. V_{PN} Should be Sufficiently Less Than This Value Considering the Effect of the Stray Inductance so that V_{DS} Should Not Exceed BV_{DSS} in Any Case.
- 2. t_{ON} and t_{OFF} Include the Propagation Delay Time of the Internal Drive IC. Listed Values are Measured at the Laboratory Test Condition, and They Can be Different According to the Field Applications Due to the Effect of Different Printed Circuit Boards and Wirings. Please see Figure 4 for the Switching Time Definition with the Switching Test Circuit of Figure 5.
- 3. The peak current and voltage of each MOSFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Recommended Operating Condition

Symbol	Parameter	Conditions		Unit		
Symbol	Parameter	Conditions	Min.	Тур.	Max.	Ullit
V _{PN}	Supply Voltage	Applied Between P and N	-	300	400	V
V _{CC}	Control Supply Voltage	Applied Between V _{CC} and COM	13.5	15	16.5	V
V _{BS}	High-Side Bias Voltage	Applied Between V _B and V _S	13.5	15	16.5	V
V _{IN(ON)}	Input ON Threshold Voltage	Applied Between IN and COM	3.0	-	V _{CC}	V
V _{IN(OFF)}	Input OFF Threshold Voltage	Applied Between IN and COM	0	-	0.6	V
t _{dead}	Blanking Time for Preventing Arm-Short	$V_{CC} = V_{BS} = 13.5 \sim 16.5 \text{ V}, T_{J} \le 150^{\circ}\text{C}$	1.0	-	-	μs
f _{PWM}	PWM Switching Frequency	T _J ≤ 150°C	-	15	-	kHz

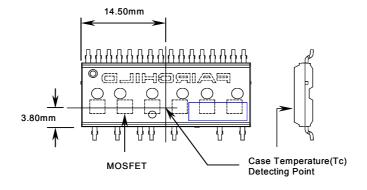


HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low side FRFET On
1	0	VDC	High side FRFET On
1	1	Forbidden	Shoot through
Open	Open	Z	Same as (0,0)

Note:

- 1. It is Recommended the Bootstrap Diode D₁ to Have Soft and Fast Recovery Characteristics with 600-V Rating.
- 2. Parameters for Bootstrap Circuit Elements are Dependent on PWM Algorithm. For 15 kHz of Switching Frequency, Typical Example of Parameters is Shown Above.
- $3. \ \ RC\ coupling\ (R_5\ and\ C_5)\ at\ Each\ Input\ of\ Motion\ SPM^{\textcircled{\tiny{\textcircled{\tiny{0}}}}}\ and\ Micom\ (Indicated\ as\ Dotted\ Lines)\ May\ be\ Used\ to\ Prevent\ Improper\ Signal\ Due\ to\ Surge\ Noise.$
- Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C₁, C₂ and C₃ Should Have Good High-Frequency characteristics to Absorb High-Frequency Ripple Current.

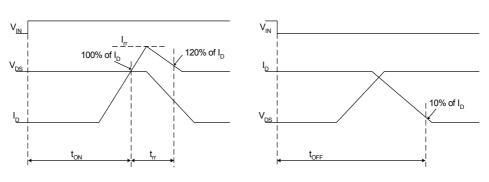
Figure 2. Recommended MCU Interface and Bootstrap Circuit with Parameters



Note:

Attach the thermocouple on top of the heatsink-side of Motion SPM (between Motion SPM and heatsink if applied) to get the correct temperature measurement.

Figure 3. Case Temperature Measurement



(a) Turn-on (b) Turn-off Figure 4. Switching Time Definitions

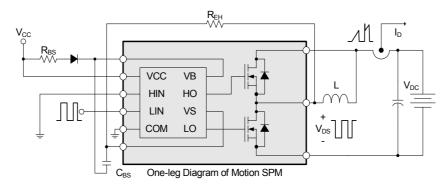


Figure 5. Switching and RBSOA (Single-pulse) Test Circuit (Low-side)

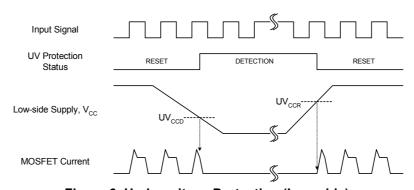


Figure 6. Undervoltage Protection (Low-side)

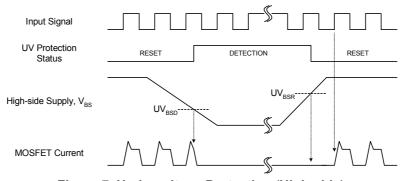
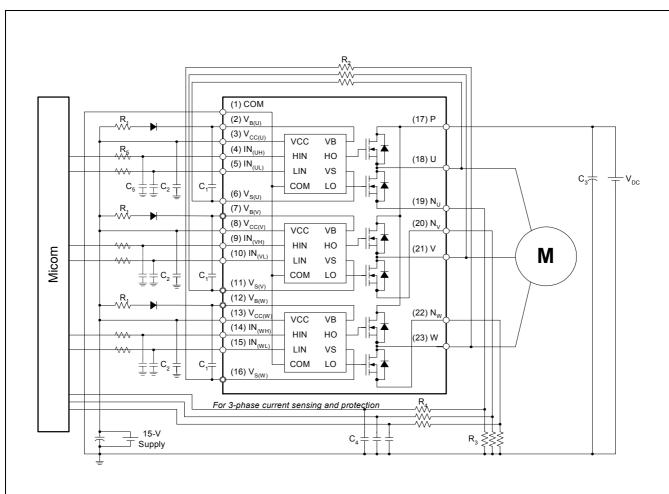


Figure 7. Undervoltage Protection (High-side)

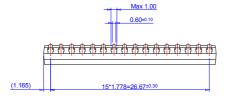


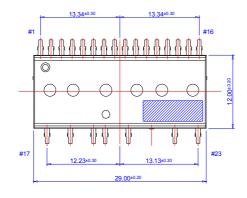
Note

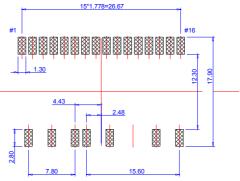
- 1. About Pin Position, Refer to Figure 1.
- $2. \ RC \ Coupling \ (R_5 \ and \ C_5, \ R_4 \ and \ C_4) \ at \ Each \ Input \ of \ Motion \ SPM^{\textcircled{\$}} \ and \ Micom \ are \ Useful \ to \ Prevent \ Improper \ Input \ Signal \ Caused \ by \ Surge \ Noise.$
- 3. The voltage Drop Across R₃ Affects the Low Side Switching Performance and the Bootstrap Characteristics Since it is Placed Between COM and the Source Terminal of the Low Side MOSFET. For this Reason, the Voltage Drop Across R₃ Should Be Less Than 1 V in the Steady-State.
- 4. Ground Wires and Output Terminals, Should Be Thick and Short in Order to Avoid Surge Voltage and Malfunction of HVIC.
- 5. All the Filter Capacitors Should Be Connected Close to Motion SPM, and They Should Have Good Characteristics for Rejecting High-Frequency Ripple Current.

Figure 8. Example of Application Circuit

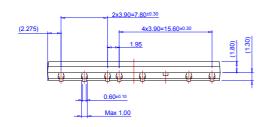
Detailed Package Outline Drawings

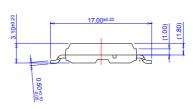


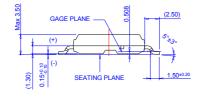




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