from Te

EMBER 2007

ES

- 5% Efficiency
- Protection
- Device Synchroniz
- t Protection
- s B EMC Performance
- ized Compone
- d SOP-14 P es

- Co
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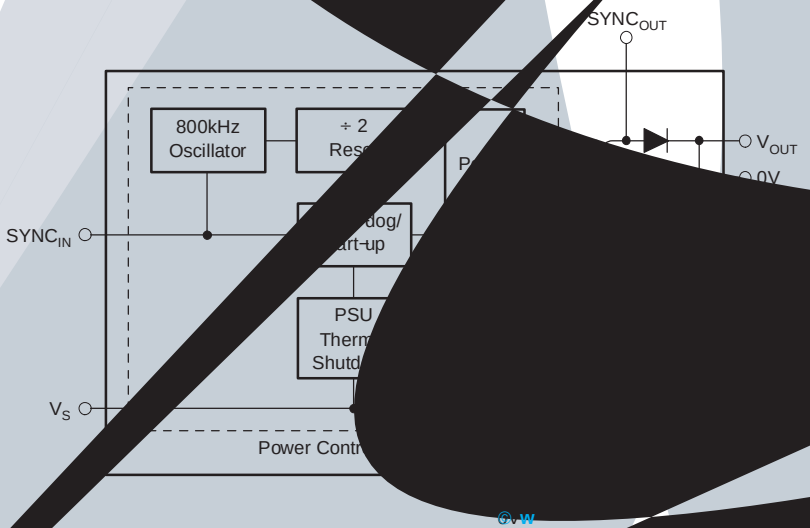
DESCRIPTION

The DCP01B series is a family of 1W, unregula isolated DC/DC converters. Requiring a minim external components and including on-chip protection, the DCP01B series provides ext such as output disable and synchronizatio frequencies.

The use of a highly-integrated packa results in highly reliable products with a po of 40W/in^3 (2.4W/cm^3). This combination o and small sizes makes the DCP01B suita for a wide range of applications.



ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = nominal, C_{IN} = 2.2µF, and C_{OUT} = 0.1µF, unless otherwise noted.

PARAMETER	TEST CONDITIONS		DCP01B SERIES MIN	DCP01B SERIES TYP	DCP01B SERIES MAX	UNITS
Output						
Power	100% full load			0.97		W
Ripple	O/P capacitor = 1µF, 50% load			20		mV_{PP}
Voltage vs temperature	Room to cold			0.046		%/°C
	Room to hot			0.016		%/°C
Input						
Voltage range on V_S			−10		+10	%
Isolation						
Voltage	1s flash test		1			kVrms
	60s test, UL1950(1)		1			kVrms
Line Regulation						
Output voltage	I_O = constant(2)	V_S (min) to V_S (typ)		1	15	%
		V_S (typ) to V_S (max)		1	15	%
Switching/Synchronization						
Oscillator frequency (f_{OSC})	Switcing frequency = f_{OSC}/2			800		kHz
Sync input low					0.4	V
Sync input current	V_{SYNC} = +2V			75		µA
Disable time				2		µs
Capacitance loading on $SYNC_{IN}$ pin	External				3	pF
Reliability						
Demonstrated	MSL 3−(U) versions, T_A = +55°C			55		FITS
Thermal Shutdown						
IC temperature at shutdown				+150		°C
Shutdown current				3		mA
Temperature Range						
Operating			−40		+100	°C

(1) During UL1950 recognition tests only.
(2) I_{OUT} ≥ 10% load current.

ELECTRICAL CHARACTERISTICS PER DEVICE

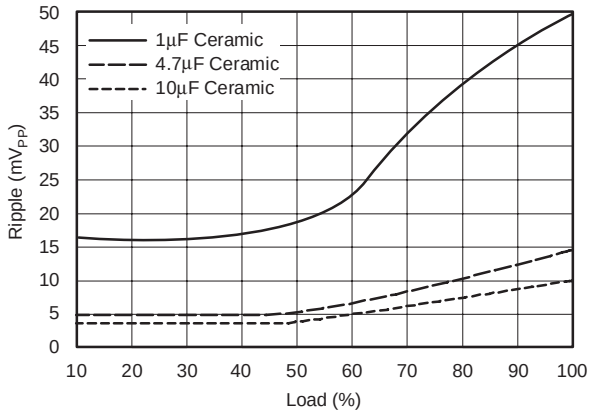
At T_A = +25°C, V_S = nominal, C_{IN} = 2.2µF, and C_{OUT} = 0.1µF, unless otherwise noted.

	INPUT VOLTAGE (V)	OUTPUT VOLTAGE (V)	LOAD REGULATION (%)	NO LOAD CURRENT (mA)	EFFICIENCY (%)	BARRIER CAPACITANCE (pF)
	V_S	V_{NOM} AT V_S (TYP)		I_Q		C_{ISO}
		75% LOAD(3)	10% TO 100% LOAD(4)	0% LOAD	100% LOAD	V_{ISO}

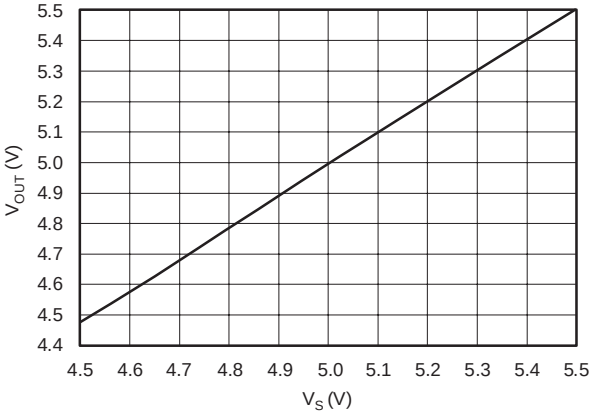
TYPICAL CHARACTERISTICS

At T_A = 25°C, unless otherwise noted.

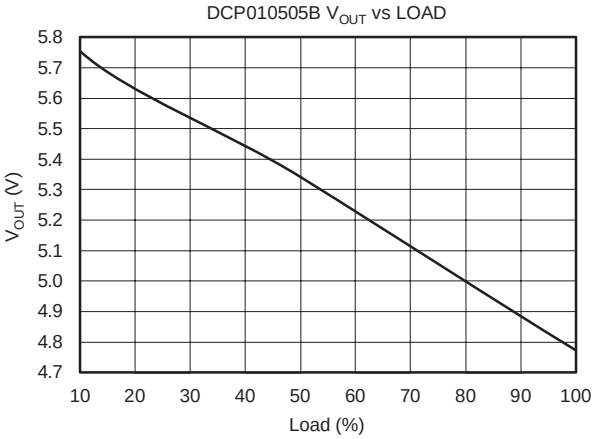
DCP010505B
OUTPUT RIPPLE vs LOAD (20MHz BW)

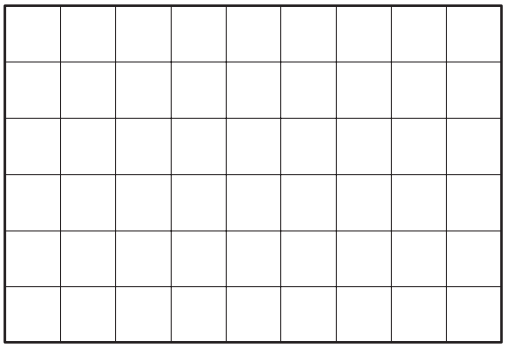


DCP010505B V_{OUT} vs V_S



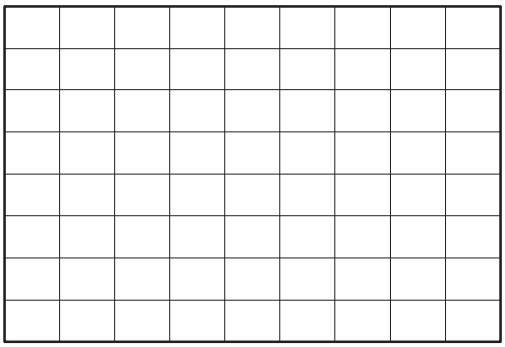
DCP010505B V_{OUT} vs LOAD

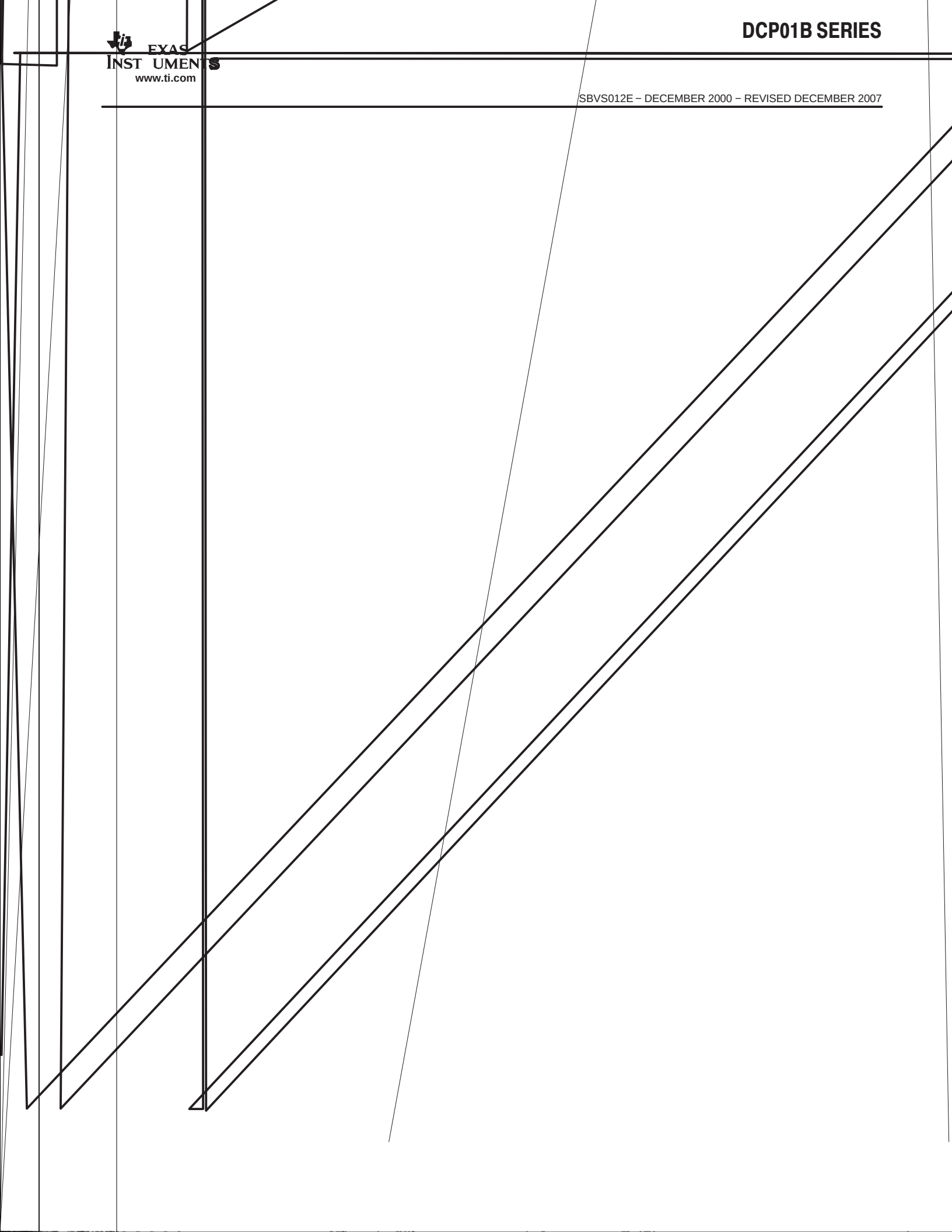




TYPICAL CHARACTERISTICS (continued)

At T_A = 25°C, unless otherwise noted.





FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP01B offers up to 1W of unregulated output power with a typical efficiency of up to 85%. This is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design uses an advanced BiCMOS/DMOS process. For additional information, refer to the application notes located in the DCP01B product folder at www.ti.com.

POWER STAGE

This uses a push-pull, center-tapped topology switching at 400kHz (divide-by-2 from 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP01B circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the SYNC pin low. The output pins will be tri-stated. This will occur in 2µs.

THERMAL SHUTDOWN

The DCP01B is protected by a thermal shutdown circuit. If the on-chip temperature exceeds 150°C, the device will shut down. Once the temperature falls below 150°C, normal operation will resume. If the thermal condition continues, operation will randomly cycle on and off. This will continue until the temperature is reduced.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This is due to the small variations in switching frequencies between the DC/DC converters.

The DCP01B overcomes this by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the $SYNC_{IN}$ pins together, taking care to minimize the stray capacitance. Stray capacitance (> 3pF) will have the effect of reducing the switching frequency, or even stopping the oscillator circuit.

If synchronized devices are used, it should be noted that at startup, all devices will draw maximum current simultaneously. This can cause the input voltage to dip. If it dips below the minimum input voltage (4.5V), the devices may not start up. A 2.2µF capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the $SYNC_{IN}$ pins are driven by an external device. Details are contained in Application Report SBAA035, *External Synchronization of the DCP01/02 Series of DC/DC Converters*, available for download at www.ti.com.

CONSTRUCTION

The DCP01B basic construction is the same as standard ICs. There is no substrate within the molded package. The DCP01B is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Since there is no solder within the package, the DCP01B does not require any special PCB assembly processing. This results in an isolated DC/DC converter with inherently high reliability.

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP01B can be disabled or enabled by driving the $SYNC_{IN}$ pin using an open drain CMOS gate. If the $SYNC_{IN}$ pin is pulled low, the DCP01B will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2µs. Removal of the pull-down will cause the DCP01B to be enabled.

Capacitive loading on the $SYNC_{IN}$ pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

A high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that at least a 1µF capacitor is used on V_{OUT}. Dual outputs should have both the positive and negative buses decoupled to V_{OUT} ground (pin 5). The required 2.2µF low equivalent series resistance (ESR) ceramic capacitor on the input of the 5V to 15V versions, and the ≥ 0.47µF low-ESR ceramic capacitor on the 24V versions help reduce ripple and noise. See Application Bulletin SBVA012, *DC-to-DC Converter Noise Reduction*, available for download at www.ti.com.

Connecting the DCP01B in Series

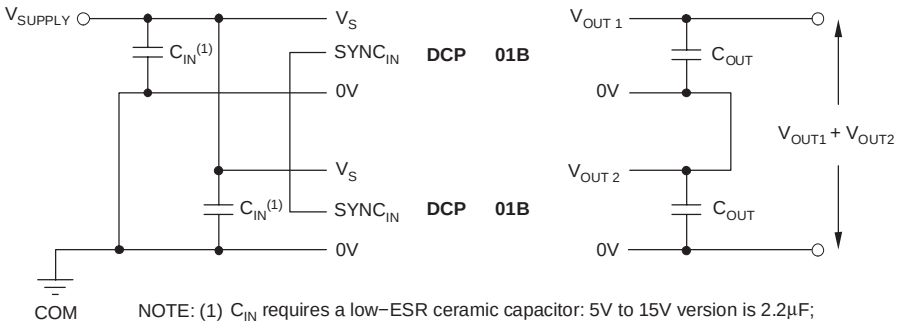
Multiple DCP01B isolated 1W DC/DC converters can be connected in series to provide nonstandard voltage rails. This is possible by using the floating outputs provided by the DCP01B galvanic isolation.

Connect the positive V_{OUT} from one DCP01B to the negative V_{OUT} (0V) of another, as shown in Figure 1. If the $SYNC_{IN}$ pins are tied together, the self-synchronization feature of the DCP01B will prevent beat frequencies on the voltage rails. The $SYNC_{IN}$ feature of the DCP01B allows easy connection in series, which reduces separate filtering components.

The outputs on dual output DCP01B versions can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 2. For example, a dual 15V DCP01B could be connected to provide a 30V rail.

Connecting the DCP01B in Parallel

If the output power from one DCP01B is not sufficient, it is possible to parallel the outputs of multiple DCP01B converters (see Figure 3). Again, the $SYNC_{IN}$ feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.



NOTE: (1) C_{IN} requires a low−ESR ceramic capacitor: 5V to 15V version is 2.2µF; 24V version is minimum 0.47µF. C_{OUT} = 1.0µF.

Decoupling Ceramic Capacitors

All capacitors have losses due to their internal equivalent series resistance (ESR), and to a lesser degree their equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of Frequency versus Capacitor Impedance. These will show the capacitors' impedance falling as frequency is increased (see Figure 4). As the frequency is increased, the impedance will stop decreasing and begin to rise. The point of minimum impedance indicates the capacitors' resonant frequency. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.

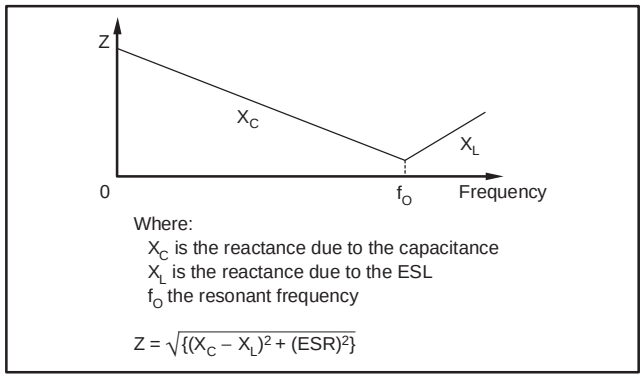


Figure 4. Capacitor Impedance vs Frequency

At f_O, $X_C = X_L$; however, there is a 180° phase difference resulting in cancellation of the imaginary component. The resulting effect is that the impedance at the resonant point is the real part of the complex impedance; namely, the value of the ESR. The resonant frequency must be well above the 800kHz switching frequency of the DCP and DCVs.

The effect of the ESR is to cause a voltage drop within the capacitor. The value of this voltage drop is simply the product of the ESR and the transient load current, as shown in Equation (1):

$$V_{IN} = V_{PK} - (ESR \times I_{TR})$$

Where:

V_{IN} is the voltage at the device input.

V_{PK} is the maximum value of the voltage on the capacitor during charge.

I_{TR} is the transient load current.

The other factor that affects the performance is the value of the capacitance. However, for the input and the full wave outputs (single-output voltage devices), the ESR is the dominant factor.

Input Capacitor and the effects of ESR

If the input decoupling capacitor is not ceramic with < 20mΩ ESR, then at the instant the power transistors switch on, the voltage at the input pins will fall momentarily. Should the voltage fall below approximately 4V, the DCP will detect an under-voltage condition and switch the DCP drive circuits to the off state. This is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. This would result in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value. Then the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process is repeated until the capacitor is charged sufficiently to start the device correctly. Otherwise, the device will be caught up in a loop.

Normal startup should occur in approximately 1ms from power being applied to the device. If a considerably longer startup duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5V to 15V input devices, a 2.2µF low-ESR ceramic capacitor will ensure a good startup performance, and for the remaining input voltage ranges, 0.47µF ceramic capacitors are good. Tantalum capacitors are not recommended, since most do not have low-ESR values and will degrade performance. If tantalum capacitors must be used, close attention must be paid to both the ESR and voltage as derated by the vendor.

Output Ripple Calculation Example

DCP020505: Output voltage 5V, Output current 0.4A. At full output power, the load resistor is 12.5Ω. Output capacitor of 1µF, ESR of 0.1Ω. Capacitor discharge time 1% of 800kHz (ripple frequency):

$t_{DIS} = 0.0125\mu s$

τ = C ×ficientl3 1 0 0 1 TD 0 Tw Tf 10d(µ) Tm 0.0053 Tc (DIS)T

DUAL OUTPUT VOLTAGE DCP AND DCVs

The voltage output for the dual DCPs is half wave rectified; therefore, the discharge time is 1.25µs. Repeating the above calculations using the 100% load resistance of 25Ω (0.2A per output), the results are shown below:

τ = 25µs

t_{DIS} = 1.25µs.

V_{DIS} = 244mV

V_{ESR} = 20mV

Ripple Voltage = 266mV

This time, it is the capacitor discharging that is contributing to the largest component of ripple. Changing the output filter to 10µF, and repeating the calculations:

Ripple Voltage = 45mV.

This value is composed of almost equal components.

The above calculations are given only as a guide. Capacitor parameters usually have large tolerances and can be susceptible to environmental conditions.

PCB LAYOUT

Figure 5 and Figure 6 illustrate a printed circuit board (PCB) layout for the two conventional (DCP01/02, DCV01), and two SO-28 surface-mount packages (DCP02U). Figure 7 shows the schematic.

Input power and ground planes have been used, providing a low-impedance path for the input power. For the output, the common or 0V has been connected via a ground plane, while the connections for the positive and negative voltage outputs are conducted via wide traces in order to minimize losses.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance; thus, improving the ripple performance. This is of particular importance to the input decoupling

Figure 5. Example of PCB Layout, Component-Side View

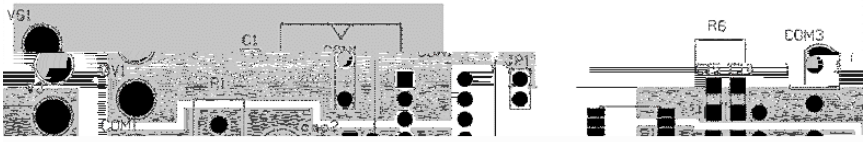
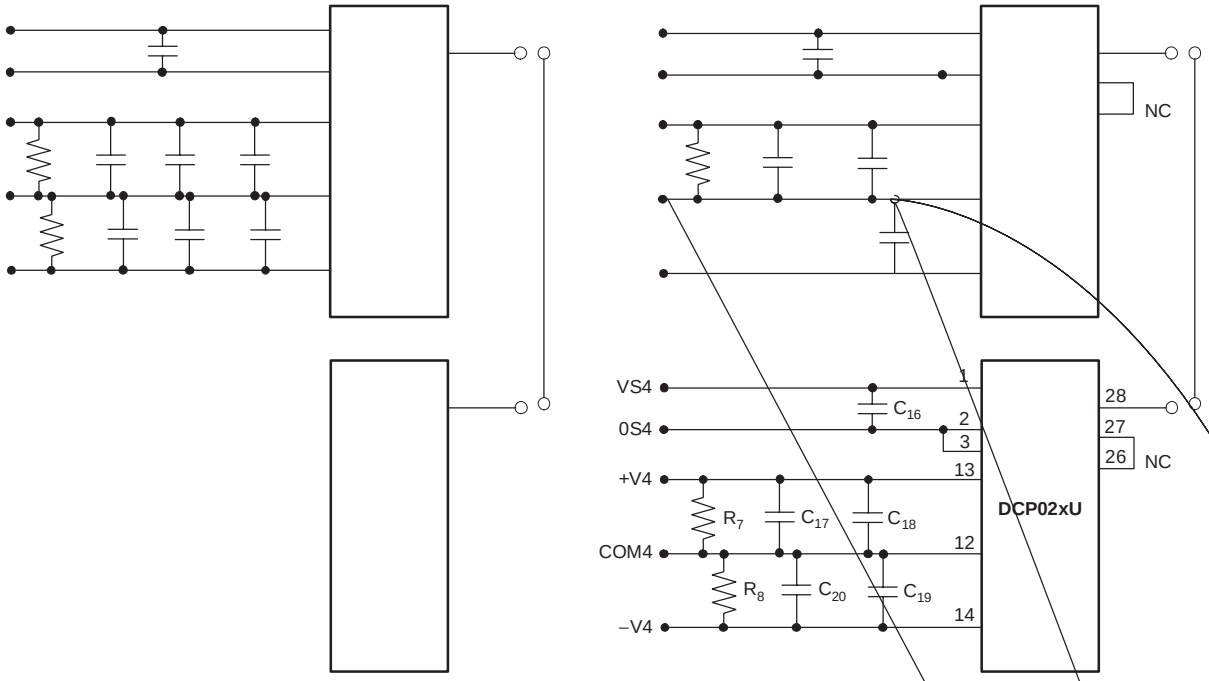


Figure 6. Example of PCB Layout, Non-component-Side View



(1) Capacitors C2−1, C4−1, C7−1, and C9−1 are through-hole plated components connected in parallel with C2, C4, C7 and C9 (1206 SMD), respectively.
(2) For optimum low-noise performance, use low-ESR capacitors.
(3) Do not connect the SYNC pin jumper (JP1−JP4) if the SYNC function is not being used.
(4) Connections to the power input should be made with a minimum wire of 16/0.2 twisted pair, with the length kept short.
(5) VSx and 0Vx are input supply and ground respecively (x represents the channel).
(6) +Vx and −Vx are the positive and negative outputs, referenced to a common ground COMx.
(7) JPx are the links used for self-synchronization; if this facility is not being used, the links should be unconnected.
(8) R1−R8 are the power output loads; do not fit these if an external load is connected.
(9) CON1 and CON2 are DIL-14; CON3 and CON4 are SO-28 packages.
(10) NC = not connected.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCP010505BP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010505BP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505BP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505BP-U/7E4	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505BP-UE4	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505DBP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010505DBP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505DBP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505DBP-U/7E4	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010505DBP-UE4	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010507DBP-U/7E4	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010507DBP-UE4	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010507DBPE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010512BP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010512BP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010512BP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010512DBP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010512DBP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010512DBP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010512DBPE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010515BP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010515BP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010515BP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP010515DBP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP010515DBP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR

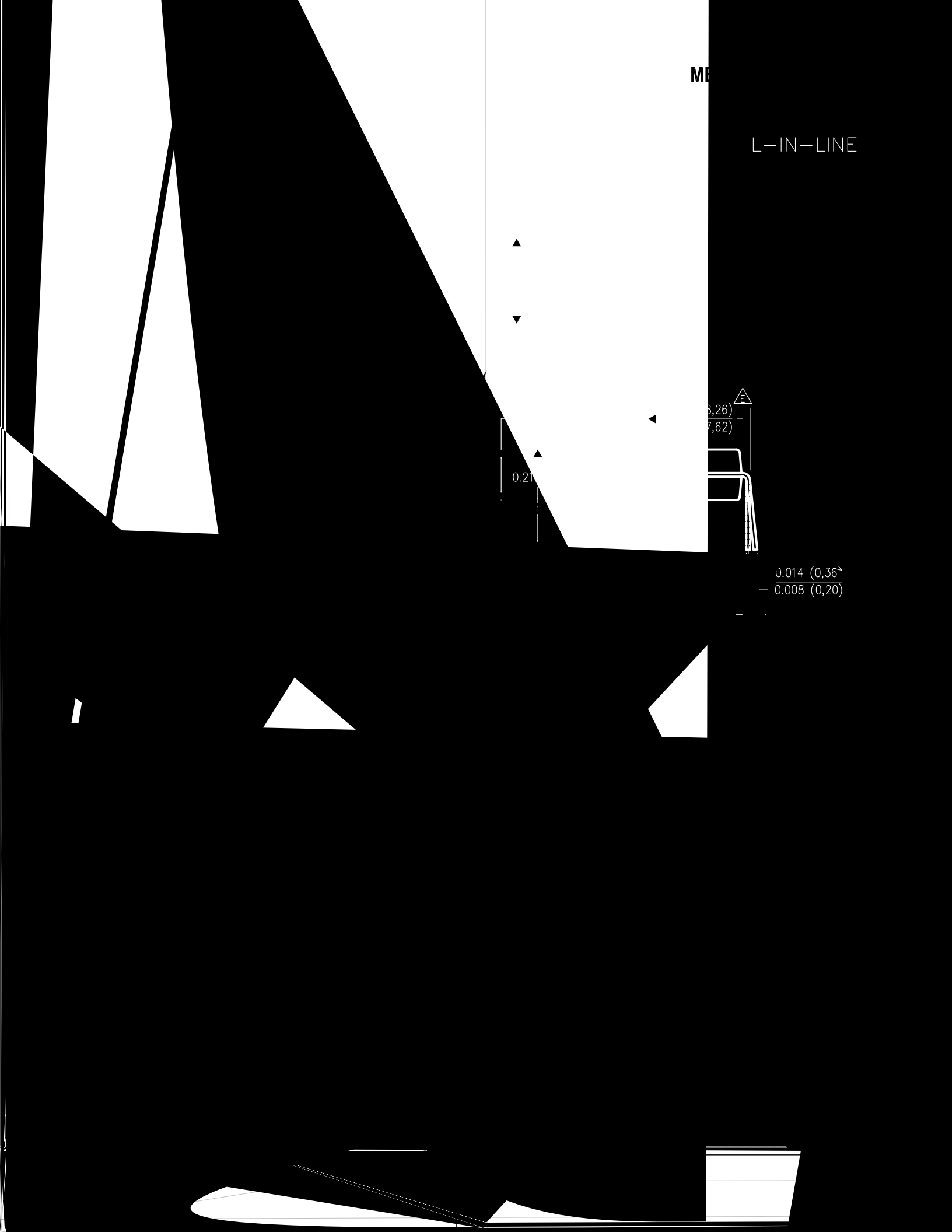
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
DCP010515DBP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP011512DBP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP011512DBP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP011512DBP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP011515DBP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP011515DBP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP011515DBP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP012405BP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP012405BP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP012415DBP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
DCP012415DBP-U	ACTIVE	SOP	DUA	7	25	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
DCP012415DBP-U/700	ACTIVE	SOP	DUA	7	700	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

to Customer on an annual basis.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0.008 (0,20)

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