Miniature, 2W, Isolated UNREGULATED DC/DC CONVERTERS

FEATURES

- **Up To 89% Efficiency**
- **Thermal Protection**
- **Device-to-Device Synchronization**
- **SO-28 Power Density of 106W/in^3 (6.5W/cm^3)**
- **EN55022 Class B EMC Performance**
- **UL1950 Recognized Component**
- **JEDEC 14-Pin and SO-28 Packages**

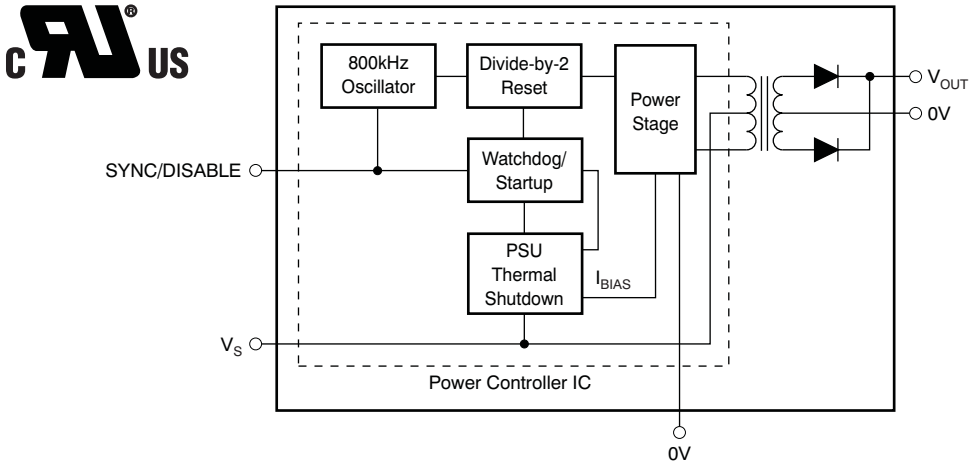
APPLICATIONS

- **Point-of-Use Power Conversion**
- **Ground Loop Elimination**
- **Data Acquisition**
- **Industrial Control and Instrumentation**
- **Test Equipment**

DESCRIPTION

The DCP02 series is a family of 2W, isolated, unregulated DC/DC converters. Requiring a minimum of external components and including on-chip device protection, the DCP02 series provides extra features such as output disable and synchronization of switching frequencies.

The use of a highly integrated package design results in highly reliable products with power densities of 79W/in^3 (4.8W/cm^3) for DIP-14, and 106W/in^3 (6.5W/cm^3) for SO-28. This combination of features and small size makes the DCP02 suitable for a wide range of applications.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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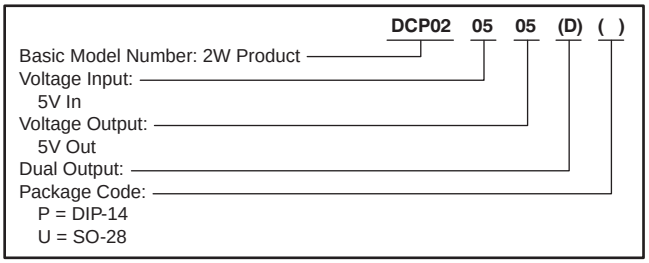
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING

For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI website at www.ti.com.

Supplemental Ordering Information



ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (unless otherwise noted) (1)

PARAMETER		DCP02 Series	UNIT
Input Voltage	5V input models	7	V
	12V input models	15	V
	15V input models	18	V
	24V input models	29	V
Storage temperature range		–60 to +125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
OUTPUT						
Power	100% full load			2		W
Ripple	Output capacitor = 1µF, 50% load			20		mV_{PP}
Voltage vs. Temperature	Room to cold			0.046		%/°C
	Room to hot			0.016		%/°C
INPUT						
Voltage range on V_S			–10		10	%
ISOLATION						
Voltage	1s Flash test		1			kVrms
	60s test, UL1950(1)		1			kVrms
LINE REGULATION						
Output Voltage	I_O = constant(2)	V_S (min) to V_S (typ)		1	15	%
		V_S (typ) to V_S (max)		1	15	%

(1) During UL1950 recognition tests only.
(2) I_{OUT} 10% load current

DEVICE INFORMATION

NVA PACKAGE
DIP-14 (Single-DIP)
(Top View)

NVA PACKAGE
DIP-14 (Dual-DIP)
(Top View)

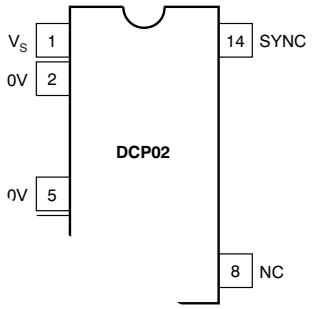


Table 1. Pin Description (Single-DIP)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
NC	7, 8	Not connected
SYNC	14	Synchronization pin

DVB PACKAGE
SO-28 (Single-SO)
(Top View)

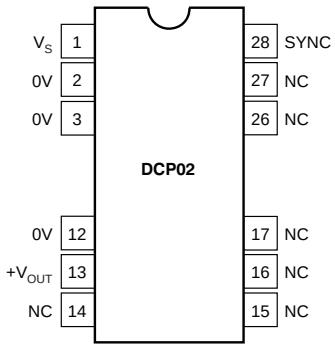


Table 2. TERMINAL FUNCTIONS (Single-SO)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	3	Input side common
0V	12	Output side common
$+V_{OUT}$	13	+Voltage out
NC	14, 15, 16, 17, 26, 27	Not connected
SYNC	28	Synchronization pin

Table 3. TERMINAL FUNCTIONS (Dual-DIP)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	5	Output side common
$+V_{OUT}$	6	+Voltage out
$-V_{OUT}$	7	–Voltage out
NC	8	Not connected
SYNC	14	Synchronization pin

DVB PACKAGE
SO-28 (Dual-SO)
(Top View)

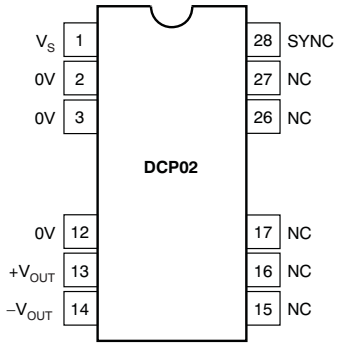


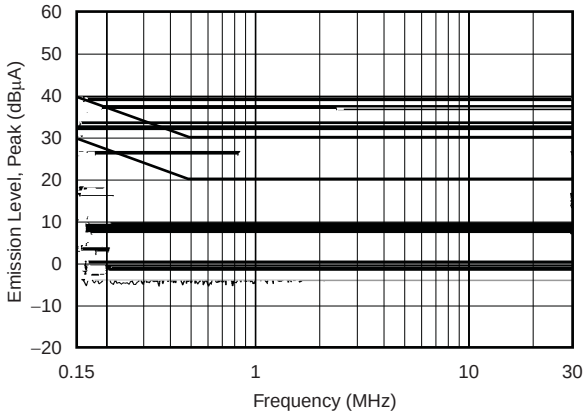
Table 4. TERMINAL FUNCTIONS (Dual-SO)

TERMINAL		
NAME	NO.	DESCRIPTION
V_S	1	Voltage input
0V	2	Input side common
0V	3	Input side common
0V	12	Output side common
$+V_{OUT}$	13	+Voltage out
$-V_{OUT}$	14	–Voltage out
NC	15, 16, 17, 26, 27	Not connected
SYNC	28	Synchronization pin

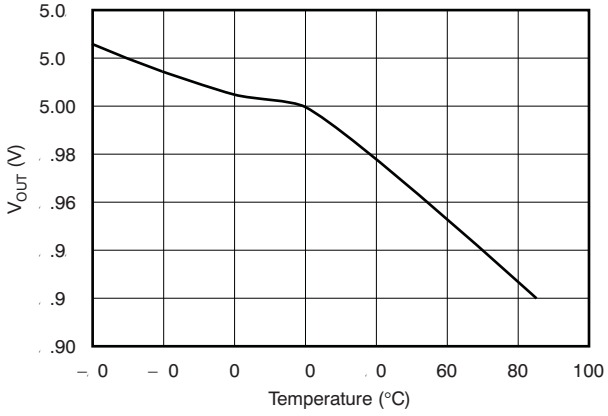
TYPICAL CHARACTERISTICS

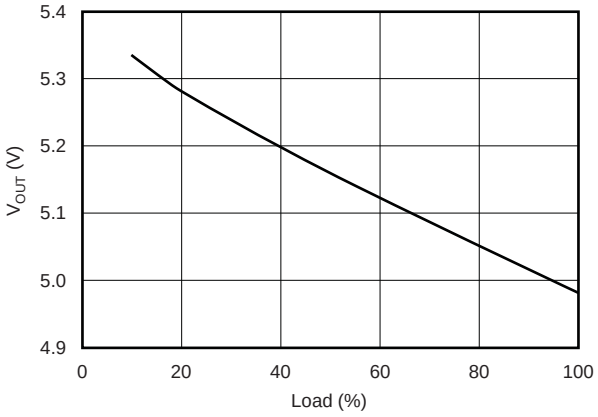
At T_A = +25°C, unless otherwise noted.

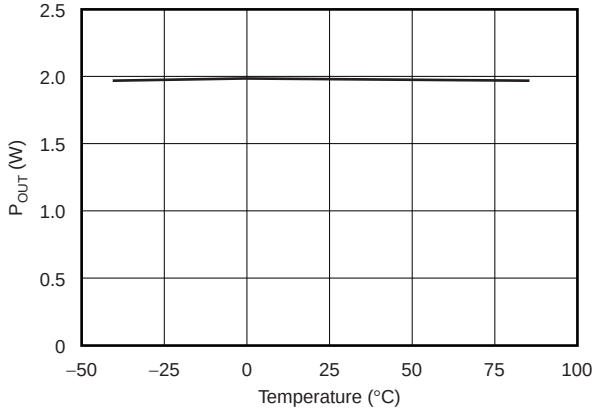
DCP020505P
CONDUCTED EMISSIONS (500mA Load)

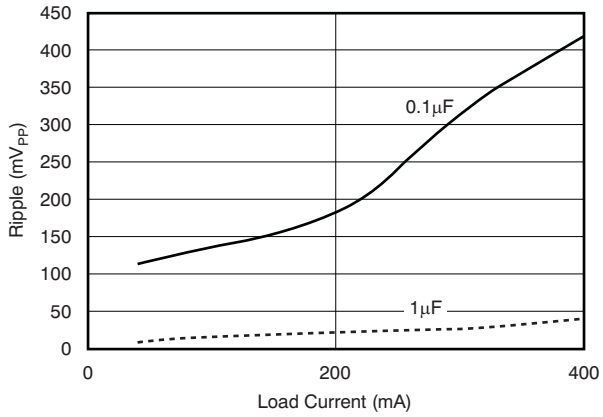


DCP020505P
V_{OUT} vs









FUNCTIONAL DESCRIPTION

OVERVIEW

The DCP02 offers up to 2W of unregulated output power from a 5V, 12V, 15V, or 24V input source with a typical efficiency of up to 89%. This efficiency is achieved through highly integrated packaging technology and the implementation of a custom power stage and control IC. The circuit design uses an advanced BiCMOS/DMOS process.

POWER STAGE

The DCP02 uses a push-pull, center-tapped topology switching at 400kHz (divide-by-2 from an 800kHz oscillator).

OSCILLATOR AND WATCHDOG

The onboard 800kHz oscillator generates the switching frequency via a divide-by-2 circuit. The oscillator can be synchronized to other DCP02 circuits or an external source, and is used to minimize system noise.

A watchdog circuit checks the operation of the oscillator circuit. The oscillator can be stopped by pulling the SYNC pin low. The output pins will be tri-stated, which occurs in 2µs.

THERMAL SHUTDOWN

The DCP02 is protected by a thermal-shutdown circuit. If the on-chip temperature exceeds +150°C, the device will shut down. Once the temperature falls below +150°C, normal operation resumes.

SYNCHRONIZATION

In the event that more than one DC/DC converter is needed onboard, beat frequencies and other electrical interference can be generated. This interference occurs because of the small variations in switching frequencies between the DC/DC converters.

The DCP02 overcomes this interference by allowing devices to be synchronized to one another. Up to eight devices can be synchronized by connecting the SYNC pins together, taking care to minimize the capacitance of tracking. Stray capacitance (> 10pF) has the effect of reducing the switching frequency, or even stopping the oscillator circuit. It is also recommended that power and ground lines be star-connected.

It should be noted that if synchronized devices are used at start up, all devices will draw maximum current simultaneously. This configuration can cause the input voltage to dip; if it dips below the minimum input voltage (4.5V), the devices may not start up. A 2.2µF capacitor should be connected close to the input pins.

If more than eight devices are to be synchronized, it is recommended that the SYNC pins be driven by an external device. Details are contained in Application Report SBAA035, External Synchronization of the DCP01/02 Series of DC/DC Converters, available for download from www.ti.com.

CONSTRUCTION

The basic construction of the DCP02 is the same as standard ICs; there is no substrate within the molded package. The DCP02 is constructed using an IC, rectifier diodes, and a wound magnetic toroid on a leadframe. Since there is no solder within the package, the DCP02 does not require any special printed circuit board (PCB) assembly processing. This architecture results in an isolated DC/DC converter with inherently high reliability.

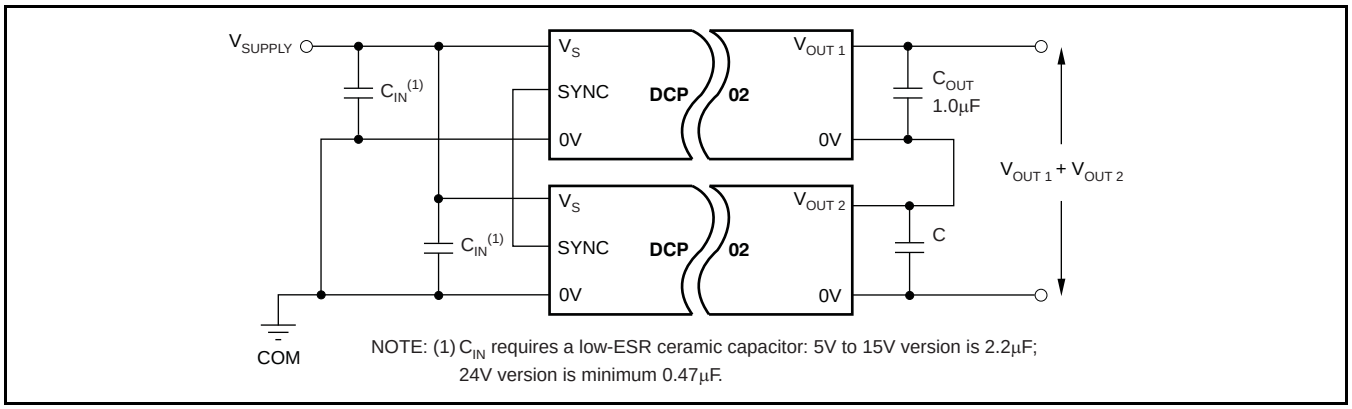


Figure 7. Connecting the DCP02 in Series

ADDITIONAL FUNCTIONS

DISABLE/ENABLE

The DCP02 can be disabled or enabled by driving the SYNC pin using an open drain CMOS gate. If the SYNC pin is pulled low, the DCP02 will be disabled. The disable time depends upon the external loading; the internal disable function is implemented in 2µs. Removal of the pull down causes the DCP02 to be enabled.

Capacitive loading on the SYNC pin should be minimized in order to prevent a reduction in the oscillator frequency.

DECOUPLING

Ripple Reduction

The high switching frequency of 400kHz allows simple filtering. To reduce ripple, it is recommended that a 1µF capacitor be used on V_{OUT}. Dual outputs should both be decoupled to pin 5. A 2.2µF capacitor on the input is also recommended.

Connecting the DCP02 in Series

Multiple DCP02 isolated 2W DC/DC converters can be connected in series to provide nonstandard voltage rails. This configuration is possible by using the floating outputs provided by the galvanic isolation of the DCP02.

Connect the positive V_{OUT} from one DCP02 to the negative V_{OUT} (0V) of another (see Figure 7). If the SYNC pins are tied together, the self-synchronization feature of the DCP02 prevents beat frequencies on the voltage rails. The SYNC feature of the DCP02 allows easy series connection without external filtering, thus minimizing cost.

The outputs on the dual-output DCP02 versions can also be connected in series to provide two times the magnitude of V_{OUT}, as shown in Figure 8. For example, a dual 15V DCP022415D could be connected to provide a 30V rail.

Connecting the DCP02 in Parallel

If the output power from one DCP02 is not sufficient, it is possible to parallel the outputs of multiple DCP02s, as shown in Figure 9. Again, the SYNC feature allows easy synchronization to prevent power-rail beat frequencies at no additional filtering cost.

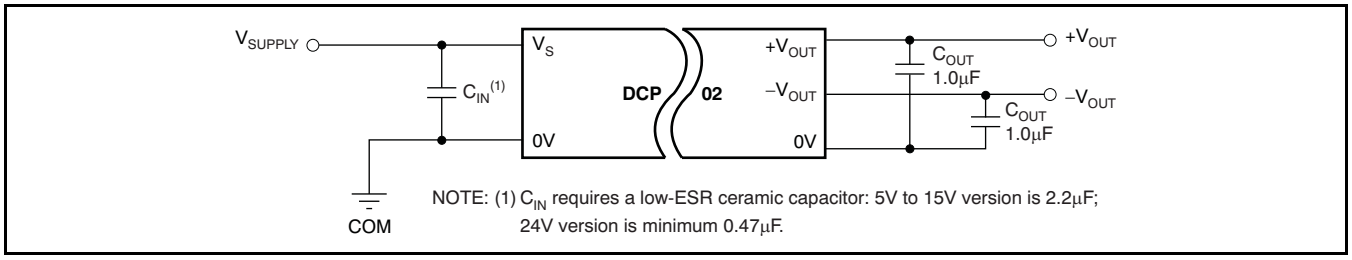


Figure 8. Connecting Dual Outputs in Series

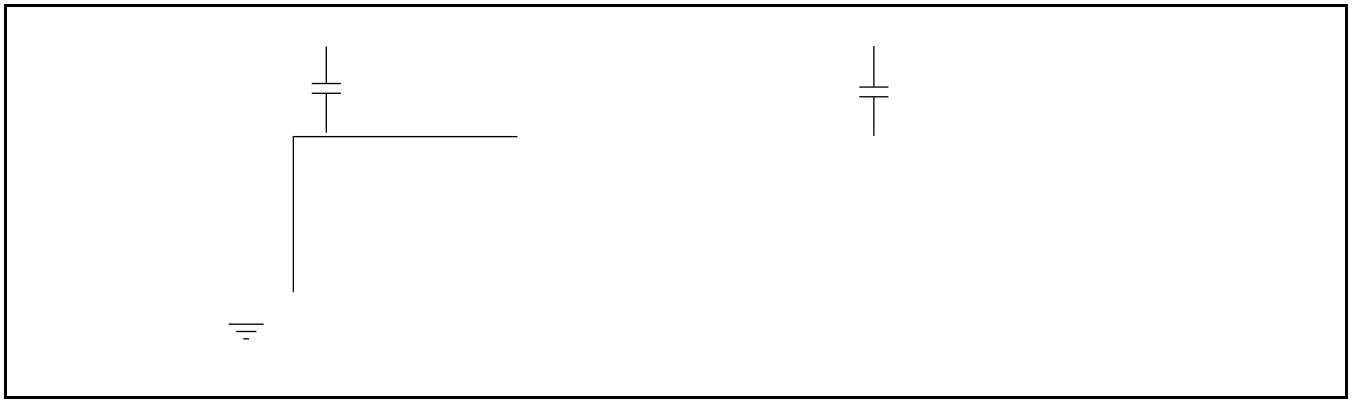


Figure 9. Connecting Multiple DCP02s in Parallel

APPLICATION INFORMATION

OPTIMIZING PERFORMANCE

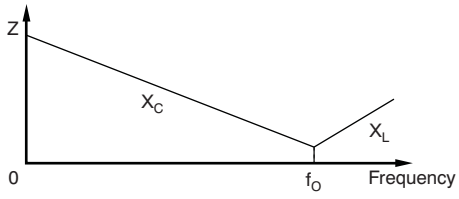
TRANSFORMER DRIVE CIRCUIT

SELF-SYNCHRONIZATION

PCB Design

Decoupling Ceramic Capacitors

All capacitors have losses because of internal equivalent series resistance (ESR), and to a lesser degree, equivalent series inductance (ESL). Values for ESL are not always easy to obtain. However, some manufacturers provide graphs of frequency versus capacitor impedance. These graphs typically show the capacitor impedance falling as frequency is increased (as shown in Figure 10). As the frequency increases, the impedance stops decreasing and begins to rise. The point of minimum impedance indicates the resonant frequency of the capacitor. This frequency is where the components of capacitance and inductance reactance are of equal magnitude. Beyond this point, the capacitor is not effective as a capacitor.



$$Z = \sqrt{(X_C - X_L)^2 + (ESR)^2}$$

Where:

X_C is the reactance due to the capacitance.
X_L is the reactance due to the ESL.
f_O is the resonant frequency.

Input Capacitor and the Effects of ESR

If the input decoupling capacitor is not ceramic with <20m ESR, then at the instant the power transistors switch on, the voltage at the input pins falls momentarily. Should the voltage fall below approximately 4V, the DCP detects an under-voltage condition and switches the DCP drive circuits to the off state. This detection is carried out as a precaution against a genuine low input voltage condition that could slow down or even stop the internal circuits from operating correctly. A slow-down or stoppage would result in the drive transistors being turned on too long, causing saturation of the transformer and destruction of the device.

Following detection of a low input voltage condition, the device switches off the internal drive circuits until the input voltage returns to a safe value. Then the device tries to restart. If the input capacitor is still unable to maintain the input voltage, shutdown recurs. This process is repeated until the capacitor is charged sufficiently to start the device correctly. Otherwise, the device will be caught up in a loop.

Normal startup should occur in approximately 1ms from power being applied to the device. If a considerably longer startup duration time is encountered, it is likely that either (or both) the input supply or the capacitors are not performing adequately.

For 5V to 15V input devices, a 2.2µF low-ESR ceramic capacitor ensures a

Clearly, increasing the capacitance has a much smaller effect on the output ripple voltage than does reducing the value of the ESR for the filter capacitor.

DUAL OUTPUT VOLTAGE DCP AND DCVs

length.

The voltage output for the dual DCPs is half wave rectified; therefore, the discharge time is 1.25µs. Repeating the above calculations using the 100% load resistance of 25 (0.2A per output), the results are:

τ = 25µs

t_{DIS} = 1.25µs

V_{DIS} = 244mV

V_{ESR} = 20mV

Ripple Voltage = 266mV

This time, it is the capacitor discharging that contributes to the largest component of ripple. Changing the output filter to 10µF, and repeating the calculations, the result is:

Ripple Voltage = 45mV.

This value is composed of almost equal components.

The previous calculations are given

PCB LAYOUT

The $SYNC_{IN}$ pin, when not being used, is best left as a floating pad. A ground ring or annulus connected around the pin prevents noise being conducted onto the pin. If the $SYNC_{IN}$ pin is to be connected to one or more $SYNC_{IN}$ pins, then the linking trace should be narrow and must be kept short in length. In addition, no other trace should be in close proximity to this trace because that will increase the stray capacitance on this pin. In turn, the stray capacitance affects the performance of the oscillator.

Ripple and Noise

Careful consideration should be given to the layout of the PCB in order to obtain the best results.

The DCP02 is a switching power supply, and as such can place high peak current demands on the input supply. In order to avoid the supply falling momentarily during the fast switching pulses, ground and power planes should be used to connect the power to the input of DCP02. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

THERMAL MANAGEMENT

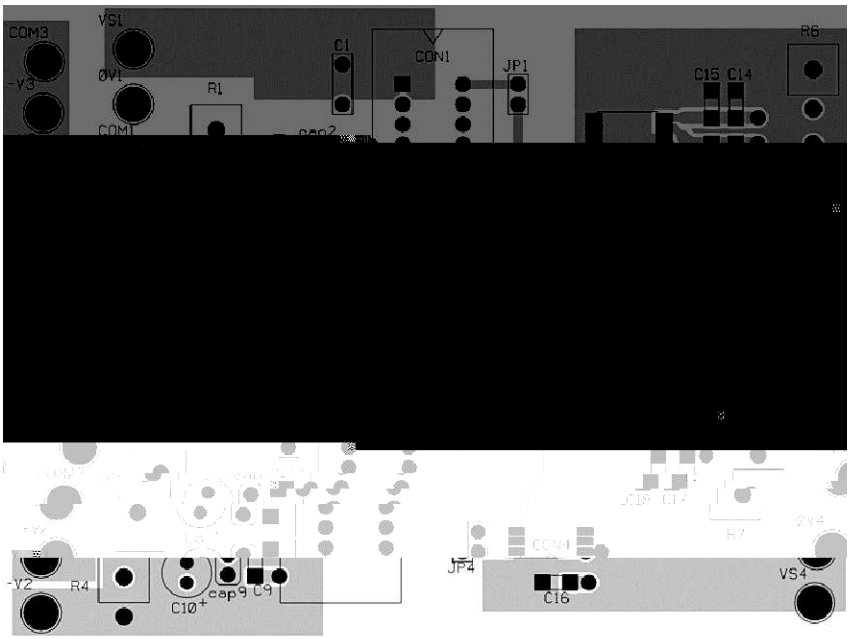


Figure 11. Example of PCB Layout, Component-Side View

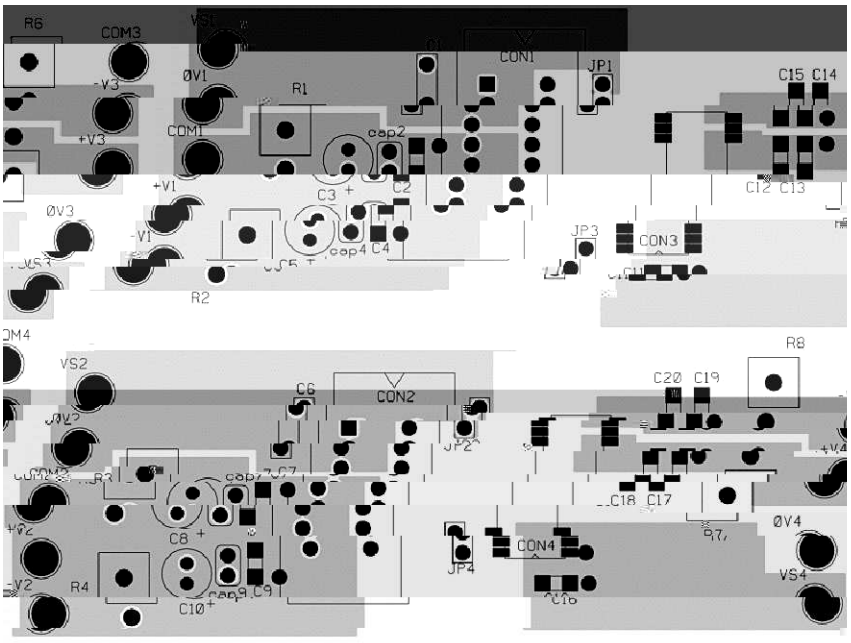


Figure 12. Example of PCB Layout, Non-Component-Side View

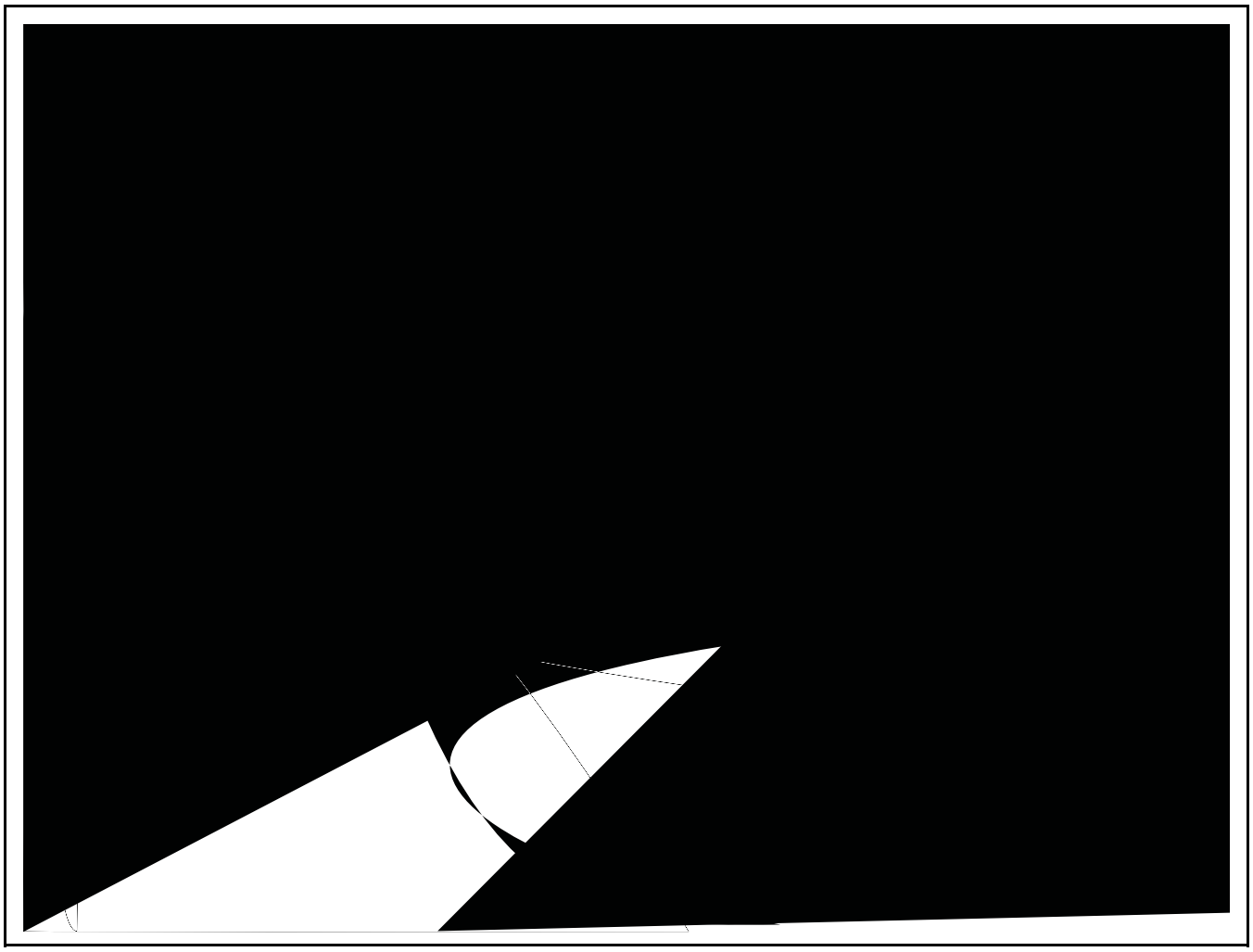
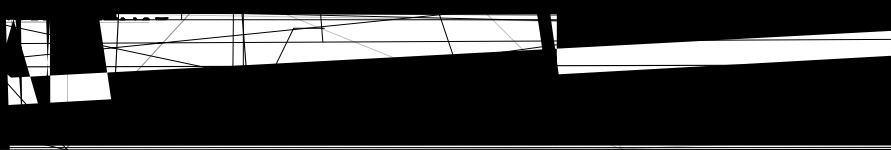


Figure 13. Example of PCB Layout, Schematic Diagram

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DCP020503P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP020503U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP020505P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP020505U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP020505U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP020505U/1KE4	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP020505UE4	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP020507P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP020507U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP020507U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP020509P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP020509U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP020509U/1K	OBSOLETE	SOP	DVB	12		TBD	Call TI	Call TI	Samples Not Available
DCP020515DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP020515DU	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP020515DU/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP021205P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP021205PE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP021205U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP021205U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP021212DP	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP021212DU	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP021212DU/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP021212P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP021212U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP021212U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples
DCP021515P	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP021515PE4	ACTIVE	PDIP	NVA	7	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	Request Free Samples
DCP021515U	ACTIVE	SOP	DVB	12	28	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Request Free Samples
DCP021515U/1K	ACTIVE	SOP	DVB	12	1000	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR	Purchase Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
DCP022405DP	ACTIVE	PDIP	NVA	7	25				



MPDS106A – AUGUST 2001 – REVISED NOVEMBER 2001

DVB(R-PDSO-G12/28) **PLASTIC SMALL-OUTLINE**