

LXMG1644-12-61

12V Quad 6W CCFL Programmable Inverter Module

PRODUCTION DATASHEET

DESCRIPTION

The LXMG1644-12-61 is a Quad 6W Output Direct DriveTM CCFL (Cold range dimming, amplitude control results Cathode Fluorescent Lamp) Inverter in lower ripple on the input supply and Module specifically designed for driving reduced LCD backlight lamps. It is ideal for generation. Many STN type panels are driving typical 12.1" to 18.1" TFT panels.

The modules are available with a amplitude dimming. dimming input that permits brightness control from either a DC voltage source or the system battery or AC adapter directly a PWM signal or external Potentiometer. to high frequency, high-voltage waves The maximum output current is externally programmable over a range of 10 to 16mA lamps. in 1mA steps to allow the inverter to properly match to a wide array of LCD tended for panel assemblies where lamp panel lamp current specifications.

LXMG1643 series does not provide wide wire. range 'burst' mode dimming, rather dimming is provided by amplitude control are stable fixed-frequency operation, of the output current waveform, this limits the potential dim range to typically less and both open/shorted lamp protection than 5:1.

For applications not requiring wide potential transient noise particularly well suited for current

The modules convert DC voltage from required to ignite and operate CCFL

The LXMG1644-12-61 inverter is inpairs share close proximity with one LXMG1644 modules unlike the another and a common return (low side)

> Other benefits of this new topology secondary-side strike-voltage regulation with fault timeout.

IMPORTANT: For the most current data and a panel to inverter cross reference, consult MICROSEMI's website: http://www.microsemi.com

Control Analog Current Amplitude Dimming Method

Output Open/Short-Circuit Protection and Timeout

KEY FEATURES

Externally Programmable

Maximum Output Current Easy to Use Brightness

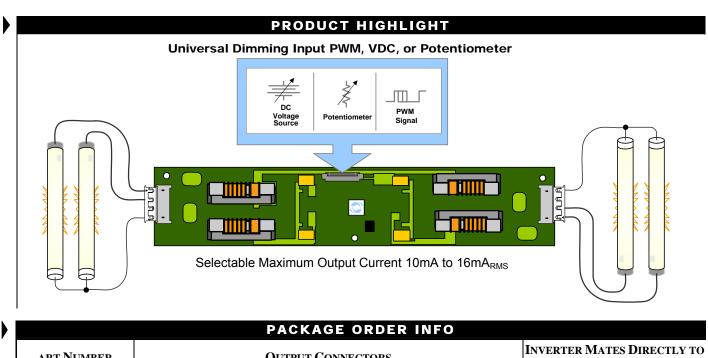
- **Fixed Frequency Operation**
- Rated From -20 to 70°C UL 60950 E175910.
- **RoHS** Compliant

APPLICATIONS

- High Brightness Displays
- **Desktop Displays**
- Industrial Display Controls

BENEFITS

- Compact, Low Profile Design
- Programmable output current allows inverter to mate with a wide variety of LCD panel's specifications



ART NUMBER	OUTPUT CONNECTORS	INVERTER MATES DIRECTLY TO PANEL CONNECTORS
LXMG1644-12-61	Two JST SM04(4.0)B-BHS-1-TB(LF)(SN) or Yeon Ho 20015WR-07A00	JST BHR-04VS-1

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ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Input Signal Voltage (V _{IN1}) Input Power	
Output Voltage, no load	
Output Current (each output)	
Output Power (each output)	6.0W
Input Signal Voltage (SLEEP Input)	-0.3V to V _{IN1}
Input Signal Voltage (BRITE)	
Ambient Operating Temperature, zero airflow	20°C to 70°C
Operating Relative Humidity, non-condensing	≤90%
Storage Temperature Range	

Note 1: Exceeding these ratings could cause damage to the device. All voltages are with respect to Ground. Currents are positive into, negative out of specified terminal.

RECOMMENDED OPERATING CONDITIONS (R.C.)

This module has been designed to operate over a wide range of input and output conditions. However, best efficiency and performance will be obtained if the module is operated under the condition listed in the 'R.C.' column. Min. and Max. columns indicate values beyond which the inverter, although operational, will not function optimally.

Parameter	Symbol	Recommen	Units		
raiameter	Symbol	Min	R.C.	Max	Units
Input Supply Voltage Range (Fully Regulated Lamp Current)	V _{IN1}	10.8	12	13.2	V
Input Supply Voltage Range (Functional)		10.2	12	13.8	
Output Power (each lamp)	Po		5.0	6.0*	W
Linear BRITE Control Input Voltage Range ¹	VBRT_ADJ	0.65 to 0.9		2.0	V
Lamp Operating Voltage	VLAMP	530	625	720	V _{RMS}
Lamp Current (Each pair, Full Brightness)	IOLAMP	10		16	mA _{RMS}
Operating Ambient Temperature Range	T _A	-20		70	°C

*Total output power must not exceed 12W per lamp pair. Higher voltage lamps may require the maximum output current to be set lower 16mA

¹ The minimum V_{BRT ADJ} voltage depends on the panel characteristics, depending on the panel it can vary from 0.65V to 0.9V

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the recommended operating condition and ambient temperature of 25° C except where otherwise noted.

Baramatar	Symbol Test Conditions		LXMG1644-12-61			Units	
Parameter	Symbol		Min	Тур	Max	Units	
OUTPUT PIN CHARACTERISTICS							
Full Bright Lamp Current (two lamps)	I _{L(MAX)}	$V_{BRT_ADJ} \ge 2.0V_{DC}, \overline{SLEEP} \ge 2.0V, V_{IN1} = 12V_{DC}$ $I_{SET1} = Ground, I_{SET2} = Ground$	9	10	11	mA _{RMS}	
Full Bright Lamp Current (two lamps)	I _{L(MAX)}	$V_{BRT_ADJ} \ge 2.0V_{DC}, \overline{SLEEP} \ge 2.0V, V_{IN1} = 12V_{DC}$ $I_{SET1} = Ground, I_{SET2} = Open$	10.8	12	13	mA _{RMS}	
Full Bright Lamp Current (two lamps)	I _{L(MAX)}	$V_{BRT_ADJ} \ge 2.0V_{DC}$, $\overline{SLEEP} \ge 2.0V$, $V_{IN1} = 12V_{DC}$ $I_{SET1} = Open$, $I_{SET2} = Ground$	12.8	14	15	mA _{RMS}	
Full Bright Lamp Current (two lamps)	I _{L(MAX)}	$V_{BRT_ADJ} \ge 2.0V_{DC}$, $\overline{SLEEP} \ge 2.0V$, $V_{IN1} = 12V_{DC}$ $I_{SET1} = Open$, $I_{SET2} = Open$	14.7	16	17	mA _{RMS}	
Output Current pair of Lamps to pair of Lamps Deviation	I _{LL%DEV}	$V_{BRT_ADJ} \ge 2.0V_{DC}$, $\overline{SLEEP} \ge 2.0V$, $V_{IN1} = 12V_{DC}$ $I_{SET1} = Open$, $I_{SET2} = Open$		3	10	%	
Min. Average Lamp Current (each output)	I _{L(MIN)}	$V_{BRT_{ADJ}} \le 0.5V_{DC}$, SLEEP $\ge 2.0V$, $V_{IN1} = 12V_{DC}$ I _{SET1} = I _{SET2} = Ground		5.5²		mA _{RMS}	
Lamp Start Voltage	V _{LS}	-20°C < T _A < 70°C, V _{IN1} > 10.8V _{DC}	1500	1650		V _{RMS}	
Operating Frequency	fo	$V_{BRT_{ADJ}}$ = 2.5 V_{DC} , SLEEP \geq 2.0V, V_{IN1} = 12V	69	72	75	kHz	

² The inverter is capable of a lower output current than may be recommended by the panel manufacturer. It is the user's responsibility to set the minimum brightness (BRITE) input at or above the panel specification for minimum current.



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		Parameter		Symbol	Test Conditions	LXMG1644-12-61			Units
		Parameter		Symbol	Test Conditions	Min	Тур	Max	Units
•	BRITE INP	UT			1				1
	Input Curre	ent		I _{BRT}	V _{BRT_ADJ} = 0V _{DC} V _{BRT_ADJ} = 3V _{DC}		-300 50		μA _{DC} μA _{DC}
	Minimum Ir	nput for Max. La	amp Current	V _{BRT_ADJ}	I _{O(LAMP)} = Maximum Lamp Current		2.0	2.05	VDC
	Minimum Ir	- nput for Min. La	mp Current	VBRT ADJ	I _{O(LAMP)} = Minimum Lamp Current	0.65*			V _{DC}
•	SLEEP INPUT						1		
	RUN Mode	•		$V_{\overline{\text{SLEEP}}}$		2.0		V _{IN1}	V _{DC}
	SLEEP Mo	de		V		-0.3		0.8	V _{DC}
•	SET _{1,2} INPUT			l	1				
	SET _{1,2} Low	/ Threshold		VL				0.4	V
	Input Curre	ent		I _{SET}	V _{SET} ≤ 0.4V		-300		μA
•	POWER C	HARACTERIS	TICS		I				
	Sleep Curr	ent		I _{IN(MIN)}	$V_{IN1} = 12V_{DC}, \overline{SLEEP} \le 0.8V$	0.0	10	30	μA _{DC}
	Run Currer	Run Current		I _{RUN}	V_{IN1} = 12V _{DC} , SLEEP \geq 2.0V, I _{SET1} = Open I _{SET2} = Ground, V _{LAMP} = 625V _{RMS}		1750		mA _{DC}
	Efficiency			$V_{IN1} = 12V_{DC}, \overline{SLEEP} \ge 2.0V, I_{SET1} = Open$					
	Emolonoy			η	$I_{\text{SET2}} = \text{Ground}, V_{\text{LAMP}} = 625V_{\text{RMS}}$		85		%
	* The Inverte			rrent than ma	I_{SET2} = Ground, V_{LAMP} = 625 V_{RMS} y be recommended by the panel manufacturer. It is the u			the minim	
	* The Inverte			rrent than ma tion for minim	I_{SET2} = Ground, V_{LAMP} = 625 V_{RMS}			the minim	
	* The Inverte			rrent than ma tion for minim	I_{SET2} = Ground, V _{LAMP} = 625V _{RMS} y be recommended by the panel manufacturer. It is the u num current. This is likely greater than the 0.65V minimum			the minim	
	* The Inverte (BRITE) inpu	t at or above the PIN	panel specifica	rrent than ma tion for minim FUNC	I_{SET2} = Ground, V_{LAMP} = 625 V_{RMS} y be recommended by the panel manufacturer. It is the u num current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION	n input.	bility to set		 um brigh
С	* The Inverte (BRITE) inpu	t at or above the PIN	panel specifica Mates with	rrent than ma tion for minim FUNC 51021-120	I _{SET2} = Ground, V _{LAMP} = 625V _{RMS} by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION	n input.	bility to set		 um brigh
с С	* The Inverte (BRITE) inpu CONN CONN	PIN 53261-1271)	panel specifica Mates with Main Inpu	rrent than ma tion for minim FUNC 51021-120	$I_{SET2} = Ground, V_{LAMP} = 625V_{RMS}$ by be recommended by the panel manufacturer. It is the unand current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION 00 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{IN1} \leq 13.2V$)	n input.	bility to set		 um brigh
с С	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3	PIN 53261-1271) V _{IN1}	panel specifica Mates with Main Inpu Power Su	rrent than ma tion for minim FUNC 51021-120 It Power S pply Retur	$I_{SET2} = Ground, V_{LAMP} = 625V_{RMS}$ by be recommended by the panel manufacturer. It is the under current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION D0 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{IN1} \leq 13.2V$) The second se	n input.	bility to set		 um brigh
с С	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6	PIN 53261-1271) V _{IN1} GND	panel specifica Mates with Main Inpu Power Su	FUNC 51021-120 tt Power S pply Retur gnal Groun	$I_{SET2} = Ground, V_{LAMP} = 625V_{RMS}$ by be recommended by the panel manufacturer. It is the under current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION D0 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{IN1} \leq 13.2V$) The second se	n input.	bility to set		 um brigh
с С	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7	The second secon	Mates with Main Inpu Power Su Analog Si No Conne	FUNC 51021-120 tt Power S pply Retur gnal Groun	$I_{SET2} = Ground, V_{LAMP} = 625V_{RMS}$ by be recommended by the panel manufacturer. It is the under current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION D0 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{IN1} \leq 13.2V$) The second se	(9508G input	bility to set		 um brigh
с С	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7 CN1-8	Pin 53261-1271) V _{IN1} GND AGND NC	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (FUNC 51021-120 tr Power S pply Retur gnal Groun ect Control. (0	$I_{SET2} = Ground, V_{LAMP} = 625V_{RMS}$ by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION $DESCRIPTION$ 00 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{IN1} \leq 13.2V$) m nd	* input. (9508G inpu = ON	bility to set		 um brigh
C	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7 CN1-8 CN1-9	The second secon	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (Brightnes	FUNC 51021-120 the Power S pply Return gnal Ground ect Control. (0) s Control (1)	$I_{\text{SET2}} = \text{Ground, } V_{\text{LAMP}} = 625 V_{\text{RMS}}$ by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION 00 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{\text{IN1}} \leq 13.2$ V) The modest statement of the second statement of th	sinput. (9508G inpu = ON o current.	ut cable	assembl	 um brigh
	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7 CN1-8 CN1-9 CN1-10	The second secon	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (Brightnes SET ₁ MSE	FUNC 51021-120 the Power S pply Return gnal Groun ect Control. (0 5 Control (3 Connecti	$I_{\text{SET2}} = \text{Ground}, V_{\text{LAMP}} = 625V_{\text{RMS}}$ by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION $Description$ $D0 \text{ housing}, 50079-8100 \text{ pins}. \text{ Mates with LX}$ $upply (10.8V \le V_{\text{IN1}} \le 13.2V)$ m $N < \overline{\text{SLEEP}} < 0.8 = \text{OFF}, \overline{\text{SLEEP}} >= 2.0V = 0.65V \text{ to } 2.0V). 2.0V_{\text{DC}}$ gives maximum lamp	e ON current.	ut cable	assembl	 um brigh
	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7 CN1-8 CN1-9 CN1-10 CN1-10 CN1-11 CN1-12	Tin tar or above the PIN 53261-1271) VIN1 GND AGND AGND NC SLEEP BRITE SET1 SET2	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (Brightnes SET ₁ MSE SET ₂ LSE	FUNC 51021-120 t Power S pply Retur gnal Groun ect Control. (0 s Control (3 Connecti 3 Connect	$I_{SET2} = Ground, V_{LAMP} = 625V_{RMS}$ by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION $DESCRIPTION$ $D0 \text{ housing, } 50079-8100 \text{ pins. Mates with LX}$ $upply (10.8V \le V_{IN1} \le 13.2V)$ The second	e ON current.	ut cable	assembl	 um brigh
	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7 CN1-8 CN1-9 CN1-10 CN1-10 CN1-11 CN1-12	Tin tar or above the PIN 53261-1271) VIN1 GND AGND AGND NC SLEEP BRITE SET1 SET2	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (Brightnes SET ₁ MSE SET ₂ LSE D)B-BHS-1-1 High volta	FUNC 51021-120 51021-120 tt Power S pply Retur gnal Groun ect Control. (0 s Control. (0 s Connecti 3 Connecti 5 Connect	I _{SET2} = Ground, V _{LAMP} = $625V_{RMS}$ by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION 00 housing, 50079-8100 pins. Mates with LX upply (10.8V $\leq V_{IN1} \leq 13.2V$) m nd V $\leq \overline{SLEEP} < 0.8 = OFF$, $\overline{SLEEP} >= 2.0V = 1000$ (0.65V to 2.0V). 2.0V _{DC} gives maximum lamp ing this pin to ground decreases the output co ing this pin to ground decreases the output co ing this pin to ground decreases the output co) or Yeon Ho 20015WR-07A00) ction to high Side of lamp. Connect to lamp t	 Second state Secon	Table 1)	assembl	y
с С С	* The Inverte (BRITE) inpu CONN N1 (Molex N1-1,2,3 N1-4,5,6 CN1-7 CN1-8 CN1-9 CN1-8 CN1-9 CN1-10 CN1-11 CN1-12 N2, CN3 (A	PIN 53261-1271) VIN1 GND AGND NC SLEEP BRITE SET1 SET2 JST SM04(4.0)	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (Brightness SET ₁ MSE SET ₂ LSE D)B-BHS-1-1 High volta DO NOT High volta	FUNC 51021-120 51021-120 tt Power S pply Retur gnal Groun ect Control. (0 3 Connecti 3 Connecti 5 Connect FB(LF)(SN age connect to	I _{SET2} = Ground, V _{LAMP} = 625V _{RMS} by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION 00 housing, 50079-8100 pins. Mates with LX upply (10.8V ≤ V _{IN1} ≤ 13.2V) rn nd $V < \overline{SLEEP} < 0.8 = OFF$, $\overline{SLEEP} >= 2.0V = 0.65V$ to 2.0V). 2.0V _{DC} gives maximum lamp ing this pin to ground decreases the output control to ground decreases the output control to recease the output control to high Side of lamp. Connect to lamp to Ground. ction to high Side of lamp. Connect to lamp to the formula of the formula	e ON current. urrent (see cerminal with	Table 1) Table 1)	assembl	y ength.
	* The Inverte (BRITE) input CONN N1 (Molex CN1-1,2,3 CN1-4,5,6 CN1-7 CN1-8 CN1-9 CN1-10 CN1-10 CN1-11 CN1-12 N2, CN3 (CN2,3-1	PIN 53261-1271) VIN1 GND AGND NC SLEEP BRITE SET1 SET2 JST SM04(4.0 VHI1	Mates with Main Inpu Power Su Analog Si No Conne ON/OFF (Brightness SET ₁ MSE SET ₂ LSE D)B-BHS-1-1 High volta DO NOT High volta	FUNC 51021-120 51021-120 tt Power S pply Retur gnal Groun ect Control. (0 3 Connection 3 Connection 5 Connection 16(LF)(SN age connect to age connect to age connect to	I _{SET2} = Ground, V _{LAMP} = 625V _{RMS} by be recommended by the panel manufacturer. It is the unum current. This is likely greater than the 0.65V minimum TIONAL PIN DESCRIPTION DESCRIPTION 00 housing, 50079-8100 pins. Mates with LX upply (10.8V ≤ V _{IN1} ≤ 13.2V) rn nd $V < \overline{SLEEP} < 0.8 = OFF$, $\overline{SLEEP} >= 2.0V = 0.65V$ to 2.0V). 2.0V _{DC} gives maximum lamp ing this pin to ground decreases the output control to ground decreases the output control to recease the output control to high Side of lamp. Connect to lamp to Ground. ction to high Side of lamp. Connect to lamp to the formula of the formula	e ON current. urrent (see cerminal with	Table 1) Table 1)	assembl	y ength.

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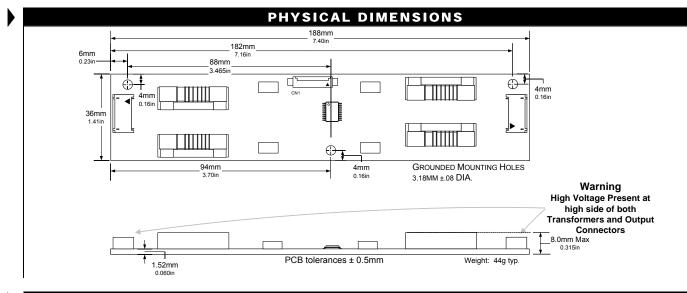
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TABLE 1

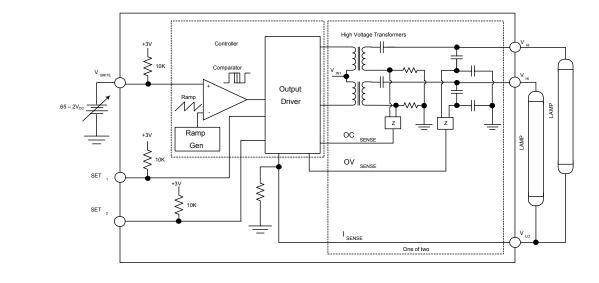
OUTPUT CURRENT SETTINGS (TWO LAMPS)

SET₁ (Pin 11)	SET ₂ (Pin 12)	Nominal Output Current
Open*	Open*	16.0mA
Open*	Ground	14.0mA
Ground	Open*	12.0mA
Ground	Ground	10.0mA

* If driven by a logic signal it should be open collector or open drain only, not a voltage source.



SIMPLIFIED BLOCK DIAGRAM



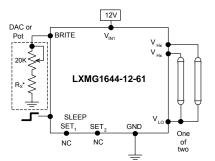


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TYPICAL APPLICATION



 * Set Rx from 2.7K to 3.9K depending on panel minimum lamp current requirements

Figure 1 – Brightness Control (Output current set to maximum)

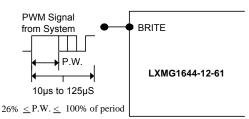
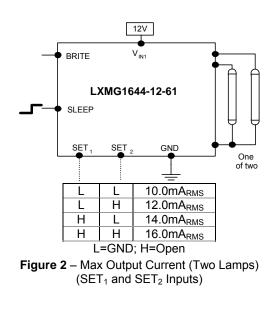


Figure 1A - PWM Brightness Control



- The brightness control may be a voltage output DAC or other voltage source, a digital pot or 20K manual pot. The inverter contains an internal 10K pull-up to 3V to bias the pot, add a 1.8K to 3.9K resistor to set the lower threshold voltage. A 3.3V Logic Level PWM signal from a microcontroller may also be used as shown in Figure 1A.
- If you need to turn the inverter ON/OFF remotely, connect to TTL logic signal to the SLEEP input.
- Connect V_{HI} to high voltage wire from the lamp. Connect V_{LO} to the low voltage wire (wire with thinner insulation). Never connect V_{LO} to circuit ground as this will defeat lamp current regulation. If both lamp wires have heavy high voltage insulation, connect the longest wire to V_{LO}. This wire is typically white.
- Use the SET₁ and SET₂ (see Figure 2) inputs to select the desired maximum output current. Using these two pins in combination allows the inverter to match a wide variety of panels from different manufactures. Generally the best lamp lifetime correlates with driving the CCFL at the manufactures nominal current setting. However the SET₁ and SET₂ inputs allow the user the flexibility to adjust the current to the maximum allowable output current to increase panel brightness at the expense of some reduced lamp life.
- Although the SET pins are designed such that just leaving them open or grounding them is all that is needed to set the output current, they can also be actively set. Using a open collector or open drain logic signal will allow you to reduce the lamp current for situations where greater dim range is required, as an example in nighttime situations. In conjunction with a light sensor or other timer the panel could be set to higher brightness (maximum output current) for daytime illumination and lower brightness (minimum or typical output current) at nighttime. Since the dim ratio is a factor of both the burst duty cycle and the peak output current, using this technique the effective dim ratio can be increased greater than the burst duty cycle alone. Conversely the SET inputs could be used to overdrive the lamp temporarily to facilitate faster lamp warm up at initial lamp turn on. Of course any possible degradation on lamp life from such practices is the users responsibility since not all lamps are designed to be overdriven.
- The inverter has a built in fault timeout function. If the output return is open (lamp disconnected or broken) or shorted the inverter will attempt to strike the lamp for several seconds. After about a second without success the inverter will shutdown. In order to restart the inverter it is necessary to toggle the sleep input or cycle the V_{IN1} input supply. In the timeout shutdown mode input drain current will be about 8mA.

APPLICATION



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NOTES

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