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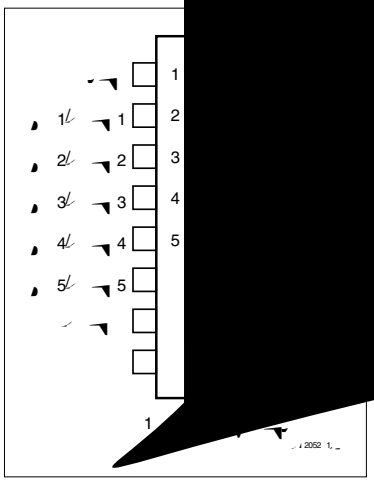


			communications input/output
	EED segment 5/ program 5 input	$PROG_6$	Program 6 input
CP	Control port	REF	Voltage reference output
		V_{CC}	Supply voltage

This open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the

F D G

The bq2052 determines battery capacity by monitoring the amount of charge removed from a primary battery. The bq2052 measures discharge currents and battery voltage, monitors the battery for the low battery-voltage thresholds, and compensates available capacity for temperature and discharge rate. The bq2052 measures capacity by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground.

Figure 1 shows a typical battery pack application of the bq2052 using the LED display capability as a charge-state indicator. The bq2052 displays capacity with two, four, or five LEDs using the programmed full count (PFC) as the battery's "full" reference. The bq2052 has a push-button input for momentarily enabling the LED display.

F

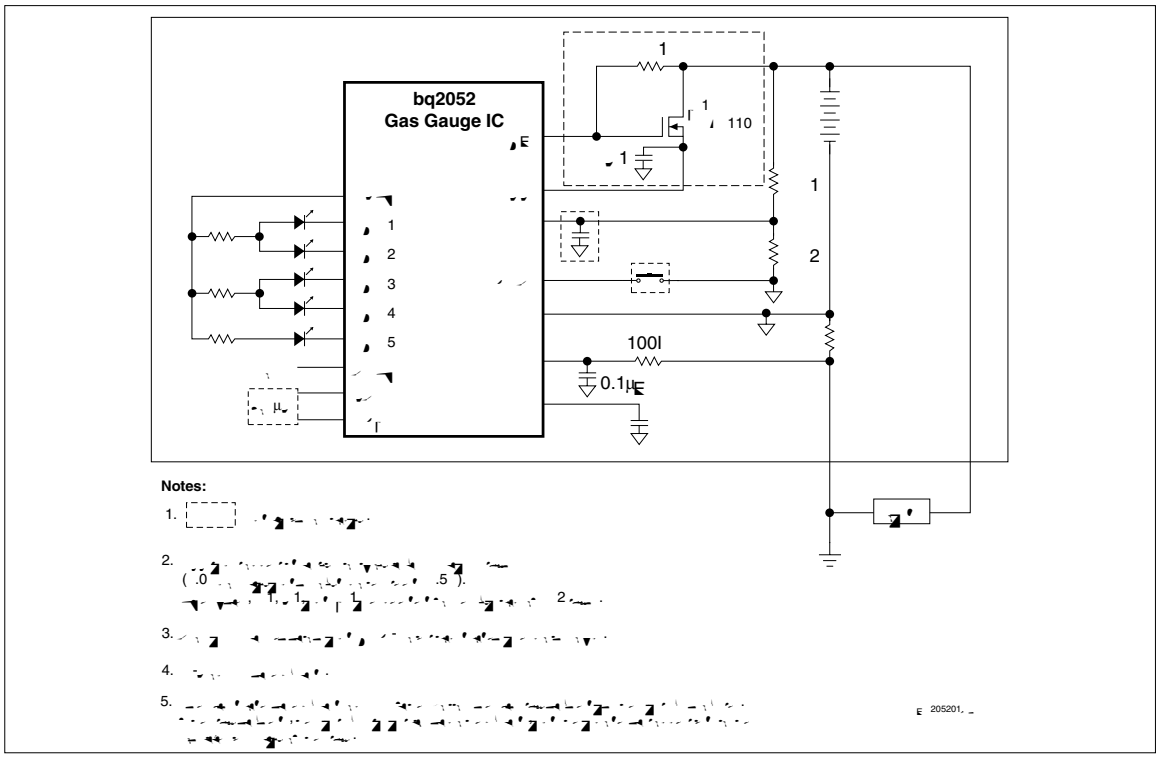
The bq2052 uses a voltage-to-frequency converter (VFC) for discharge measurement and an analog-to-digital converter (ADC) for battery voltage measurement.

D C

The VFC measures the discharge flow of the battery by monitoring a small value sense resistor between the SR pin and V_{SS} as shown in Figure 1. The bq2052 detects "discharge" activity when the potential at the SR input, V_{SRO}, is positive. The bq2052 integrates the signal over time using an internal counter. The fundamental rate of the counter is 3.125µVh. The VFC measures signals up to 0.5V in magnitude.

D F

The bq2052 has a digital filter to eliminate discharge counting below a set threshold. The minimum discharge threshold, V_{SRD}, for the bq2052 is 250µV.



F 1. A D F 5- F LED D

In conjunction with monitoring the SR input for discharge currents, the bq2052 monitors the battery potential through the SB pin. The voltage at the SB pin, V_{SB}, is developed through a high impedance resistor network connect across the battery. The bq2052 monitors the

2. 2052

G			G_3			
1	2	(FC)	H		L	
-	-	-	SCALE = 1/40	SCALE = 1/80	SCALE = 1/160	mVh/ count
H	H	48128	1203	602	301	mVh
H	Z	46080	1152	576	288	mVh
H	L	43264	1082	541	271	mVh
Z	H	39936	998	499	250	mVh
Z	Z	38400	960	480	240	mVh
Z	L	36096	902	451	226	mVh
L	H	31744	794	397	199	mVh
L	Z	28928	723	362	181	mVh
L	L	26112	653	327	164	mVh

G -G

The PFC register stores the user-specified battery full capacity. The 8-bit PFC registers stores the full capacity in mVh scaled as shown in Table 2.

The FNAC register stores the full capacity reference of the battery. It can be programmed to initialize to PFC or zero. The 8-bit FNAC register stores data scaled to the same units as PFC. The bq2052 does not update FNAC during the course of operation; therefore, if it is programmed to 0 on initialization, it must be written to full using the serial port.

er

The DCR is the main gas gauging register and contains the cumulative amount of discharge counted by the bq2052. The 16-bit register stores data scaled to the same units as PFC.

The CAC registers contain the current available capacity of the battery. The data stored in CAC represents the amount of remaining capacity of the battery compensated for rate and temperature use conditions. Tables 3, 4, and, 5 outline the options for typical efficiency compensation factors for lithium primary batteries. The bq2052 applies the efficiency factors to FNAC to derive CAC.

The bq2052 applies the compensation according to the formula:

$$CAC = [F_{CE} * FNAC] - DCR$$

Where F_{CE} is the calculated efficiency compensation factor, FNAC = Full Nominal Available Capacity and DCR = Discharge Count Register.

The bq2052 calculates an F_{CE} based on the battery discharge rate and temperature. The discharge rate portion of the F_{CE} compensation is a "peak hold" function; therefore, the bq2052 latches the highest discharge rate it has measured and uses the highest rate to calculate F_{CE} throughout the complete discharge cycle. The highest discharge rate measured by the bq2052 is stored in MRATE (address = 12h).

The bq2052 does not latch the temperature portion of an F_{CE} calculation. Therefore, CAC may increase or decrease during the course of a complete discharge cycle if a temperature shift causes a change in the calculated F_{CE} value.

2052

The bq2052 is programmed with the $PROG_{1–6}$ pins. During power-up or initialization, the bq2052 reads the state of these six three-level inputs and latches in the programmable configuration settings.

Programmed Full Count (PFC)

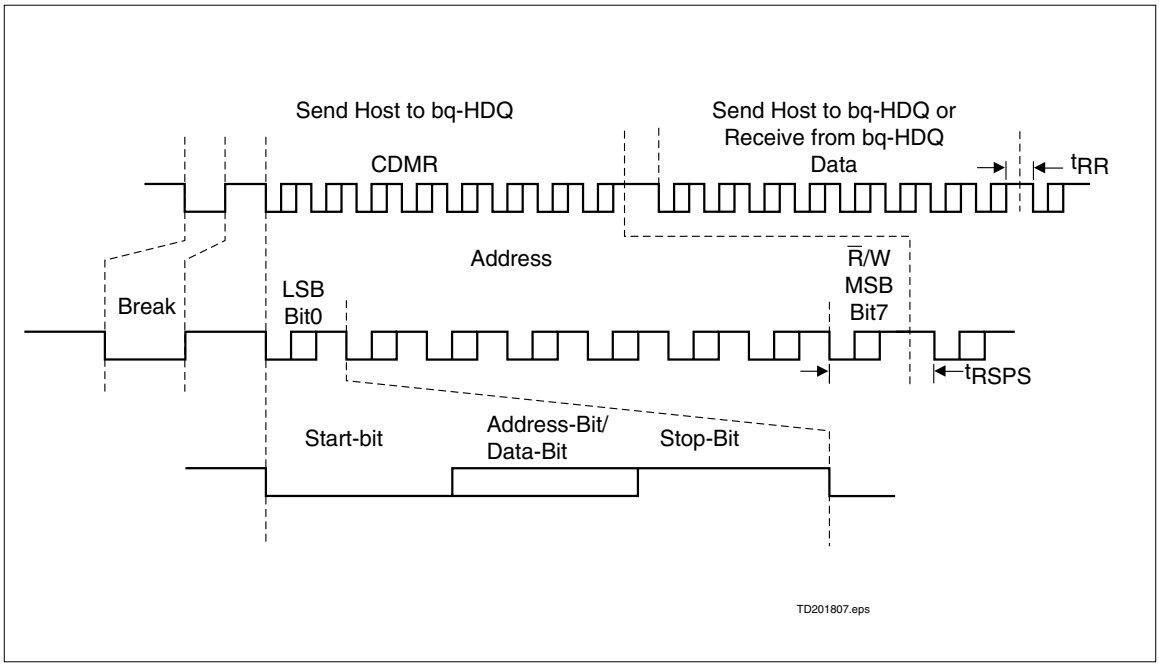
The battery's rated design capacity or Programmed Full Count (PFC) is programmed with the $PROG_1$–$PROG_3$ pins as shown in Table 2, and represents the battery's full reference.

The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

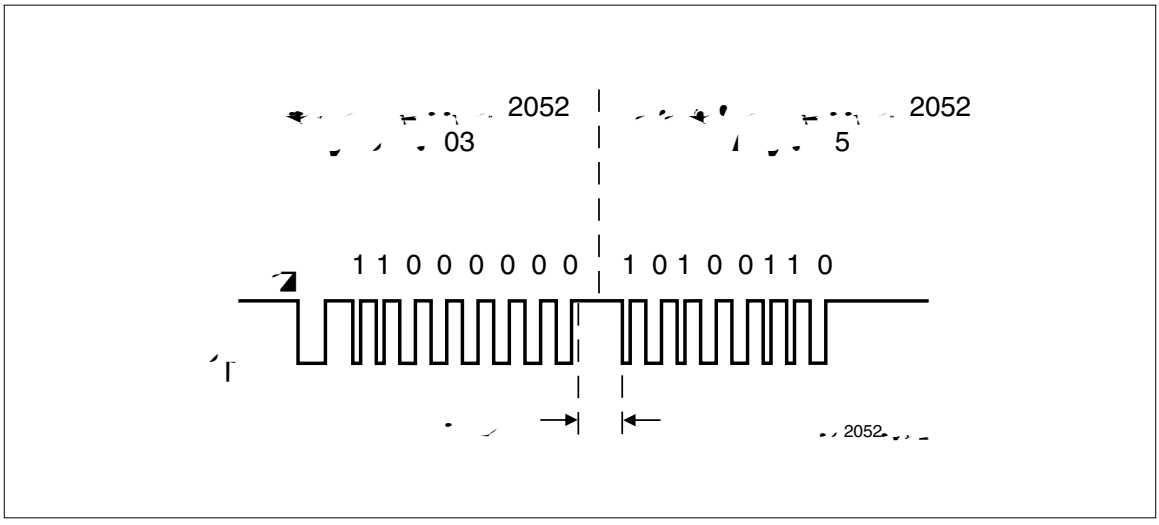
Battery capacity (mAh) * sense resistor (Ω) = PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference. The bq2052 stores the selected PFC in the PFC register (address = 10h).

Name	Description	Address	R/W	7	6	5	4	3	2	1	0
CMDWD	Command word	00h	W	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
FLGS1	Primary status flags	01h	R	INIT	RSVD	RSVD	CPIN	RSVD	RSVD	EDV1	EDVF
TEMP	Temperature (°C)	02h	R	TEMP7	TEMP6	TEMP5	TEMP4	TEMP3	TEMP2	TEMP1	TEMP0
NAC	Nominal available capacity	03h	R/W	NAC7	NAC6	NAC5	NAC4	NAC3	NAC2	NAC1	NAC0
BATID	Battery identification	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
VSRL	Current scale (Low)	05h	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
VSRH	Current scale (High)	06h	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
PPD	Program pin pull-down	07h	R	RSVD	RSVD	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up	08h	R	RSVD	RSVD	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
VSB	Battery voltage register	0bh	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	End-of-discharge threshold select register	0ch	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
RCAC	Relative compensated capacity	0dh	R	RSVD	RCAC6	RCAC5	RCAC4	RCAC3	RCAC2	RCAC1	RCAC0
CACL	Compensated avail-										



F 4. 2052 C F E F



F 5. C F 2052

C [illegible] 2052

The bq2052 includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2052 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2052 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2052. The command directs the bq2052 to either store the next eight bthetof42htot309.4(pto)(thereiv -1.1to)(t0.2(rto)(t.4(pto)(the 25.94(pto)(tspecifi -1.1to)(tr)]T1to)(t0ds)-551hto),287(to)-236822.4-287.3682

F (FLG 1)

The FLGS1 register (address = 01h) contains the primary bq2052 flags.

The ***initialized*** flag (INIT) is asserted to a 1 or 0 whenever the bq2052 is initialized either by the application of Vcc or by a serial port command. INIT = 1 signifies that the device has been reset with FNAC set to PFC. INIT = 0 signifies that the battery has been reset with FNAC = 0.

The INIT location is:

FLG 1 B							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
INIT	-	-	-	-	-	-	-

where INIT is:

0 The bq2052 initialized with FNAC = 0.

1 The bq2052 initialized with FNAC = PFC.

The CPIN but reflects the state of the CP output. If set, the CP output is high impedance. If cleared, the CP output is asserted low. The CP output is an open drain output and requires an external pull-up register.

The CPIN location is

FLG 1 B							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	CPIN	-	-	-	-

Where CPIN is:

0 CP is low

1 CP is high impedance

The bq2052 sets the ***first end-of-discharge warning*** flag (EDV1) when the battery voltage VSB is less than the EDV1 threshold VTS. The flag warns the user that the battery is almost empty. The bq2052 modulates the first segment pin, SEG1, at a 4Hz rate if the 4 or 5 segment display mode is enabled and EDV1 is asserted.

The EDV1 threshold has a default value of 0.76V but can be adjusted by writing the VTS register .

The EDV1 location is

FLG 1 B							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 $V_{SB} \geq V_{TS}$

1 $V_{SB} < V_{TS}$

The bq2052 sets the ***final end-of-discharge warning*** flag (EDVF) when VSB is less than the EDVF threshold. The EDVF threshold is set 100mV below the EDV1 threshold. The EDVF flag is used to warn the system or user that battery power is at a failure condition. The bq2052 turns all segment drivers off upon EDVF detection.

The EDVF location is:

FLG 1 B							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 $V_{SB} \geq (V_{TS} - 100mV)$

1 $V_{SB} < (V_{TS} - 100mV)$

F (E)

The 8-bit TEMP register (address=02h) contains the battery temperature in degrees C. The bq2052 contains an internal temperature sensor. The temperature is used to set discharge efficiency factors. The temperature register contents are store in 2's complement form and represent the temperature ± 5°C.

F A C (AC)

The NAC register contains the uncompensated remaining capacity of the battery. The bq2052 determines NAC as

$$NAC = FNAC - DCR$$

B I (BA ID)

The 8-bit BATID register (address=04h) is a general purpose memory register that can be used to uniquely identify a battery pack. The bq2052 maintains the BATID contents as long as VRBI is greater than 2V. The contents of this register have no effect on the operation of the bq2052.

C (L/ H)

The VSRH high-byte register and the VSRL low-byte register are used to calculate the average signal across the SR and VSS pins. This register pair is updated every 5.625 seconds. VSRH and VSRL form a 16-bit value representing the average current over this time. The battery pack current can be calculated by:

$$|I(mA)| = \frac{(VSRH * 256 + VSRL)}{(Rs)}$$

where

R_S = sense resistor value in Ω.

VSRH = high-byte value of current scale

VSRL = low-byte value of current scale

-D (D)

The PPD register (address = 07h) contains the pull-down programming pin information for the bq2052. The program pins, $PROG_{1–6}$, have a corresponding PPD register location, $PPD_{1–6}$. A given location is set if the bq2052 detects a pull-down resistor on its corresponding segment driver. For example, if $PROG_1$ and $PROG_4$ have pull-down resistors, the contents of PPD are xx001001.

- ( )

The PPU register (address = 08h) contains the pull-up programming pin information for the bq2052. The segment drivers, $PROG_{1–6}$, have a corresponding PPU register location, $PPU_{1–6}$. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if $PROG_3$ and $PROG_5$ have pull-up resistors, the contents of PPU are xx010100.

B (. B)

The battery voltage register (address = 0bh) stored the voltage detected on the SB pin. The bq2052 updates the VSB register approximately once per second with the present value of the battery voltage.

$$V_{SB} = 1.2V * \left(\frac{VSB}{256}\right)$$

(.)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register. The VTS register sets the EDV1 trip point. EDVF is set 100mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.66V.

$$EDV1 = 1.2V * \left(\frac{VTS}{256}\right).$$

CAC (CAC)

The RCAC register (address = 0dh) provides the relative battery state-of-charge by dividing CAC by FNAC. RCAC varies from 0 to 7dh representing relative state-of-charge from 0 to 125%.

A - C (CAC)

The CAC registers (address = 0eh–0fh) contain the available capacity compensated for discharge rate and temperature. The CAC value is also used in calculating the LED display pattern relative to PFC.

F C (FC)

The PFC register (address = 10h) contains the user selected programmed full count (PFC) setting.

A - C (F AC)

The FNAC (address = 11h) contains the full capacity reference of the battery.

D (A A E)

The MAXRATE register (address = 12h) stores the highest discharge rate detected by the bq2052. The bq2052 uses the MAXRATE value to calculate the efficiency compensation factors.

(A E)

The RATE register (address = 13h) provides the current discharge rate of the battery.

C (DC H/DC L)

The DCRH high-byte register and the DCRL low-byte register are the main gas gauging registers for the bq2052. The DCR registers are incremented during discharge.

Writing to the DCR registers affects the available charge counts and, therefore, affects the bq2052 gas gauge operation.

D

The bq2052 can directly display remaining capacity information using low-power LEDs. The bq2052 uses the CAC value in relation to FNAC as the basis for the display activity. The bq2052 displays the battery's remaining capacity in either of three modes selected with program pin $PROG_5$. The display is activated using the $\overline{DISP}$ input. When $\overline{DISP}$ is connected to V_{CC}, the SEG outputs are OFF. When pulledaffec61.(Disc)11.led77.ii.ledN 2tWSEG

In incremental mode ($PROG_5$ = L), the battery charge state is displayed on pins SEG1–SEG4. The charge state condition indicated by each segment is shown in Table 7. Only the segment pin representing the present remaining capacity is ON (low); all other segments are OFF (high impedance). When $\overline{DISP}$ is pulled low, the display is active for 10s.

7. I F D
G_5 = L

EG	F C
SEG4	90 -100%
SEG3	50 - < 90%
SEG2	20 - < 50%
SEG1	< 20%
SEG1—BLINK	$V_{SB} < V_{EDV1}$

In binary mode (PROG5 = H), the battery charge state is displayed using only pins SEG1 and SEG2, with the remaining capacity indication defined as in Table 8. When $\overline{DISP}$ is pulled low, the display is active for 4s.

8. B D
G_5 = H

EG 1	EG 2	F C
ON	ON	70 -100%
ON	OFF	40 - < 70%
OFF	ON	10 - < 40%
OFF	OFF	< 10% or $V_{SB} < V_{EDVF}$

In bar graph mode ($PROG_5$ = Z), the battery charge state is displayed using pins SEG1 through SEG 5 according to Table 9. When $\overline{DISP}$ is pulled low, the display is active for 4s.

A micro-power source for the bq2052 can be inexpensively built using a FET and an external resistor as shown in Figure 1.

BI I

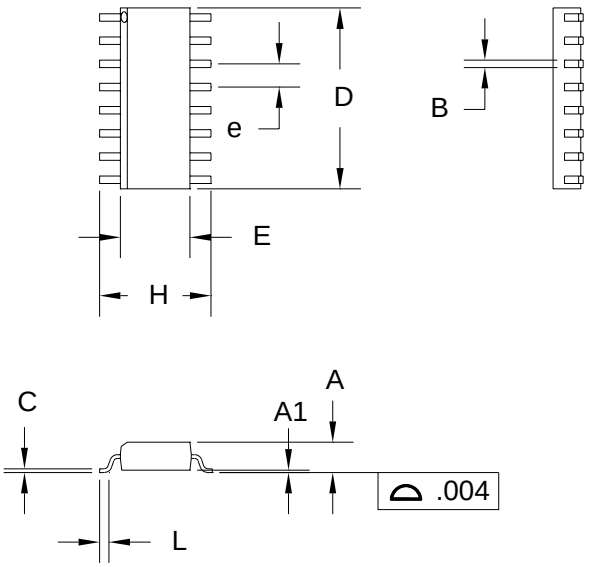
The RBI input pin should be used with a storage capacitor or external supply to provide backup potential to the internal bq2052 registers when V

C (A =)

t_{CYCH}	Cycle time, host to bq2052 (write)	190	-	-	µs	See note
t_{CYCB}	Cycle time, bq2052 to host (read)	190	205	250	µs	
t_{STRH}	Start hold, host to bq2052 (write)	5	-	-	ns	
t_{STRB}	Start hold, bq2052 to host (read)	32	-	-	µs	
t_{DSU}	Data setup	-	-	50	µs	
t_{DSUB}	Data setup	-	-	50	µs	
t_{DH}	Data hold	90	-	-	µs	
t_{DV}	Data valid	-	-	80	µs	
t_{SSU}	Stop setup	-	-	145	µs	
t_{SSUB}	Stop setup	-	-	145	µs	
t_{RSPS}	Response time, bq2052 to host	190	-	320	µs	
t_B	Break	190	-	-	µs	
t_{BR}	Break recovery	40	-	-	µs	

The open-drain HDQ pin should be pulled to at least V_{CC} by the host system for proper HDQ operation. HDQ may be left floating if the serial interface is not used.

16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

Ordering Information

bq2052

Temperature Range:
blank = Commercial (-20 to +70°C)

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2052 Gas Gauge IC

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ2052SN-A515	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ2052SN-A515G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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