

SBS 1.1-COMPLIANT GAS GAUGE ENABLED WITH IMPEDANCE TRACK™ TECHNOLOGY FOR USE WITH THE bq29312A

FEATURES

- Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries
- Better than 1% Error Over Lifetime of the Battery
- Instant Accuracy – No Learning Cycle Required
- Supports the Smart Battery Specification SBS V1.1
- Works With the TI bq29312A Analog Front-End (AFE) Protection IC to Provide Complete Pack Electronics Solution

- Lifetime Data Logging
- 38-Pin TSSOP (DBT)

APPLICATIONS

- Notebook PCs
- Medical and Test Equipment
- Portable Instrumentation

DESCRIPTION

The bq20z80 SBS-compliant gas gauge IC, incorporating patented Impedance Track™ technology, is designed for battery-pack or in-system installation. The bq20z80 measures and maintains an accurate record of available **External**

Components

- Based on a Powerful Low-Power RISC CPU Core With High-Performance Peripherals
- Integrated Field Programmable FLASH Memory Eliminates the Need for External Configuration Memory
- Measures Charge Flow Using a High-Resolution, 16-Bit Integrating Delta-Sigma Converter
 - Better Than 0.65 nVh of Resolution
 - Self-Calibrating
 - Offset Error Less Than 1 μ V
- Uses 16-Bit Delta-Sigma Converter for Accurate Voltage and Temperature Measurements
- Extensive Data Reporting Options For Improved System Interaction
- Optional Pulse Charging Feature for Improved Charge Times
- Drives 3-, 4- or 5-Segment LED Display for Remaining Capacity Indication
- Supports SHA-1 Authentication

bus. It is designed to work with the bq29312A analog front-end (AFE) protection IC to maximize functionality and safety, and minimize component count and cost in smart battery circuits.

The Impedance Track technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables remaining capacity to be calculated with discharge rate, temperature, and cell aging all accounted for during each stage of every cycle.

AVAILABLE OPTIONS

T _A	PACKAGE	
	38-PIN TSSOP (DBT) Tube	38-PIN TSSOP (DBT) Tape and Reel
-40°C to 85°C	bq20z80DBT-V102 ⁽¹⁾	bq20z80DBTR-V102 ⁽²⁾

- (1) A single tube quantity is 50 units.
 (2) A single reel quantity is 2000 units



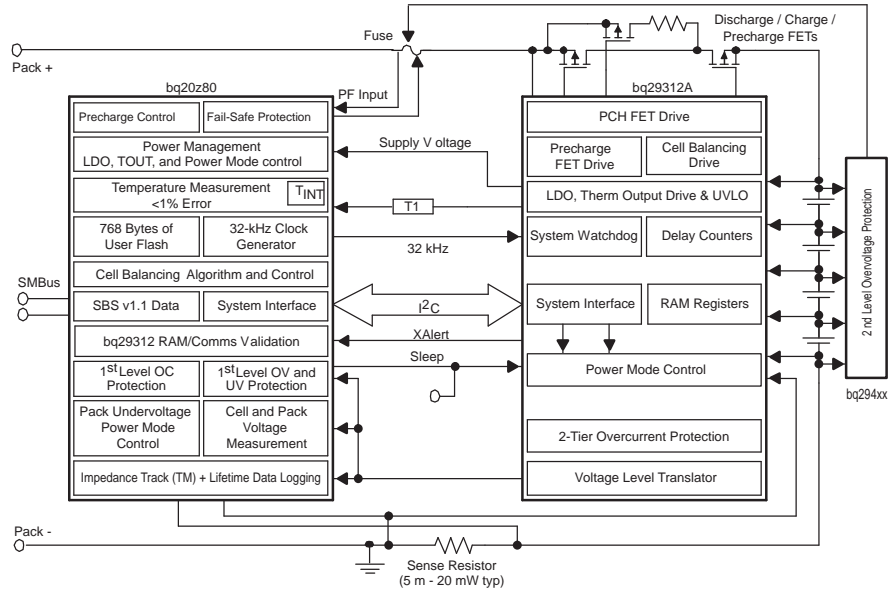
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Impedance Track is a trademark of Texas Instruments.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SYSTEM DIAGRAM



TSSOP (DBT) (TOP VIEW)

VIN	1	38	VSSD
TS1	2	37	NC
TS2	3	36	NC
PU	4	35	CLKOUT
PRES	5	34	XCK1 / VSSA
SCLK	6	33	XCK2 / ROSC
SAFE	7	32	FILT
VDDD	8	31	VDDA
RBI	9	30	VSSA
SDATA	10	29	VSSA
VSSD	11	28	SR1
SAFE	12	27	SR2
NC	13	26	MRST
NC	14	25	XALERT
SMBC	15	24	LED1
SMBD	16	23	LED2
DISP	17	22	LED3
PFIN	18	21	LED4
VSSD	19	20	LED5

NC - No internal connection

TERMINAL FUNCTIONS

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	VIN	I	Voltage measurement input from the AFE
2	TS1	I	1 st Thermistor voltage input connection to monitor temperature
3	TS2	I	2 nd Thermistor voltage input connection to monitor temperature
4	PU	O	Output to pull up the $\overline{\text{PRES}}$ pin for system detection
5	$\overline{\text{PRES}}$	I	Active low input to sense system insertion and typically requires additional ESD protection
6	SCLK	I/OD	Communication clock to the AFE
7	SAFE	O	Active high output to enforce additional level of safety protection; e.g., fuse blow. (Inverse of pin 12)
8	VDDD	P	Positive supply for digital circuitry and I/O pins
9	RBI	P	Backup power to the bq20z80 data registers during periods of low operating voltage. RBI accepts a storage capacitor or a battery input.
10	SDATA	I/O	Data transfer to and from the AFE
12	$\overline{\text{SAFE}}$	O	Active low output to enforce additional level of safety protection; e.g., fuse blow. (Inverse of pin 7)
13	NC	-	Not used— leave floating
14	NC	-	Not used— leave floating
15	SMBC	I/OD	SMBus clock open-drain bidirectional pin used to clock the data transfer to and from the bq20z80
16	SMBD	I/OD	SMBus data open-drain bidirectional pin used to transfer address and data to and from the bq20z80
17	$\overline{\text{DISP}}$	I	Display control for the LEDs. This pin is typically connected to bq29312A REG via a 100-k Ω resistor and a push-button switch to VSSD.
18	$\overline{\text{PFIN}}$	I	Active low input to detect secondary protector output status and allows the bq20z80 to report the status of the 2 nd level protection output
20	LED5	O	LED5 display segment that drives an external LED depending on the firmware configuration
21	LED4	O	LED4 display segment that drives an external LED depending on the firmware configuration
22	LED3	O	LED3 display segment that drives an external LED depending on the firmware configuration
23	LED2	O	LED2 display segment that drives an external LED depending on the firmware configuration
24	LED1	O	LED1 display segment that drives an external LED depending on the firmware configuration
25	XALERT	I	Input from bq29312A XALERT output.
26	MRST	I	Master reset input that forces the device into reset when held high
27	SR2	IA	Connections for a small-value sense resistor to monitor the battery charge- and discharge-current flow
28	SR1	IA	Co.alue the battery charge- and discharge-current
31	VDDA	P	Positive supply for analog circuitry
32	FILT	IA	Analog input to external filter components which are a 150-pF capacitor to V _{SSA} , in parj 1el 0 0 1 -8 Tf (display18.224 535.6 Tm /F2 -8 Tf (and)Tj 1 0 0 1 333.968 535.6 Tm /F2 -8 Tf (
36, 37	NC	-	Not used— leave floating
11, 19, 38	VSSD	P	Negative supply for digital circuitry
29, 30	VSSA	P	Negative supply for analog circuitry.

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain O = Output, OA = Analog output, P = Power

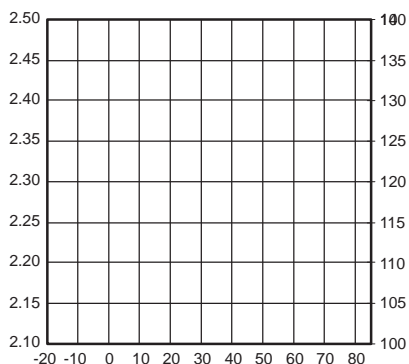
ABSOLUTE MAXIMUM RATINGS

ELECTRICAL CHARACTERISTICS

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$V_{DD} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IT-} Negative-going voltage input		2.1	2.3	2.5	V
V_{HYS} Power-on reset hysteresis		50	150	200	mV



CHARACTERISTICS

$V_{DD} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{(SR)}$ Input voltage range, $V_{(SR2)}$ and $V_{(SR1)}$	$V_{(SR)} = V_{(SR2)} - V_{(SR1)}$	-0.25		0.25	V
$V_{(SROS)}$ Input offset			1		μV
INL Integral nonlinearity error			0.004%	0.019%	

CHARACTERISTICS

$V_{DD} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(SP)}$ Start-up time ⁽¹⁾	0.5% frequency error		2	5	ms

(1) The frequency error is measured from the trimmed frequency of the internal system clock which is 128 oscillator frequency, nominally 4.194 MHz.

OSCILLATOR

$V_{DD} = 3\text{ V to }3.6\text{ V}$, $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(exo)}$ Frequency error from 32.768 kHz	ROSC = 100 k Ω	-2%	0.25%	2%	
	ROSC = 100 k Ω , $V_{DD} = 3.3\text{ V}$	-1%	0.25%	1%	
	XCK1 = 12-pF XTAL	-0.25%		0.25%	
$f_{(sxo)}$ Start-up time ⁽¹⁾	ROSC = 100 k Ω			250	μs
	XCK1 = 12-pF XTAL			200	ms

(1) The start-up time is defined as the time it takes for the oscillator output frequency to be within 1% of the specified frequency.

DATA FLASH MEMORY CHARACTERISTICS

$V_{DD} = 3\text{ V to }3.6\text{ V}$, $T_A = -$

REGISTER BACKUP

SMBus Timing Specifications

$V_{DD} = 3\text{ V}$ to 5 V , $T_{amb} = -40^{\circ}\text{C}$ to 85°C (unless otherwise specified)

PARAMETER		UNIT
f_{SMB}	Maximum frequency	kHz
f_{MAS}	Maximum clock frequency	kHz
t_{BUF}	Bus hold time after start and stop	ns
$t_{HD:STA}$	High-level time (initial start)	ns
$t_{SU:STA}$	Setup time (initial start)	ns
$t_{SU:STO}$	Setup time (stop)	ns
$t_{HD:DAT}$	High-level time (data)	ns
$t_{SU:DAT}$	Setup time (data)	ns
$t_{TIMEOUT}$	Timeout time	ms
t_{LOW}	Low-level time	ns
t_{HIGH}	High-level time	ns
$t_{LOW:SEXT}$	Low-level time (extend)	ms
$t_{LOW:MEXT}$	Low-level time (master extend)	ms
t_F	Fall time	ns
t_R	Clock/data rise time	ns

- (1) The bq20z80 times out when any clock low exceeds $t_{TIMEOUT}$.
- (2) $t_{HIGH:MAX}$ is minimum bus idle time. SMBC = 1 for $t > 50\ \mu\text{s}$ causes reset of any transaction involving the bq20z80 that is in progress.
- (3) $t_{LOW:SEXT}$ is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
- (4) $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

SMBus Timing Diagram



FEATURE SET

NOTE:

Primary (1st Level) Safety Features

Secondary (2nd Level) Safety Features

Charge Control Features

FEATURE SET (continued)

Gas Gauging

The bq20z80 uses the Impedance Track™ Technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than the coulomb counting method over the lifetime of the battery and there is no full charge discharge learning cycle required.

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note (SLUA364) for further details.

LED Display

The bq20z80 can drive 3-, 4-, or 5- segment LED display for remaining capacity indication.

LifeTime Data Logging Features

The bq20z80 offers a lifetime data logging array, where all important measurements are stored for warranty and analysis purposes. The data monitored includes:

- Lifetime maximum temperature
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average discharge current
- Lifetime maximum average discharge power
- Lifetime average temperature

Authentication

The bq20z80 supports authentication by the host using SHA-1.

Power Modes

The bq20z80 supports 3 different power modes to reduce power consumption:

- In Normal Mode, the bq20z80 performs measurements, calculations, protection decisions, data update in 1 second intervals. Between these intervals, the bq20z80 is in a reduced power stage.
- In Sleep Mode, the bq20z80 performs measurements, calculations, protection decisions, data update in adjustable time intervals. Between these intervals, the bq20z80 is in a reduced power stage.
- In Shutdown Mode the bq20z80 is completely disabled.

CONFIGURATION

Oscillator Function

The oscillator of the bq20z80 can be set up for internal or external operation. On power up, the bq20z80 automatically attempts to start the internal oscillator. If a 100-k Ω resistor is not connected to ROSC (pin 33), then it attempts to start the oscillator using an external 32.768-kHz crystal.

NOTE:

Install either the 100-k Ω ROSC resistor *or* the 12-pF, 32.768-kHz crystal. Do not install both.

FEATURE SET (continued)

The performance of the internal oscillator depends on the tolerance of the 100-k Ω resistor between RSOC (pin 33) and VSSA (pin 34). Choose a resistor with a tolerance of $\pm 0.1\%$, and 50-ppm or better temperature drift. Place this resistor as close as possible to the bq20z80. If a 12-pF crystal is used, place it as close as possible to the XCK1 (pin 34) and XCK2 (pin 33) pins. If not properly implemented, the PCB layout in this area can degrade oscillator performance.

System Present Operation

The bq20z80 pulls the PU pin high periodically (1 s). Connect this pin to the $\overline{\text{PRES}}$ pin of the bq20z80 via a resistor of approximately 5 k Ω . The bq20z80 measures the $\overline{\text{PRES}}$ input during the PU-active period to determine its state. If $\overline{\text{PRES}}$ input is pulled to ground by external system, the bq20z80 detects this as system present.

BATTERY PARAMETER MEASUREMENTS

The bq20z80 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage, and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SR1 and SR2 pins. The integrating ADC measures bipolar signals from -0.25 V to 0.25 V. The bq20z80 detects charge activity when $V_{\text{SR}} = V_{(\text{SR}1)} - V_{(\text{SR}2)}$ is positive and discharge activity when

Voltage

Current

Auto Calibration

Temperature

COMMUNICATIONS

SMBus On and Off State

Table 3. DATAFLASH VALUES (continued)

Class	Subclass ID	Subclass	Offset	Name	Data Type	Min Value	Max Value	Default Value	Units			
Configuration	64	Registers	0	Operation Cfg A	H2	0x0000	0xffff	0x0F29				
			2	Operation Cfg B	H2	0x0000	0xffff	0x6440				
			4	Permanent Fail Cfg	H2	0x0000	0xffff	0x0000				
			6	Non-Removable Cfg	H2	0x0000	0xffff	0x0000	hex			
LED Support	67	LED Cfg	0	LED Flash Rate	U2	0	65535	512	500µs			
			2	LED Blink Rate	U2	0	65535	1024	500µs			
			4	LED Delay	U2	1	65535	100	500µs			
			6	LED Hold Time	U1	0	255	4	s			
			7	CHG Flash Alarm	I1	-1	101	10	%			
			8	CHG Thresh 1	I1	-1	101	0	%			
			9	CHG Thresh 2	I1	-1	101	20	%			
			10	CHG Thresh 3	I1	-1	101	40	%			
			11	CHG Thresh 4	I1	-1	101	60	%			
			12	CHG Thresh 5	I1	-1	101	80	%			
			13	DSG Flash Alarm	I1	-1	101	10	%			
			14	DSG Thresh 1	I1	-1	101	0	%			
			15	DSG Thresh 2	I1	-1	101	20	%			
			16	DSG Thresh 3	I1	-1	101	40	%			
			17	DSG Thresh 4	I1	-1	101	60	%			
			18	DSG Thresh 5	I1	-1	101	60	%			
			Power	68	Power	0	Flash Update OK Voltage	U2	6000	20000	7500	mV
						2	Shutdown Voltage	U2	5000	20000	7000	mV
4	Shutdown Time	U1				0	60	10	Sec			
5	Charger Present	U2				0	23000	12000	mV			
7	Sleep Current	U2				0	100	10	mA			
9	Bus Low Time	U1				0	255	5	Sec			
10	Cal Inhibit Temp Low	I2				-400	1200	50	0.1°C			
12	Cal Inhibit Temp High	I2				-400	1200	450	0.1°C			
14	Sleep Voltage Time	U1				0	100	5	Sec			
15	Sleep Current Time	U1				0	255	20	Sec			
Gas Gauging	80	IT Cfg	0	Load Select	U1	0	255	3	num			
			1	Load Mode	U1	0	255	0	num			
			45	Term Voltage	I2	-32768	32767	12000	mV			
			60	User Rate-mA	I2	-9000	-2000	0	mA			
			62	User Rate-mW	I2	-14000	-3000	0	10mW			
			64	Reserve Cap-mAh	I2	0	9000	0	mAh			
			66	Reserve Cap-mWh	I2	0	14000	0	10mWh			
Gas Gauging	81	Current Thresholds	0	Dsg Current Threshold	U2	0	2000	100	mA			
			2	Chg Current Threshold	U2	0	2000	50	mA			
			4	Quit Current	U2	0	1000	10	mA			
			6	Dsg Relax Time	U1	0	255	1	Sec			
			7	Chg Relax Time	U1	0	255	60	Sec			





Firmware Version Changes

bq20z80-V101 to bq20z80-V102 Changes

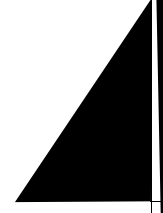
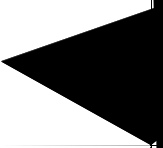
Table 4. CHANGE DETAILS

CHANGE	bq0z80-V102	bq20z80-V101	COMMENTS
Corrected to allow display to turn off when charging and button pushed.	LED display operates correctly during charging.	LED display would stay on until charging terminated after the button was pushed. Only occurs when LED display not configured to be always on during charging.	Correct operation of the LED display under all conditions
Allow negative LED thresholds to permit LED alarms to be disabled	Configuring negative LED alarm threshold disables LED alarm functionality.	Feature not available	Allow better customization
Allow zero values for ALARM and CHARGING LED blink rates to disable them	Configuring zero value for the LED blink rates disables them.	Feature not available	Allow better customization
Restore initialization of dodcharge in relaxed state so that the correct dodcharge value is used in capacity estimation	dodcharge initialized to the correct value	dodcharge value set to zero	Improved gauging accuracy with correct initialization of dodcharge value.
Only clear offset calibration flag when SMBus lines go high.	Prevents offset calibration occurring just because a safety condition occurs and then clears when the SMBus lines are low.	Offset calibration occurs multiple times if safety condition occurs when SMBus lines are low.	More appropriate period between offset calibrations when SMBus lines are low.
Change so that setting AFE Fail Limit to zero disables PF_AFE_C	Configurable option to allow disabling PF_AFE_C trigger	Feature not available.	Allow better customization
Enable LED display to turn off after charge termination and if SMBus lines are detected low and LEDs enabled during charging.	LED display turns off after charge termination.	LED display stays on when charging terminates after SMBus lines are detected low.	Correct operation of the LED display under all conditions
Set charge FET state immediately when entering sleep	Charge FET state set correctly, immediately after entering sleep	The CHG FET would not get set to the correct state for sleep until the first voltage measurement.	Quicker transition of FET to the correct state in sleep
Change <i>DF:Operation Cfg B [CCT = 0]</i> , so that <i>SBS.CycleCount()</i> threshold is in mA, not in % of FCC	Data flash default bases <i>SBS.CycleCount()</i> calculation on mA and not % of FCC	<i>DF:Operation Cfg B [CCT = 1]</i> , making the default <i>SBS.CycleCount()</i> calculation to be based on % of FCC	Data flash default changed to reflect common customer usage
When <i>DF:Operation Cfg B [CCT = 1]</i> , so that <i>SBS.CycleCount()</i> threshold is % of FCC, then <i>DF:CC Threshold</i> is used as a minimum for the <i>SBS.CycleCount()</i> threshold	Use <i>DF:CC Threshold</i> as the minimum to prevent rapid incrementing of the <i>SBS.CycleCount()</i> , damaging the data flash	Small or negative <i>SBS.Full Charge Capacity()</i> values (should not occur under normal operation) from causing the <i>SBS.CycleCount()</i> incrementing rapidly, potentially damaging the data flash	Improved system reliability
When exiting the relaxed state to sleep, the initial charge capacity is correctly calculated	Corrected initial charge capacity calculation to be accurate when exiting relaxed state to sleep	If the relaxed state was exited to sleep after a valid DOD measurement (30-minute default value), then the initial charge capacity would not be recalculated and would result in an incorrect FCC value if the sleep state was exited before another valid DOD measurement (30-minute default value)	More reliable <i>SBS:FullChargeCapacity()</i> calculation under all system conditions

Table 4. CHANGE DETAILS (continued)

CHANGE	bq0z80-V102	bq20z80-V101	COMMENTS
Correct update of Remcap in relaxed state to use passed charge	Charge or discharge current accumulated in a relaxed state used to update Remcap	If the relaxed state was exited after the accumulation of significant charge or discharge current (over at most 100 seconds with default values), the RemCap and FCC would be in error by this charge. This is only significant if the relaxed state can exist with significant current as determined by application settings.	More reliable <i>SBS:FullChargeCapacity()</i> <i>SBS:RemainingCapacity()</i> calculation under all system conditions
Implement disable of resistance update based on accumulative scale. If the product of 15 consecutive (default value) resistance scale factors is less than 0.5 or more than 1.5, then resistance update is disabled until the next valid soc measurement. Sets bit 2 of Operation Status to indicate resistance update disabled.	Prevent invalid soc values from causing incorrect resistance updates	Incorrect resistance updates that could result from invalid soc values	More reliable resistance updates under all system conditions
Implement disable of resistance update based on estimated capacity error. Sets bit 2 of Operation Status to indicate resistance update disabled.	Prevent invalid soc values from causing incorrect resistance updates	Incorrect resistance updates that could result from invalid soc values	More reliable resistance updates under all system conditions
Disable Qmax increment if due to Grid 14 and exit of discharge	Prevent unnecessary Qmax increments	Qmax increments can occur due to Grid 14 and exit of discharge	Improved Qmax data reliability under all system conditions.
Drive all unused pins low	Provides better ESD immunity	Not all unused pins driven low	Improved ESD immunity
Initial charge capacity calculation when dod0 is measured in the overdischarged state is corrected	Overdischarged state does not affect the accuracy of FCC calculations	An incorrect initial charge capacity affects FCC that is calculated during discharge or a Qmax update. If FCC is not changed by a Qmax update, then reported RemainingCapacity could be negative after 5 hours of relaxation	More reliable <i>SBS:FullChargeCapacity()</i> <i>SBS:RemainingCapacity()</i> calculation under all system conditions
Correct calculation of FCC and RemCap when dod0 is taken when the battery is overdischarged or overcharged. This allows RemCap to go negative, or greater than FCC (though is only reported from 0 - FCC).	Overcharged/Overdischarged does not affect the accuracy of FCC and RemCap calculations	The RemainingCapacity will increment (or decrement) during charging (discharging) even when the battery is in an overdischarged (overcharged) state.	More reliable <i>SBS:FullChargeCapacity()</i> <i>SBS:RemainingCapacity()</i> calculation under all system conditions
Change cell imbalance <i>DF:Battery Rest Time</i> from 1 byte to 2 bytes and set the default value to 1800 seconds	New feature providing improved customization	Feature not available	Improved customization for Cell Imbalance detection
Use upper and lower limit for resistance accumulative scale. Set default values to 300% and 30%.			More reliable resistance updates under all system conditions
Add <i>DF:CF MaxError limit</i> for setting <i>SBS.BatteryMode()</i> [<i>CONDITION FLAG</i>]. Set default value to 100%.	New feature providing improved customization	Feature not available	Improved customization

IN



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PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
BQ20Z80DBT-V102	NRND	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ20Z80DBTR-V102	NRND	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ20Z80DBTR-V102G4	NRND	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ20ZDBT-V102G4	NRND	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ20ZDBTR-V102G4	NRND	TSSOP	DBT	38		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

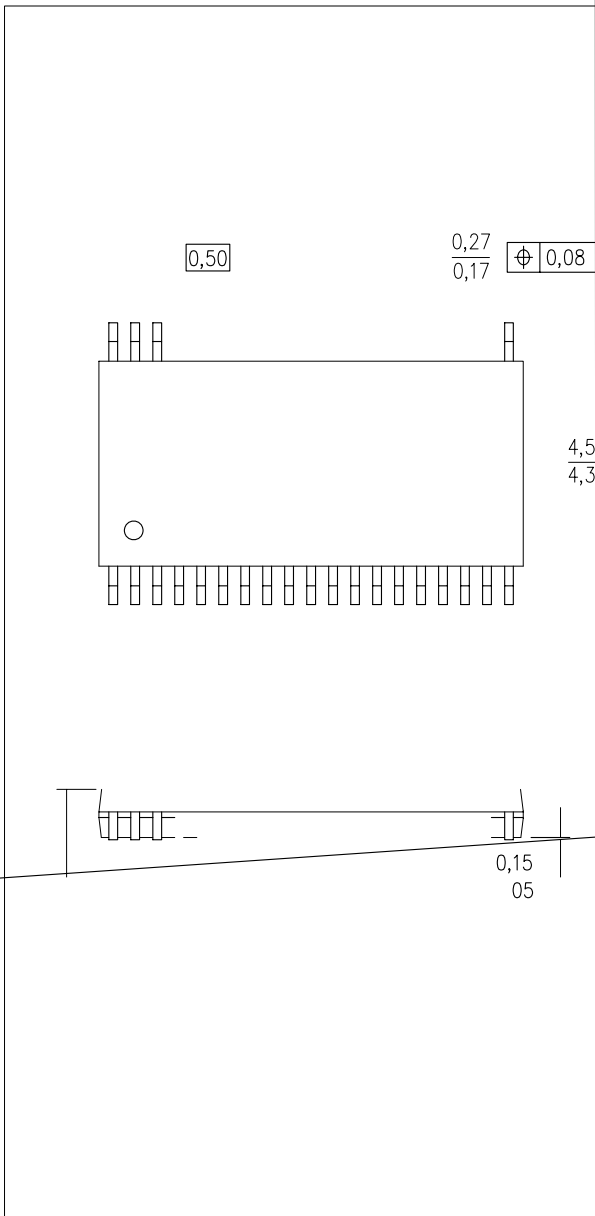
OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps u171.305.625 (0.1%) -305.625 .1% 0.



NOTES: A. All linear dimensions are in millimeters. Dimensions do not include mold flash or
 D. Falls within JEDEC MO-153.



Example
Mask Defin

4"

customers should change the

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