UNITRODE

bq2014

Gas Gauge IC with External Charge Control

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Charge control output operates an external charge controller such as the bq2004 Fast Charge IC
- Designed for battery pack integration
- 120 µA typical standby current
- Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- User-selectable end-of-discharge threshold
- Battery voltage, nominal available charge, temperature, etc. available over serial port
- 16-pin narrow SOIC

General Description

The bq2014 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery charge. The IC monitors the voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

Self-discharge of NiMH and NiCd batteries is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

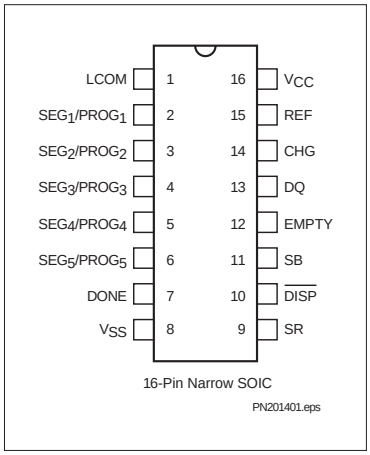
The bq2014 includes a charge control output that controls an external Fast Charge IC such as the bq2004. Nominal Available Charge (NAC) may be directly indicated using a five-segment LED display.

The bq2014 supports a simple single-line bidirectional serial link to an external processor (with a common ground). The bq2014 outputs battery information in response to external commands over the serial link.

Internal registers include available charge, -tings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2014 gas gauge data registers.

The bq2014 may operate directly from three or four cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Pin Connections



16-Pin Narrow SOIC

PN201401.eps

Pin Names

LCOM	LED common output
$SEG_1/PROG_1$	LED segment 1/ program 1 input
$SEG_2/PROG_2$	LED segment 2/ program 2 input
$SEG_3/PROG_3$	LED segment 3/ program 3 input
$SEG_4/PROG_4$	LED segment 4/ program 4 input
$SEG_5/PROG_5$	LED segment 5/ program 5 input
DONE	Fast charge complete
REF	Voltage reference output
CHG	Charge control output
DQ	Serial communications input/output
EMPTY	Empty battery indicator output
SB	Battery sense input
$\overline{DISP}$	Display control input
SR	Sense resistor input
V_{CC}	3.0–6.5V
V_{SS}	System ground

12/95 C

Pin Descriptions

LCOM **LED common output**

[illegible]

SEG_1–SEG_5 **LED displa segment outputs (dual function with $PROG_1$ $PROG_5$)**

[illegible]

$PROG_1$–$PROG_5$ **Programmed full count selection imputs (dual function with SEG_1 SEG_5)**

[illegible]

$PROG_3$–$PROG_4$ **Gas gauge rate selection inputs (dual function with SEG_3 SEG_4)**

[illegible]

$PROG_5$ **Self-discharge rate selection (dual function with SEG_5)**

[illegible]

CHG **Charge control output**

[illegible]

DONE **Fast charge complete**

[illegible]

Voltage Thresholds

n n n n w n n, / , n, 2014 n n, - - n B n. n, - - n n / n w w n, n:

$$\frac{2}{3} = -1$$

w n , 2 nn 3 nn n n n, - (ED) n (C). ED n w n C n n, n .

w ED 2014 w :

ED 1 (w n n) = 1.05

ED F ( ) = 0.95

B w w ED n n , n n - n B, n n (n n n n G G n). B'

D n, n 2014 n n n n n n . ED n n ≤ -250 n > -250 .

EMPTY Output

E w n w n B < EDF n n n - .

Reset

2014 n B n 0.1 B n w 0.25 n 2.25 (C) - n w n n.

Temperature

2014 n n n n 10 C n -35 C +85 C. - n

n n, - n n, n n n n. n, 10 C n n wn w:

TMPGG (hex)	Temperature Range
0	< -30 C
1	-30 C -20 C
2	-20 C -10 C
3	-10 C 0 C
4	0 C 10 C
5	10 C 20 C
6	20 C 30 C
7	30 C 40 C
8	40 C 50 C
9	50 C 60 C
A	60 C 70 C
B	70 C 80 C
C	> 80 C

Layout Considerations

2014 n w n n n (n) C F C w n - n n n. n - n n w n n n n n A n :

- (C2 n C3). B n CC n n A 0.1µ n CC.
- n (1, C1). n.
- n (16). 2014.

Gas Gauge Operation

n w F 2
2014. 2014
n , w
C n -
n n , w
-

n n , n A C (AC),
n n n
. B n n AC ,
w n n -
AC n n n DC (D
C n).

D C n (DC)
D (D) n
n
w n ,
2014 n n n
n n .

n
F C n (FC) wn n 2. n
D , AC n n n n
n n -
w n n n -
n w n .

n n n 2014 n
. AC n n n , 2-
n ; w AC n
AC . A n

n n n n
AC . n n n n -
n n AC n n
n - ( ) n n AC .
AC n n n n
wn , n n
- n w 256.
n n n 2, 4, 8,
n n n , w , n n n -
. , n n -
n n n n .

1. Last Measured Discharge (LMD) or learned batter capacit :

D
n . n n (n cc -
n), D = FC. D n n
, D w
n D. C n
(DC) n n w
ED 1. A n -
n DC D .
D 100% n -
n .

2. Programmed Full Count (PFC) or initial batter capacit :

n D n n -
n G1 G4. 2014 .
n n n n
FC 2. FC

= %64

B (A) * (Ω) = = 5 400

FC ( ) :

FC - 2200 A * 0.1Ω = 220

:

Example: Selecting a PFC Value

G :

= 0.1Ω
= 6
C = 2200 A , C
C = 50 A 2A

211
(2110 A) 2014 w
ED 1.

3. Nominal Available Charge (NAC):

AC
D w
0. AC 0
ED = 1.
, AC. w AC = D.

4. Discharge Count Register (DCR):

DC AC AC
0 B < ED 1.
AC = 0 ( ), DC. A AC = 0, DC.
DC
0 w AC = D. DC
w FFFF.

DC w D
ED 1:

- w AC = D ED 1.
- 4096 (8% 18% FC,
FC).
- ≥ 0 C w ED 1

(D) w
D.

Charge Counting

C
. 2014
(+) > ,
w .
(D F) 375µ , 2014
AC .
, 2014 ED .
C AC

Charge Control

C C G -
w AC > 0.94 * D.
C G w
(C G F G 1). C G w
w AC < 0.94 * D -
.

DONE Input

2014 w
- D E , AC
D AC/64 (C). - AC
94% D (AC w 94%) AC/47 ( )
- D w D E.

Discharge Counting

A w < D AC
DC
ED 1 = 0. E
(FD) < -4
, .
-4 D
D F -
. D -300

Discharge Compensation

:

A 0.05 10 C = 1.00 + (0.05 *)

= 10 C 10 C

-150 <

w n D DC n
n w n 255. -
n (C) D n -
w n 64

bq2014 Registers

2014 6

Command Register (CMDR)

C D 2014.

C D :

- /
- C

/ :

/ :

0 2014 C D .

1 C D .

C D . A

Primary Status Flags Register (FLGS1)

F G 1 (=01) 2014 .

charge status (C G) >. A C G.

C G :

C G :

0 E <

1 >

battery replaced (B) B ( ), B, C (2.25), 0.1 . B 2014 ( ). B AC D, ED 1 . B = 1.

B :

B :

0 B AC = 492-22 7.95 -1. 3 1 1.35

Table 6. bq2014 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
C D	C n	00		/	AD6	AD5	AD4	AD3	AD2	AD1	AD0
F G 1		01		C G	B	B	C	D	n/	ED 1	ED F
GG	n	02		3	2	1	0	GG3	GG2	GG1	GG0
AC	n	03	/	AC 7	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0
AC	n w	17		AC 7	AC 6	AC 5	AC 4	AC 3	AC 2	AC 1	AC 0
BA D	B n n	04	/	BA D7	BA D6	BA D5	BA D4	BA D3	BA D2	BA D1	BA D0
D		05	/	D7	D6	D5	D4	D3	D2	D1	D0
F G 2	n	06		C	D 2	D 1	D 0	n/	n/	n/	D
D	n wn	07		n/	n/	D6	D5	D4	D3	D2	D1
	n	08		n/	n/	6	5	4	3	2	1
C	C n n	09		C 7	C 6	C 5	C 4	C 3	C 2	C 1	C 0
D F	D n	0A	/	D F7	D F6	D F5	D F4	D F3	D F2	D F1	D F0
B	B	0B		B7	B6	B5	B4	B3	B2	B1	B0
	En	0C	/	7	6	5	4	3	2	1	0
		39			0	0	0	0	0	0	0

Note: n/ = n

C :

C :

0 n D w

1 A 64 n w n
D w n

valid discharge (D) w n
2014 AC = D D E
n n D
n n n D :

- (DC)
(4096
n) n D .
- A > n n
256 AC n .
- ED w 0 C
D :

D :

0 DC ≥ 4096, n
n , ED 1 w
n 0 C

1 n AC = D
D E

first end-of-discharge warning (ED 1)
w n
n, EG1, 4
n ED 1 , w
w n n .
ED 1 n
. ED 1 n n-
(-
n).

ED 1 :

ED 1 :

0 , B ≥

1 B < D=0 (
F G 2 n)

final end-of-discharge warning (ED F)
w n w n-
n. A n . ED F
n . n
E n n ED F. E
, w n
. ED F
100 w ED 1 .

ED F :

ED F :

0 ,
B ≥ - 100

1 B < - 100 n D=0
(F G 2 n)

Voltage Threshold Register (VTS)

n - (ED 1 n
ED F) n n (=0).
/w ED 1 n .
ED F 100 w ED 1. n
70 , n n ED 1 = 1.05 n
ED F = 0.95 . ED 1 = 2.4 * (/256).

Battery Voltage Register (VSB)

- n B n. B
n w
n .
B = 2.4 * (B/256)

VSB Register Bits							
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

Temperature and Gas Gauge Register (TMPGG)

GG (=02) w- 2014 7.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
3	2	1	0	-	-	-	

2014 AC, D. GG 1/16 0 15/16.

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

GG A -w :

Temperature	Available Capacity Calculation
> 0 C	AC / F
-20 C < < 0 C	0.75 * AC / F
< -20 C	0.5 * AC / F

> 0 C -20 C < < 0 C 10 C .

Nominal Available Charge Register (NACH/NACL)

/w AC (=03) AC w- (=17) 2014. AC / AC.

Table 7. Temperature Register Translation

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	< -30 C
0	0	0	1	-30 C < < -20 C
0	0	1	0	-20 C < < -10 C
0	0	1	1	-10 C < < 0 C
0	1	0	0	0 C < < 10 C
0	1	0	1	10 C < < 20 C
0	1	1	0	20 C < < 30 C
0	1	1	1	30 C < < 40 C
1	0	0	0	40 C < < 50 C
1	0	0	1	50 C < < 60 C
1	0	1	0	60 C < < 70 C
1	0	1	1	70 C < < 80 C
1	1	0	0	> 80 C

, AC AC 0. 2014 , AC 0. AC AC 0 B = ED 1. *W i ing o he NAC egi e affec he a ai l able cha ge co n and , he efo e, affec he b 2014 ga gage o e a ion. Do no i e he NAC egi e o a al, e gea e han* D.

Battery Identification Register (BATID)

/w BA D (=04) . BA D CC 2 . BA D 2014.

Last Measured Discharge Register (LMD)

D /w (=05) 2014 2014 D 2014 D FC 2014.

Secondary Status Flags Register (FLGS2)

F G 2 (=06) 2014 .

charge rate (C) . F w C w2 /.

C :

FLGS2 Bits							
7	6	5	4	3	2	1	0
C	-	-	-	-	-	-	-

C :

0 w 2 /

1 2 /

w
C = 1. n C = 0, n -
. n C
n .

discharge rate , D 2 0, 6 4.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	D 2	D 1	D 0	-	-	-	

- n w :

DR2	DR1	DR0	V_{SR} (V)
0	0	0	> -150
0	0	1	< -150

overload (D) w n
, < -250 D n -
n n n n -
> -150 n n
n n w n -
.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	D

D 2 0 n D n n
n w
w .

Program Pin Pull-Down Register (PPD)

- n D (=07) n n
n n 2014.
, EG1 5 n D E,
n , D1 6. A n n
- wn n n n n n
. F , EG1 n EG4
- wn , n n D 101001.
(**Note:** D E wn n.)

Program Pin Pull-Up Register (PPU)

- n (=08) n n
n n n 2014.
, EG1 5 n D E,
n , 1 6. A n n -
n n n . F , EG3 n
D E - , n n
/ 100100.

PPD/PPU Bits							
8	7	6	5	4	3	2	1
-	-	6	5	4	3	2	1
-	-	D_6	D_5	D_4	D_3	D_2	D_1

Capacity Inaccurate Count Register (CPI)

- n C (=09) n -
n n n n n
w n D . B -
n , 2014 n n
. A (AC= D)
(ED 1=1) n D
n n n n n ,
n 0°C, n
- n 4096 n .

C n n n
. n AC > 0.94 * D, w ,
C n n n ;
C n n n n n
AC < 0.94 * D.
n n n C -
n AC. C n n 255 w -
n n . n n n C n -
n 64, n , C , -
n F G 1 . C
w n n D ,
n C .

Digital Magnitude Filter (DMF)

-w D F (=0A) n
w n n n ,
n . B w n n -
n , D n n
.

Note: C n w n w n -
. A D n w - -
n 2014. n
4 n n D F .

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2014 reset is performed. Setting any bit other than the most-significant bit of the RST register is not allowed , and results in improper operation of the bq2014.

Resetting the bq2014 sets the following:

LMD = PFC

CPI, VDQ, NAC, and NACL = 0

CI and BRP = 1

Note: Self-discharge is disabled when PROG $_5$ = H.

Display

The bq2014 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively..

The bq2014 displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the $SEG_{1–5}$ outputs are inactive. Note: $\overline{DISP}$ must be tied to V_{CC} if the LEDs are not used. When $\overline{DISP}$ is left floating, the display becomes active whenever the NAC registers are counting at a rate equivalent to V_{SRO} < -4mV or charge current is detected, $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz, with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

The bq2014 can operate directly from 3 or 4 cells. To facilitate the power supply requirements of the bq2014, an REF output is provided to regulate an external low-threshold n-FET. A micropower source for the bq2014 can be inexpensively built using the FET and an external resistor; see Figure 1.

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
- CC		-0.3	7.0		
A		-0.3	7.0		
EF		-0.3	8.5		C 1 (F, 1)
		-0.3	7.0		100Ω (2014 -).
	-	0	70	C	C

DC Electrical Characteristics ($T_A = T_{OPR}$)

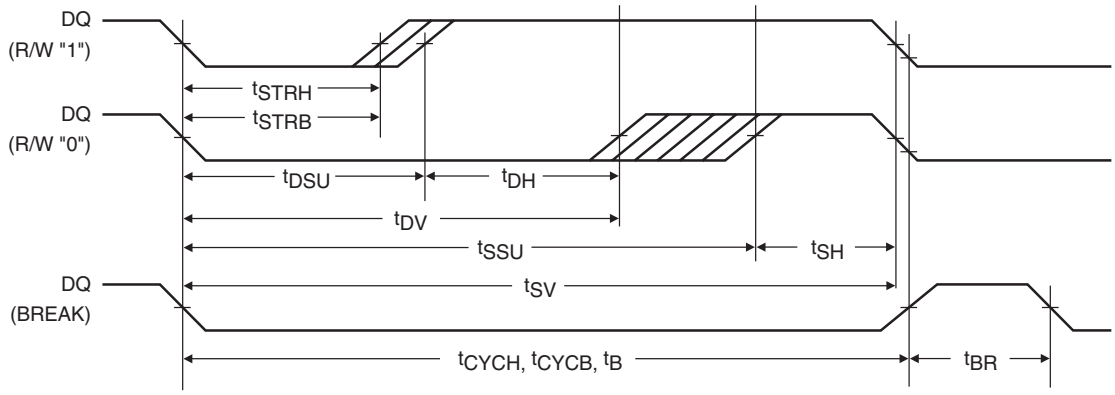
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
- CC		3.0	4.25	6.5	-	

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
[illegible]	[illegible]	3	-	-	[illegible]	[illegible]
[illegible]	[illegible]	3	-	6	[illegible]	
[illegible]	[illegible]	5	-	-	[illegible]	
[illegible]	[illegible]	500	-	-	µs	
[illegible]	[illegible]	-	-	750	µs	
[illegible]	[illegible]	750	-	-	µs	
[illegible]	[illegible]	1.50	-	-	[illegible]	
[illegible]	[illegible]	-	-	2.25	[illegible]	
[illegible]	[illegible]	700	-	-	µs	
[illegible]	[illegible]	2.95	-	-	[illegible]	
[illegible]	[illegible]	3	-	-	[illegible]	
[illegible]	[illegible]	1	-	-	[illegible]	

Note: [illegible]

Serial Communication Timing Illustration



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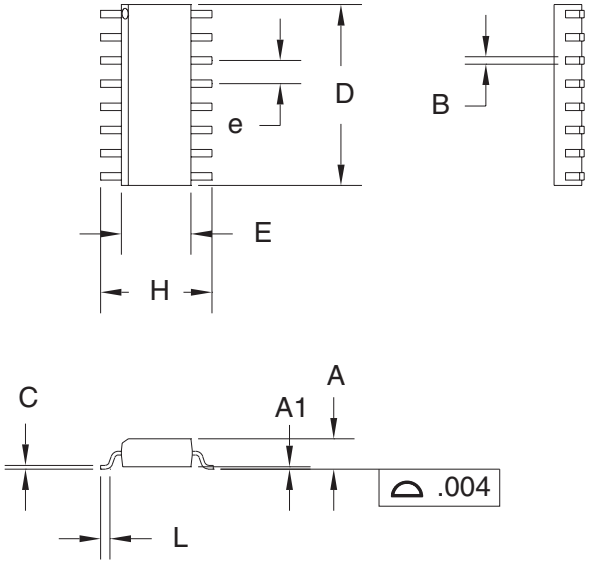
16-Pin SOIC Narrow (SN)



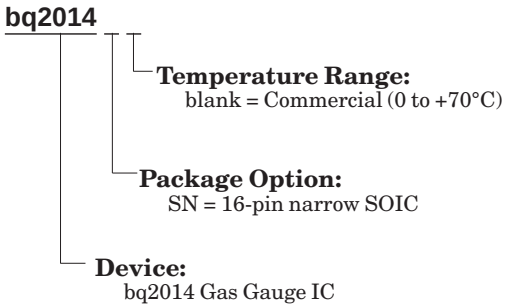
16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

All dimensions are in inches.

ChangeNo.	Page No.	Description	Nature of Change

Ordering Information



UNITRODE

PACKAGING INFORMATION

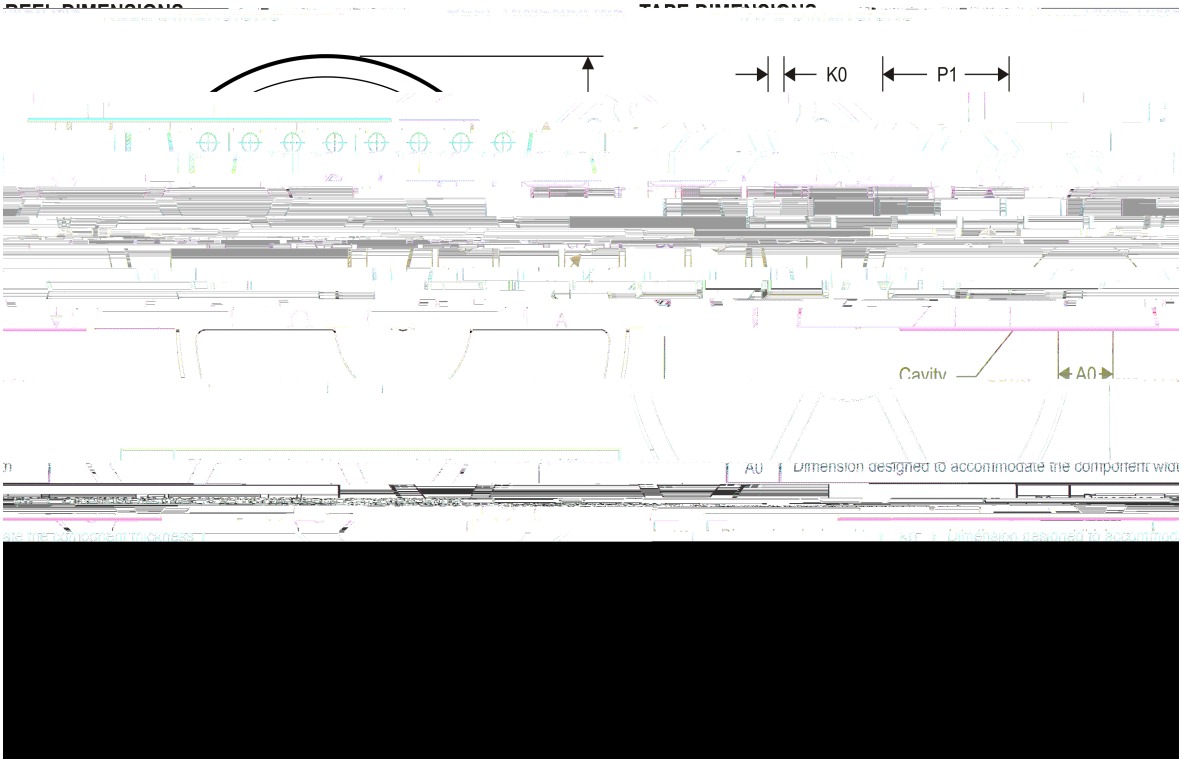
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ2014SN-D120	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ2014SN-D120G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ2014SN-D120TR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples
BQ2014SN-D120TRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

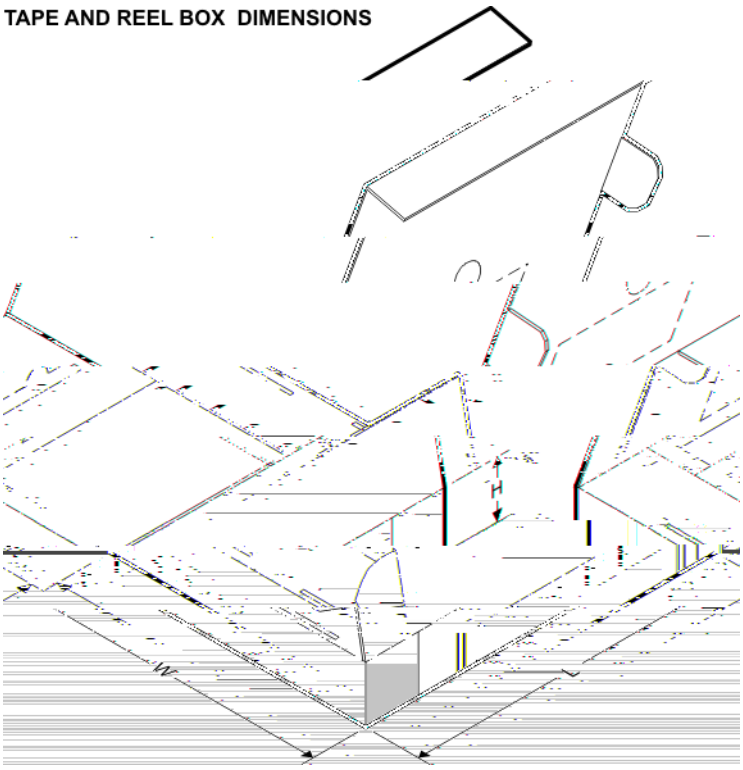
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2014SN-D120TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0		

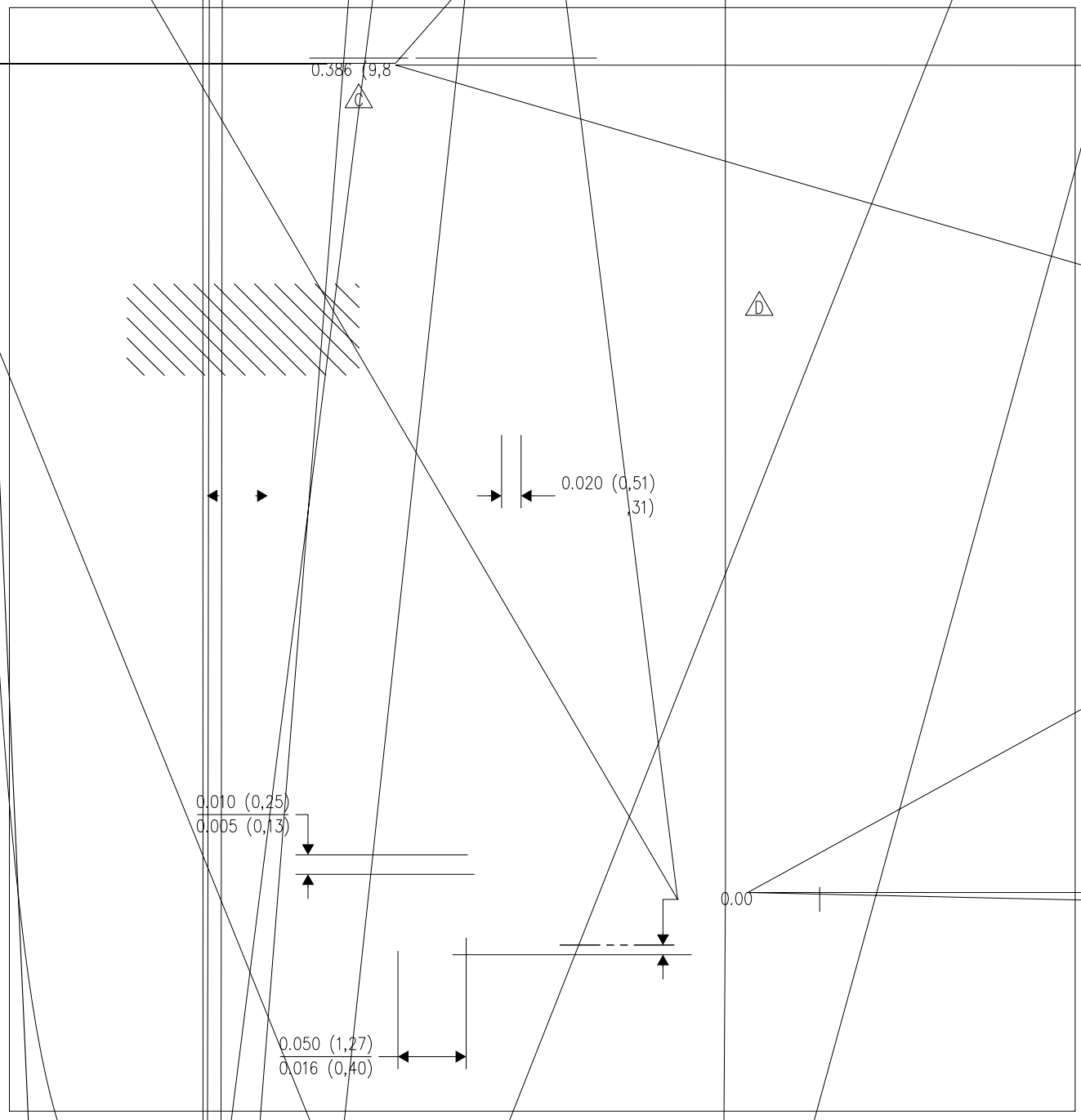
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins

PLASTIC SMALL OUTLINE

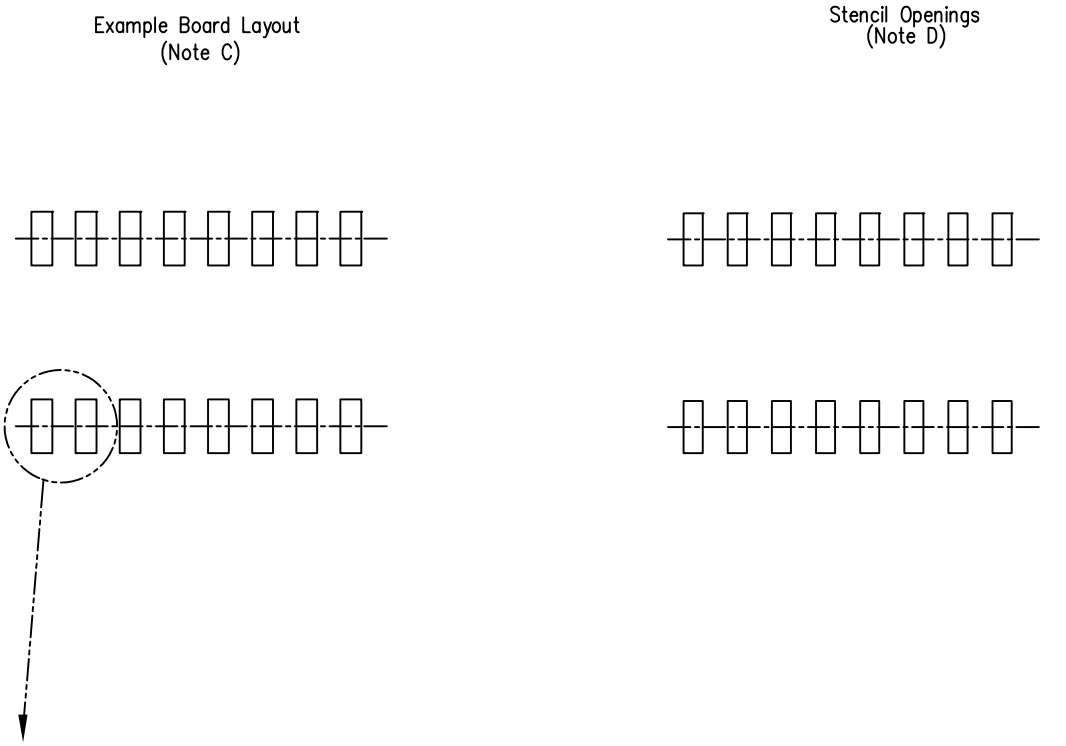


C ot include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006

D ce interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



4211283–4/E 08/12

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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