

**HIGH-PERFORMANCE BATTERY MONITORING IC  
WITH COULOMB COUNTER, VOLTAGE AND TEMPERATURE SENSORS**

**FEATURES**

- Multifunction Monitoring Integrated Circuit Designed to Work With an Intelligent Host Controller :
  - Provides State of Charge Information for Rechargeable Batteries
  - Provides Accurate Battery Voltage and Temperature Measurement
- High Accuracy Coulometric Charge and Discharge Current Integration With Automatic Offset Compensation
- 11-Bit Analog-to-Digital Converter Reports Battery Voltage With Gain and Offset Correction
- Differential Current Sense
- 32 Bytes of General Purpose RAM
- 96 Bytes of Flash (Including 32 Bytes of Shadow Flash)
- 8 Bytes of ID ROM
- Internal Temperature Sensor Eliminates the Need for an External Thermistor
- Programmable Digital Input/Output Port
- High-Accuracy Internal Timebase Eliminates External Crystal Oscillator
- Low Power Consumption:
  - Operating : 30  $\mu$ A
  - Sleep: 1  $\mu$ A
  - Hibernate: 600 nA
- Single-Wire HDQ Serial Interface
- Packaging: 8-LEAD TSSOP

**PW PACKAGE  
(TOP VIEW)**

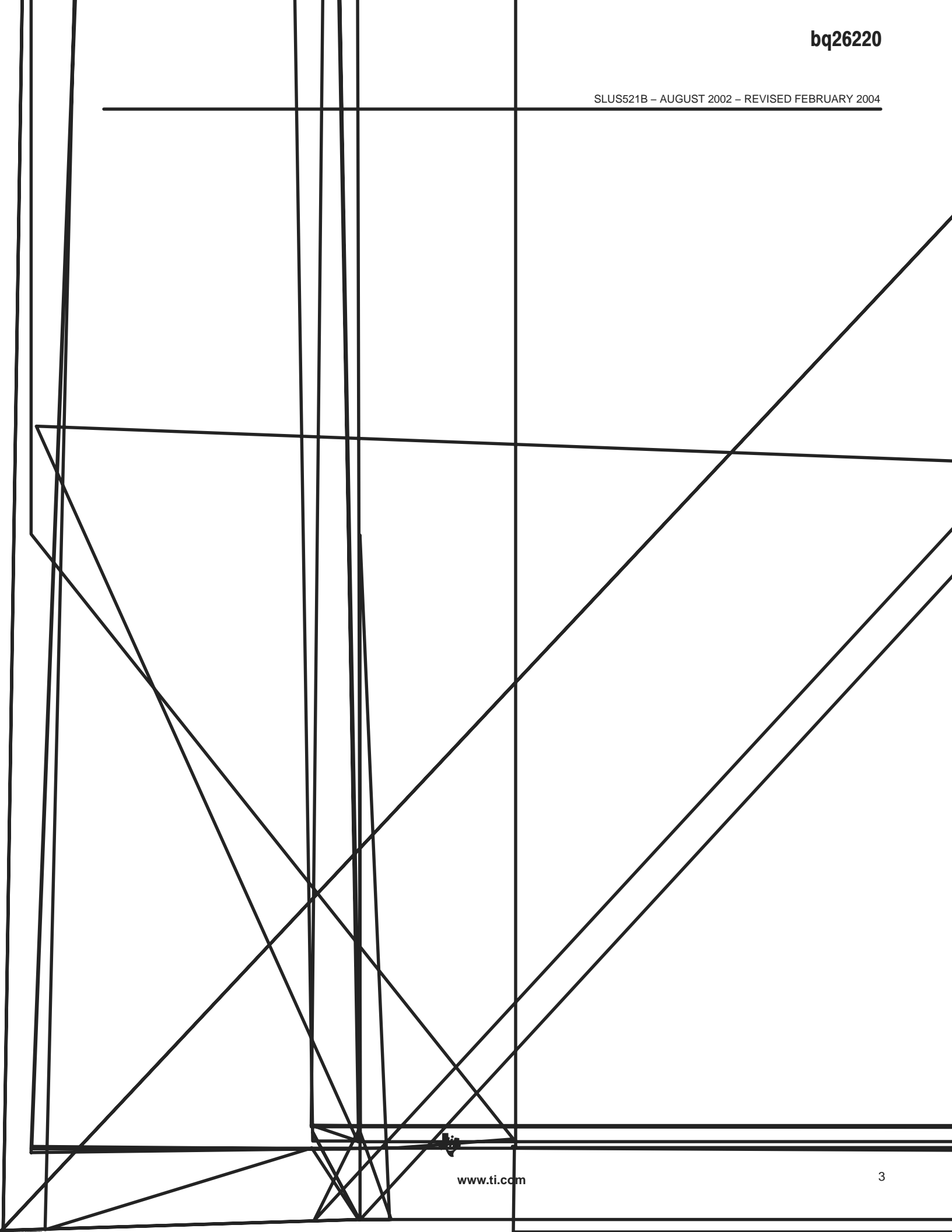


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**bq26220**

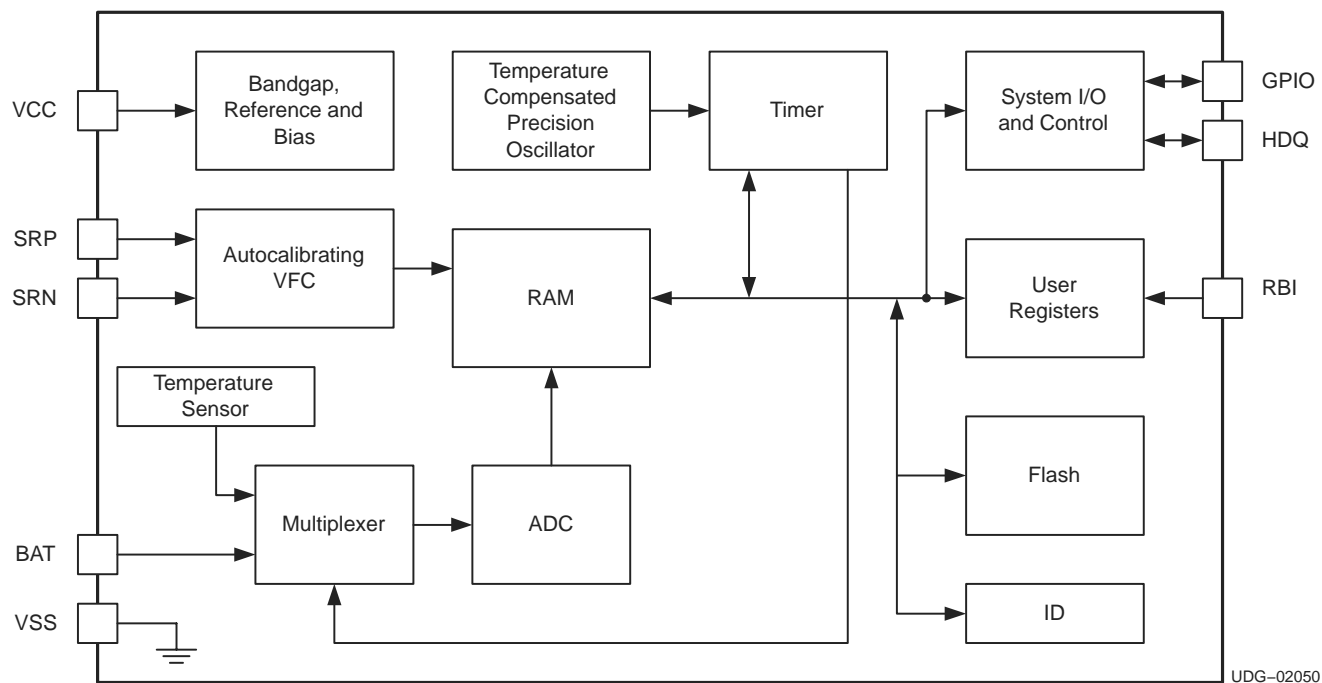
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FUNCTIONAL BLOCK DIAGRAM



UDG-02050

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	No.		
BAT	5	I	Battery voltage sense input. This pin is used for sensing and measuring the battery voltage.
RBI	1	I	Register backup input. The RBI input pin is used with a storage capacitor or external supply to provide backup potential to the internal RAM and registers while $V_{CC}$ is $< V_{(POR)}$ .
GPIO	8	I/O	General-purpose input/output pin. GPIO is a general-purpose programmable input or output port whose state is controlled via the HDQ serial communications interface.
HDQ	4	I/O	Single-wire HDQ interface. HDQ is a single-wire serial communications interface port. This bidirectional input/output communicates the register information to the host.
SRN	6	I	Current sense input 2. The bq26220 interprets charge and discharge activity by monitoring and integrating the voltage drop, $V_{SR}$ , across pins SRP and SRN. The SRN input connects to the sense resistor and the negative terminal of the pack. $V_{SRP} < V_{SRN}$ indicates discharge, and $V_{SRP} > V_{SRN}$ indicates charge.
SRP	7	I	Current sense input 1. The bq26220 interprets charge and discharge activity by monitoring and integrating the voltage drop, $V_{SR}$ , across pins SRP and SRN. The SRP input connects to the sense resistor and the negative terminal of the battery. $V_{SRP} < V_{SRN}$ indicates discharge, and $V_{SRP} > V_{SRN}$ indicates charge.
VCC	2	I	Supply voltage
VSS	3	-	Ground







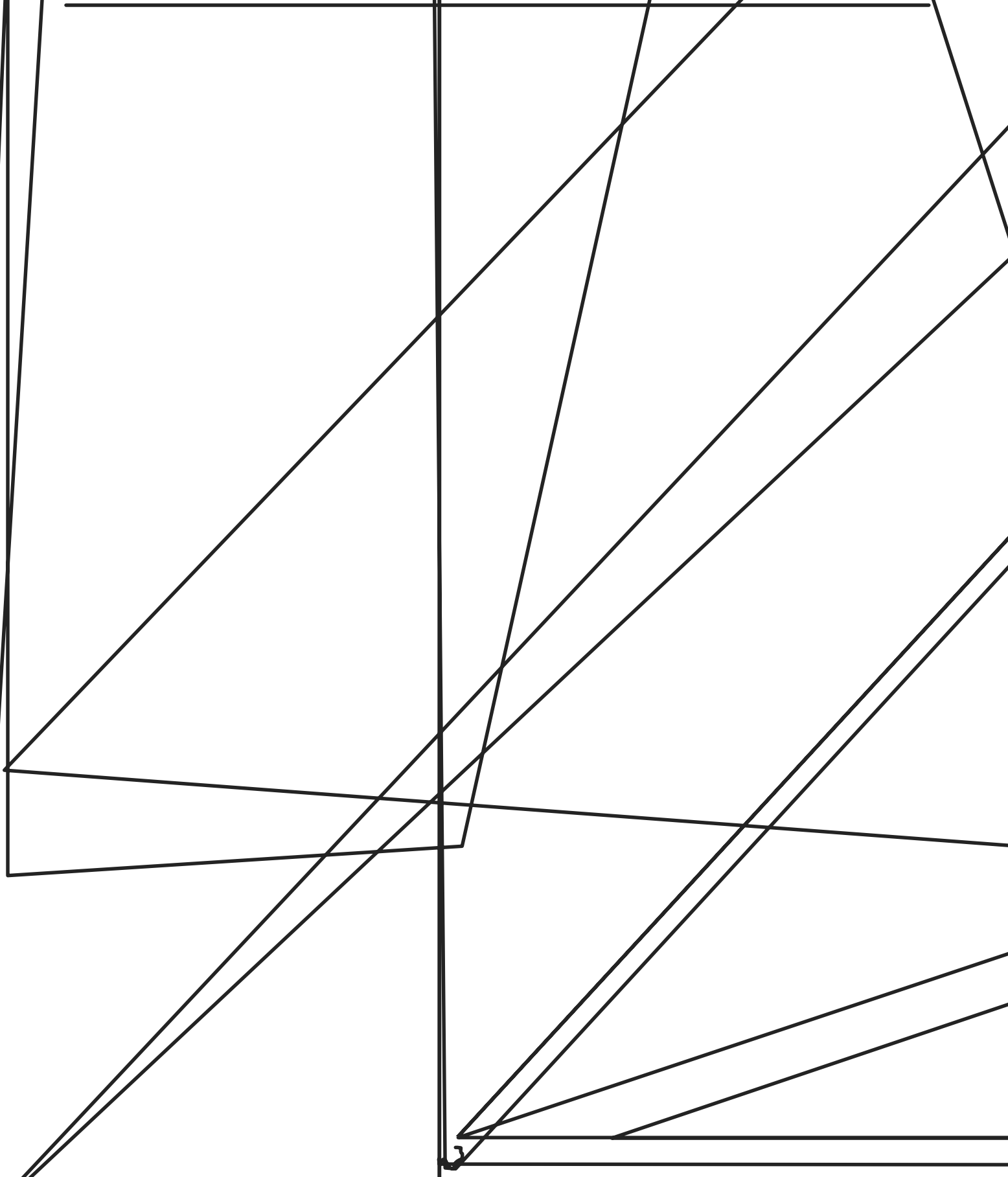




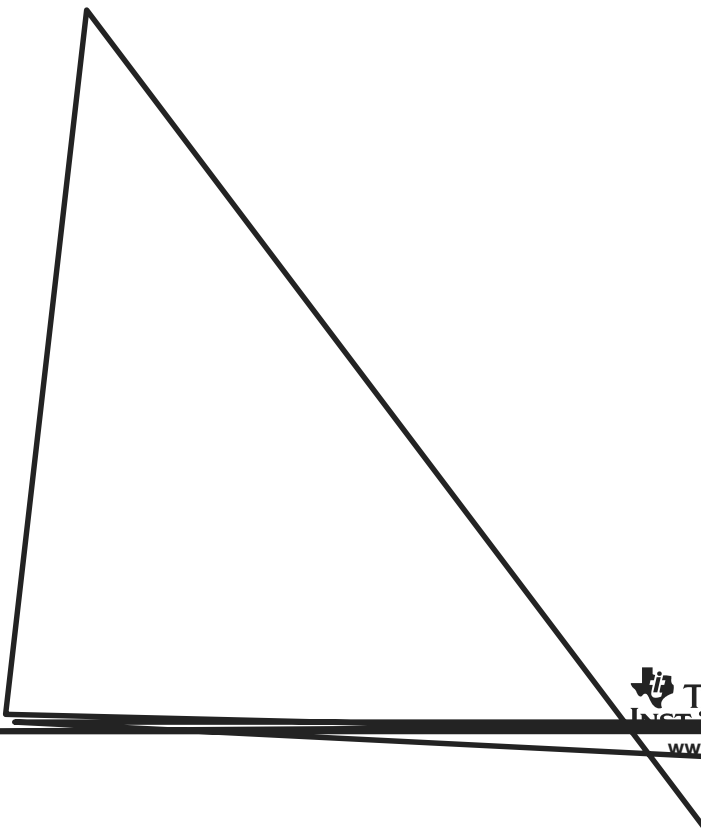


for the voltage analog to digital converter. The format for this register is described in Table 5. Table 5. ID ROM Command Code S

SLU6621E AUGUST 2002 REVISED FEBRUARY 2004











## APPLICATION INFORMATION

### clear register (CLR)

The bits in the CLR register (address 0x63) clear the DCR, CCR, SCR, DTC, and CTC registers, reset the bq26220 by forcing a power-on-reset and setting the state of the STAT pin as described in Table 11.

**Table 11. CLR Register**

CLR BITS							
7 (MSB)	6	5	4	3	2	1	0 (LSB)
RSVD	RSVD	RSVD	CTC	DTC	SCR	CCR	DCR

**Table 12. CLR Register Definitions**

RSVD	RSVD bits (bits 5, 6 and 7) are reserved for future use and should be written to 0 by the host.
CTC	CTC bit (bit 4) clears the CTCH and CTCL registers and the STC bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the CTC bit is cleared. This bit is cleared on power-on-reset.
DTC	DTC bit (bit 3) clears the DTCH and DTCL registers and the STD bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the DTC bit is cleared. This bit is cleared on power-on-reset.
SCR	SCR bit (bit 2) clears both the SCRH and SCRL registers. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.
CCR	CCR bit (bit 1) clears both the CCRH and CCRL registers. Writing a 1 to this bit clears the CCRH and CCRL registers. After these registers are cleared, the CCR bit is cleared. This bit is cleared on power-on-reset.
DCR	DCR bit (bit 0) clears both the DCRH and DCRL registers. Writing a 1 to this bit clears the DCRH and DCRL registers. After these registers are cleared, the DCR bit is cleared. This bit is cleared on power-on-reset.

### flash command register (FCMD)

The FCMD register (address 0x62) is the flash command register and programs a single flash byte-location, perform flash page erase, transfer RAM to flash and flash to RAM, enter sleep mode, and power-down. These functions are performed by writing the desired command code to the FCMD register. After the bq26220 has finished executing the issued command, the flash command register is cleared.

**Table 13. FCMD Register Definitions**

0x0F	Program byte command code. This code ANDs the contents of the FPD register with the contents of flash byte location pointed to by the contents of the FPA register.
0x40	Erase page 0 command code. This code erases all the bytes of flash from address 0x00 to 0x1F.
0x41	

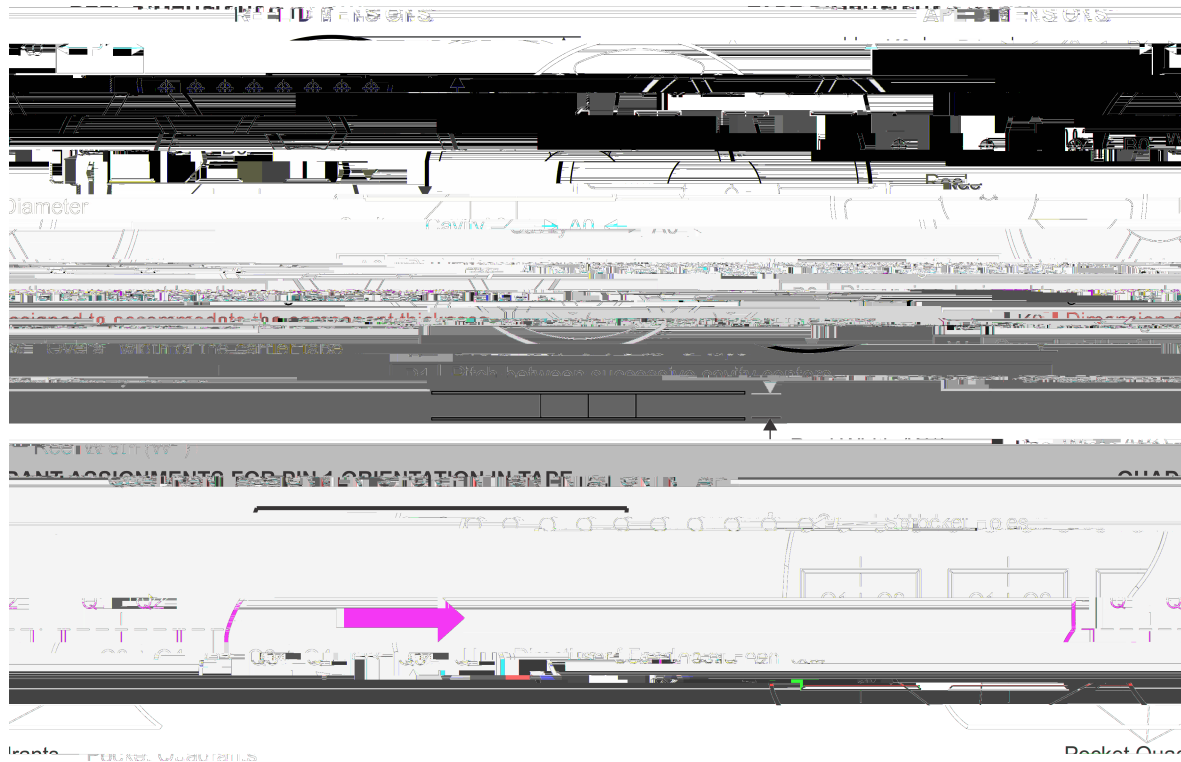
**APPLICATION INFORMATION*****temperature registers (TMPH, TMPL)***

The TMPH (address 0x61) and the TMPL registers (address 0x60) reports die temperature in hex format in units of 0.25°K. The temperature is reported as 11 bits of data, using all 8 bits of the TMPL low register and the 3 bits of the TMPH register. The temperature should be read as the concatenation of TMPH [2:0] and TMPL [7:0], 0.25°K/LSB. The 5 MSBs of TMPH, TMPH [7:3], are cleared on POR and are reserved. The 5 bits should also be masked off when reading the temperature, to ensure that incorrect data is not used when calculating the temperature.

**PACKAGING INFORMATION**

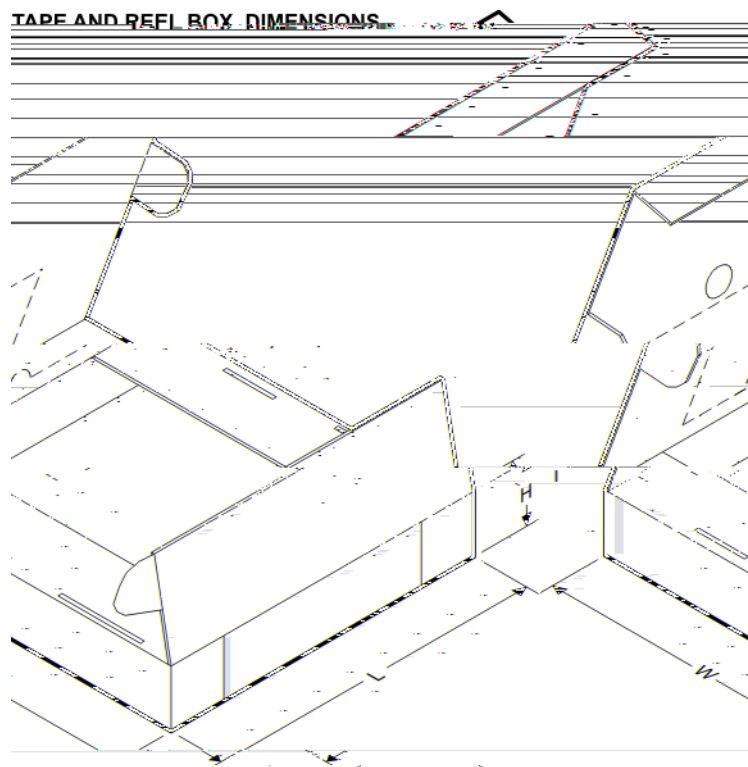


TAPE AND REEL INFORMATION



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ26220PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

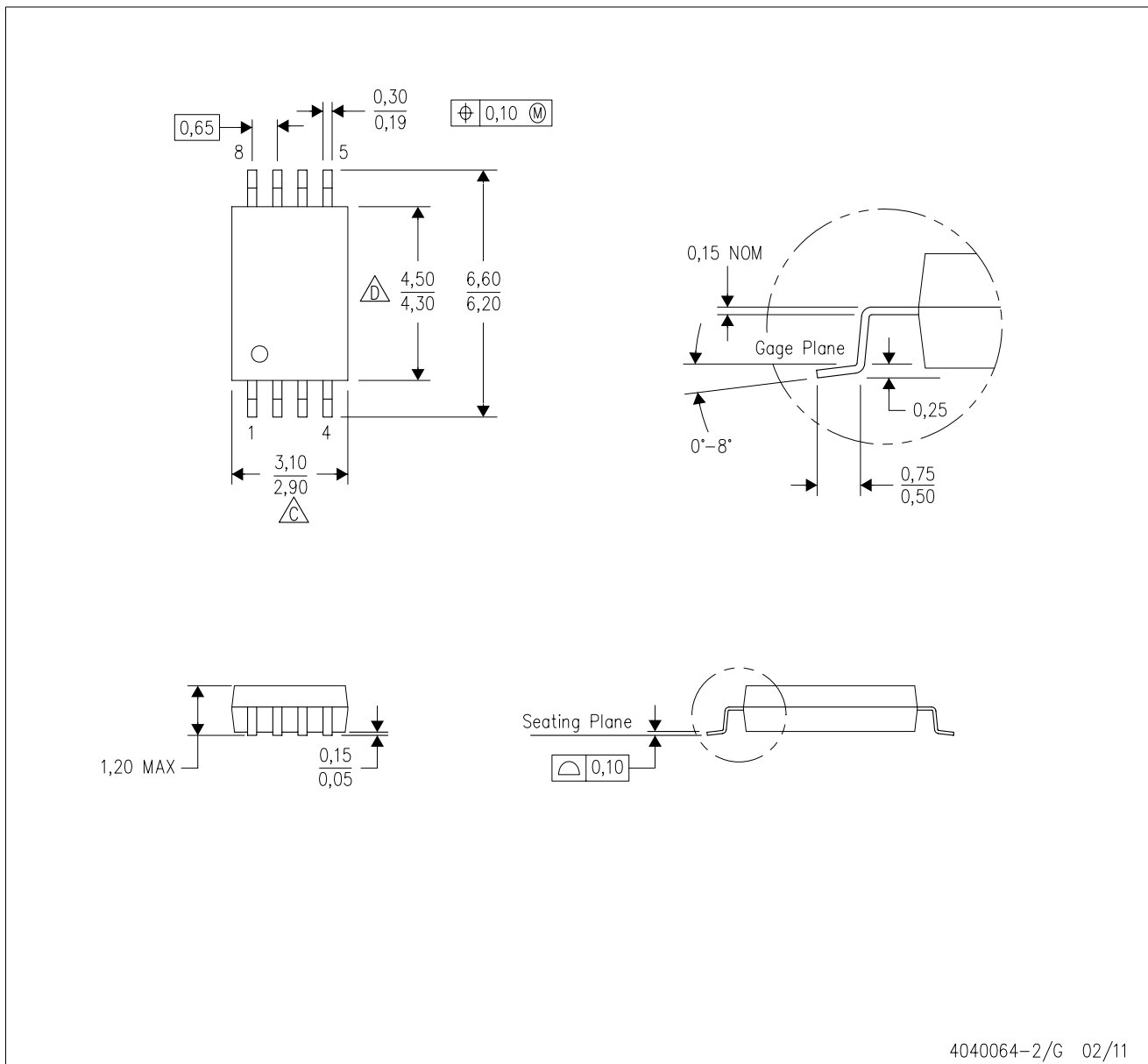


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ26220PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

PW (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040064-2/G 02/11

NOTES: A. All line 1

- △ Include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
- △ Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
- E. Falls within JEDEC MO-153

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