High- or Low-Side Measurement, Bidirectional CURRENT/POWER MONITOR with 1.8-V I²C™ Interface

Check for Samples: INA231

FEATURES

- **Bus Voltage Sensing From 0 V to +28 V**
- **High- or Low-Side Sensing**
- **Current, Voltage, and Power Reporting**
- **High Accuracy:**
  - **0.5% Gain Error (Max)**
  - **50- V Offset (Max)**
- **Configurable Averaging Options**
- **Programmable Alert Threshold**
- **1.8-V I²C Compliant**
- **Power-Supply Operation: 2.7 V to 5.5 V**
- **Package: 1.68-mm × 1.43-mm, WCSP-12**

APPLICATIONS

- **Smartphones**
- **Tablets**
- **Servers**
- **Computers**
- **Power Management**
- **Battery Chargers**
- **Power Supplies**
- **Test Equipment**

DESCRIPTION

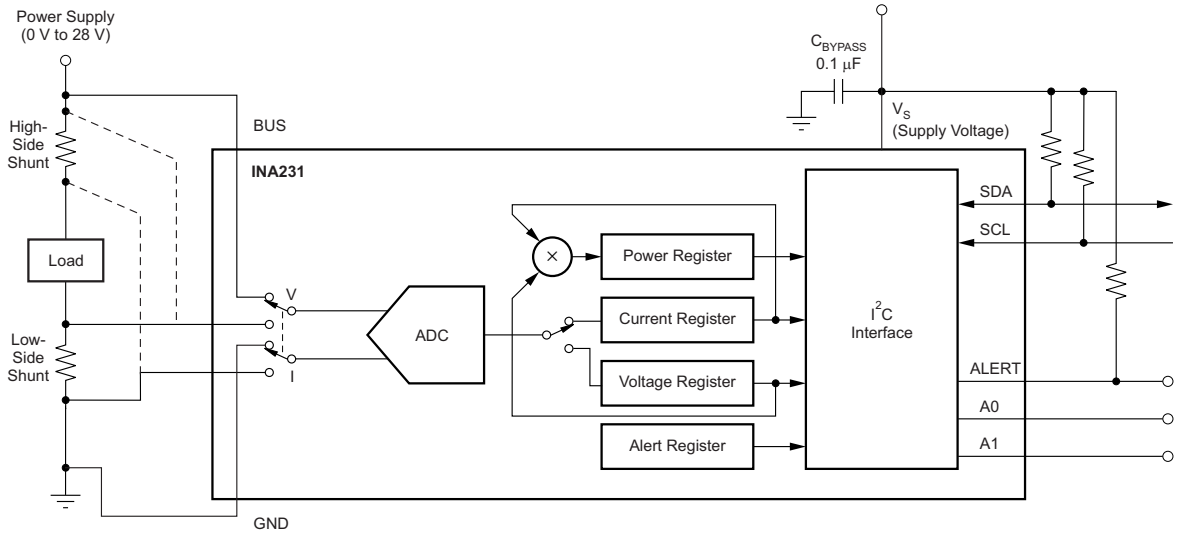
The INA231 is a current-shunt and power monitor with a 1.8-V compliant I²C interface that features 16 programmable addresses. The INA231 monitors both shunt voltage drops and bus supply voltage. Programmable calibration value, conversion times, and averaging combined with an internal multiplier enable direct readouts of current in amperes and power in watts.

The INA231 senses current on buses that vary from 0 V to +28 V, with the device powered from a single +2.7-V to +5.5-V supply, drawing 330 µA (typical) of supply current. The INA231 is specified over the operating temperature range of –40°C to +125°C.

RELATED PRODUCTS

DESCRIPTION	DEVICE
Current and power monitor with watchdog, peak-hold, and fast comparator functions	INA209
Zerø-drift, low-cost, analog current shunt monitor series in small package	INA210, INA211, INA212, INA213, INA214
Zerø-drift, bidirectional current power monitor with two-wire interface	INA219
High or Low-side, bidirectional current and power monitor with two-wire interface and programmable alert	INA226

HIGH-OR LOW-SIDE SENSING



ELECTRICAL CHARACTERISTICS

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

PARAMETER		CONDITIONS	INA231			UNIT
			MIN	TYP	MAX	
SHUNT INPUT						
	Shunt voltage input range		-81.92		81.9175	mV
CMR	Common-mode rejection	V_{IN+} = 0 V to +28 V	100	120		dB
V_{OS}	Shunt offset voltage, RTI(1)			±10	±50	µV
		T_A = –40°C to +125°C		0.1	0.5	µV/°C
PSRR	vs power supply	V_S = +2.7 V to +5.5 V		10		µV/V
BUS INPUT						
	Bus voltage input range(2)		0		28	V
V_{OS}	Bus offset voltage, RTI(1)			±5	±30	mV
		T_A = –40°C to +125°C		10	40	µV/°C
PSRR	vs power supply			2		mV/V
	BUS pin input impedance			830		kΩ
INPUT						
I_{IN+}, I_{IN-}	Input bias current			10		µA
	Input leakage(3)	(V_{IN+}) + ($V_{IN–}$), Power-Down mode		0.1	0.5	µA
DC ACCURACY						
	ADC native resolution			16		Bits
	1 LSB step size	Shunt voltage		2.5		µV
		Bus voltage		1.25		mV
	Shunt voltage gain error			0.2	0.5	%
		T_A = –40°C to +125°C		10	50	ppm/°C
	Bus voltage gain error			0.2	0.5	%
		T_A = –40°C to +125°C		10	50	ppm/°C
	Differential nonlinearity			±0.1		LSB
	ADC conversion time	CT bit = 000		140	154	µs
		CT bit = 001		204	224	µs
		CT bit = 010		332	365	µs
		CT bit = 011		588	646	µs
		CT bit = 100		1.1	1.21	ms
		CT bit = 101		2.116	2.328	ms
		CT bit = 110		4.156	4.572	ms
		CT bit = 111		8.244	9.068	ms
SMBus						
	SMBus timeout(4)			28	35	ms
DIGITAL INPUT/OUTPUT						
	Input capacitance			3		pF
	Leakage input current	0 ≤ V_{IN} ≤ V_S		0.5	2	µA
V_{IH}	High-level input voltage		1.4		6	V
V_{IL}	Low-level input voltage		–0.5		0.4	V
V_{OL}	Low-level output voltage (SDA, ALERT)	I_{OL} = 3 mA	0		0.4	V
	Hysteresis			500		mV

(1) RTI = Referred-to-input.
(2) Although the input range is 28 V, the full-scale range of the ADC scaling is 40.96 V. Do not apply more than 28 V. See the *Basic Analog-to-Digital Converter (ADC) Functions* section for more details
(3) Input leakage is positive (current flowing into the pin) for the conditions shown at the top of this table. Negative leakage currents can occur under different input conditions.
(4) SMBus timeout in the INA231 resets the interface any time SCL is low for more than 28 ms.

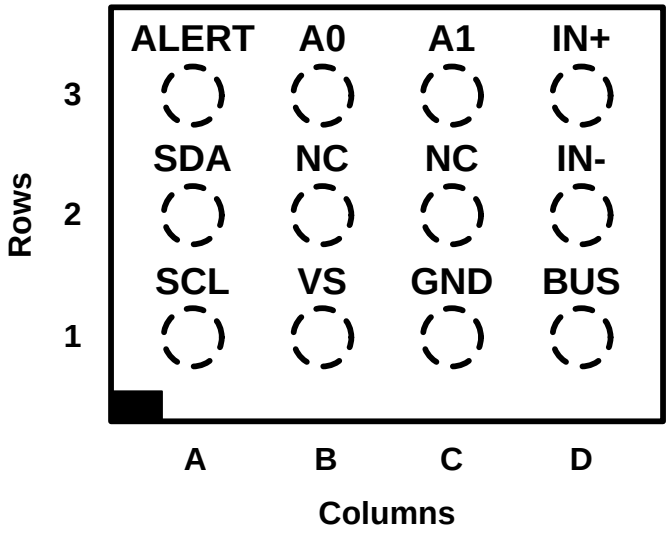
ELECTRICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

PARAMETER	CONDITIONS	INA231			UNIT
		MIN	TYP	MAX	
POWER SUPPLY					
Operating supply range		+2.7		+5.5	V
Quiescent current			330	420	µA
	Power-Down mode		3	7	µA
Power-on reset threshold			2		V
TEMPERATb5 /F1 z 0 0 0 rg 57 596.8 Td (TEM9 TI5E2I51 z 0 0 0 notCa2 7 Tf 4 0 Td (A)Tj ET BT /F2		**7 Tf 100 Tz520.47 0 Td (V,)Tj 11.21 0 Td (V)Tpecifie 0 0 30Tj 72.96 0 100**			

PIN CONFIGURATIONS

YFF PACKAGE
WCSP-12
(TOP VIEW)



PIN DESCRIPTIONS

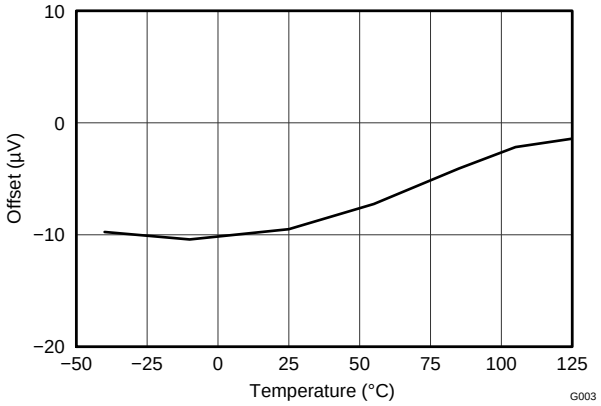
PIN		ANALOG/DIGITAL INPUT/OUTPUT	DESCRIPTION
NAME	NO.		
A0	B3	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 7 shows pin settings and corresponding addresses.
A1	C3	Digital input	Address pin. Connect to GND, SCL, SDA, or V_S. Table 7 shows pin settings and corresponding addresses.
ALERT	A3	Digital output	Multi-functional alert, open-drain output.
GND	C1	Analog	Ground
NC	B2, C2	—	No internal connection
SCL	A1	Digital input	Serial bus clock line, open-drain input.
SDA	A2	Digital input/output	Serial bus data line, open-drain input/output.
BUS	D1	Analog input	Bus voltage input
IN–	D2	Analog input	Negative differential shunt voltage input. Connect to load side of shunt resistor.
IN+	D3	Analog input	Positive differential shunt voltage input. Connect to supply side of shunt resistor.
V_S	B1	Analog	Power supply, 2.7 V to 5.5 V.

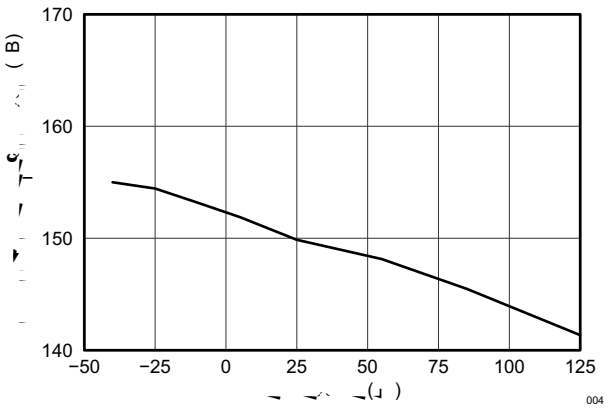
REGISTER BLOCK DIAGRAM

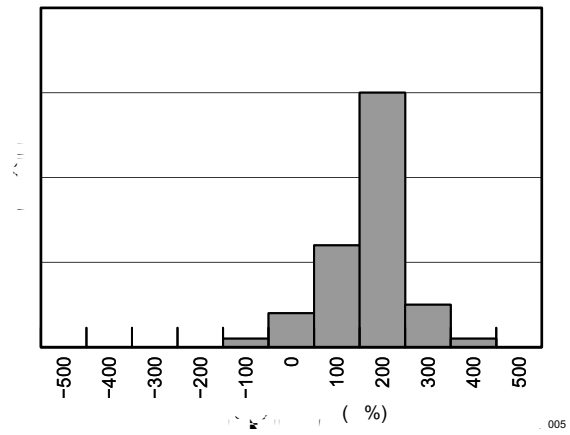
(1) Read-only

(2) Read/write

Figure 1. Register Block Diagram


10
0
−10
−20
Offset (µV)
−50
−25
0
25
50
75
100
125
Temperature (°C)
G003


170
160
150
140
(B)
−50
−25
0
25
50
75
100
125
004


−500
−400
−300
−200
−100
0
100
200
300
400
500
(%)
005

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

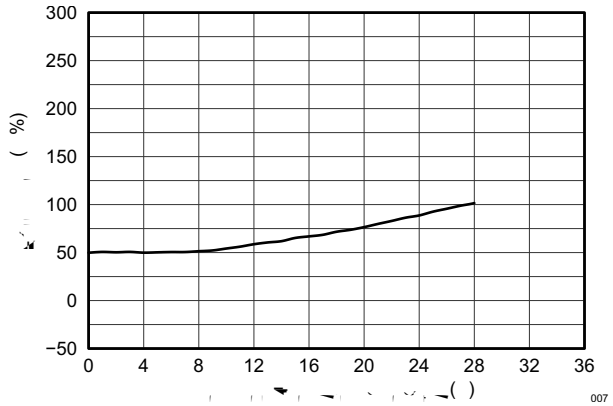


Figure 8. SHUNT INPUT GAIN ERROR vs COMMON-MODE VOLTAGE

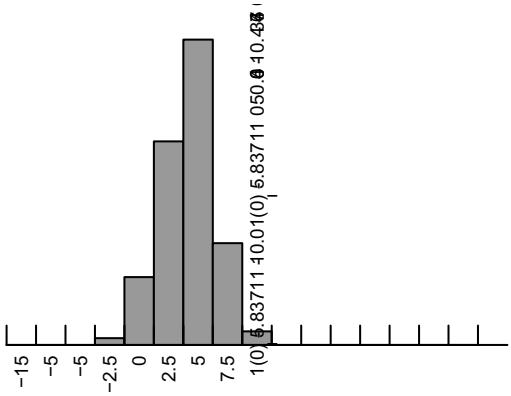


Figure 9. BUS INPUT OFFSET VOLTAGE PRODUCTION DISTRIBUTION

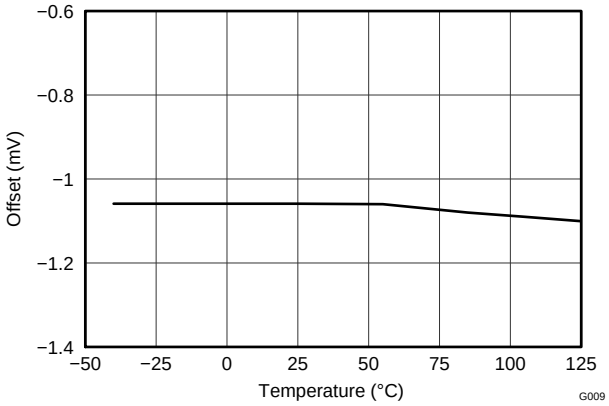


Figure 10. BUS INPUT OFFSET VOLTAGE vs TEMPERATURE

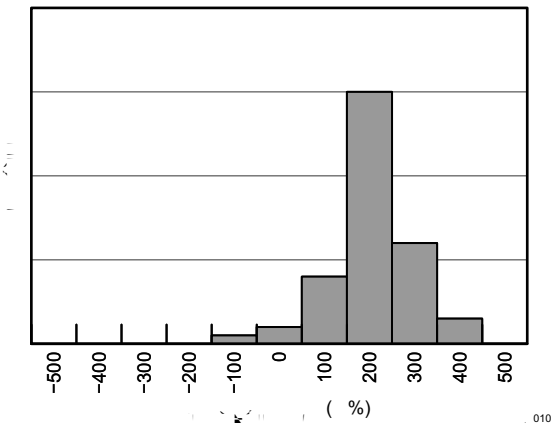


Figure 11. BUS INPUT GAIN ERROR PRODUCTION DISTRIBUTION

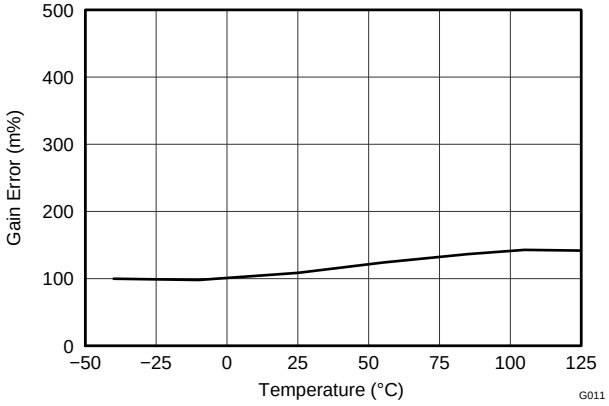


Figure 12. BUS INPUT GAIN ERROR vs TEMPERATURE

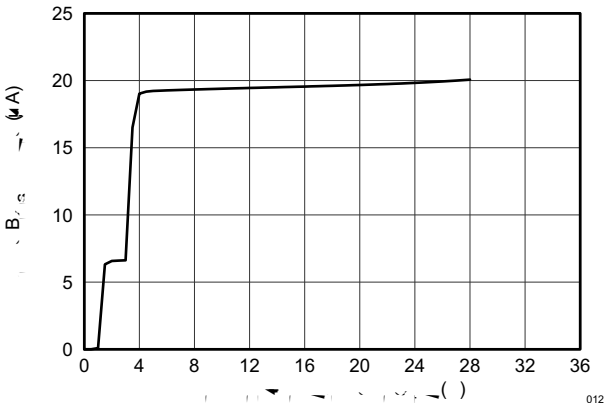


Figure 13. INPUT BIAS CURRENT vs COMMON-MODE VOLTAGE

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, V_S = +3.3 V, V_{IN+} = 12 V, V_{SENSE} = (V_{IN+} – $V_{IN–}$) = 0 mV, and V_{BUS} = 12 V, unless otherwise noted.

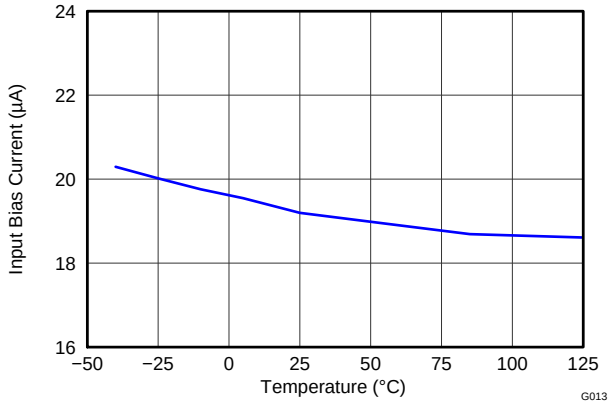


Figure 14. INPUT BIAS CURRENT vs TEMPERATURE

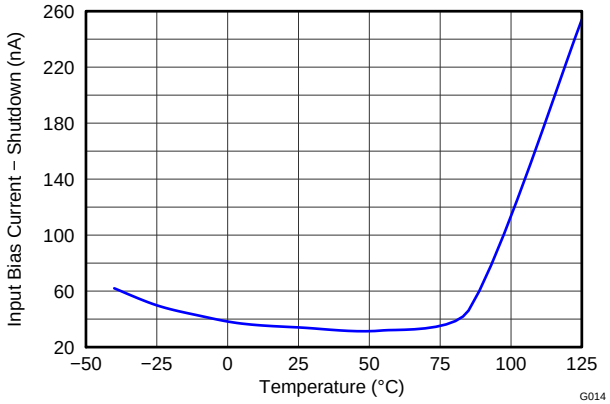


Figure 15. INPUT BIAS CURRENT vs TEMPERATURE, SHUTDOWN

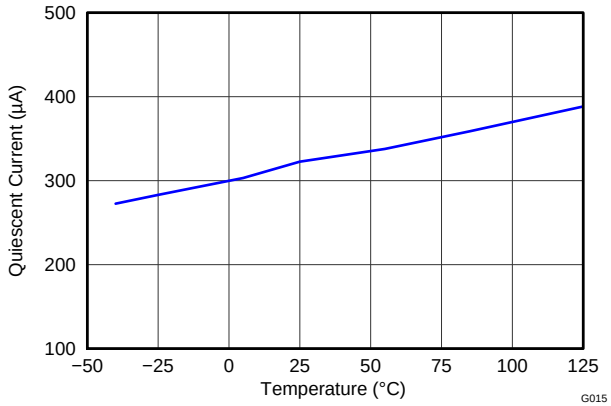


Figure 16. ACTIVE I_Q vs TEMPERATURE

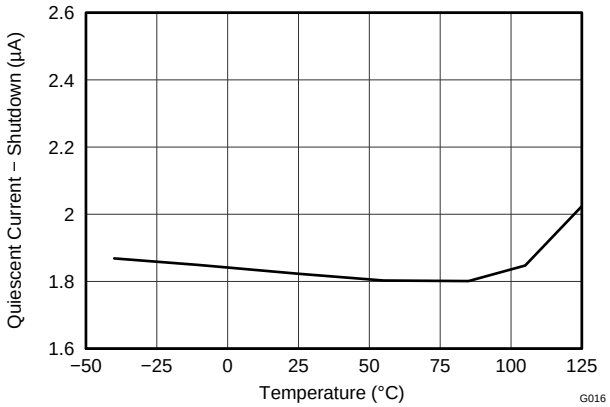


Figure 17. SHUTDOWN I_Q vs TEMPERATURE

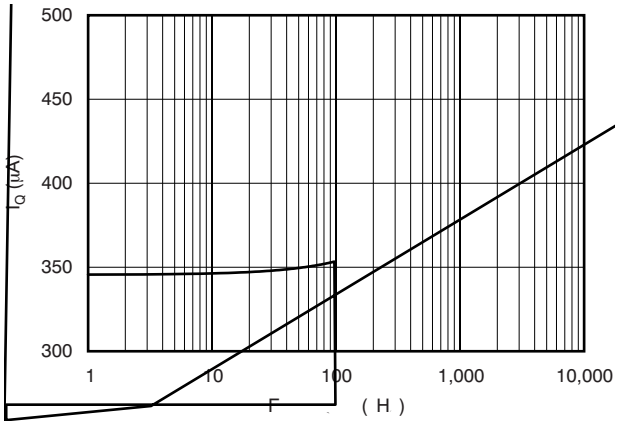


Figure 18. ACTIVE I_Q vs I^2C CLOCK FREQUENCY

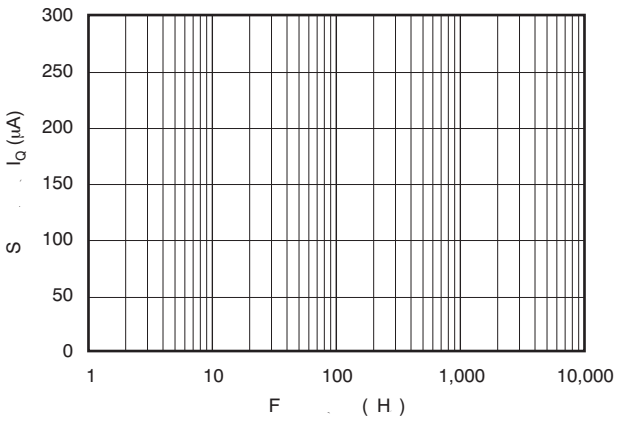


Figure 19. SHUTDOWN I_Q vs I^2C CLOCK FREQUENCY

APPLICATION INFORMATION

The INA231 is a digital current shunt monitor with an I^2C- and SMBus-compatible interface. This device provides digital current, voltage, and power readings necessary for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution, as well as continuous-versus-triggered operation. Detailed register information appears towards the end of this data sheet, beginning with Table 2. See Figure 1 for a block diagram of the INA231.

INA231 TYPICAL APPLICATION

The figure on the front page shows a typical application circuit for

In addition to the two operating modes (continuous and triggered), the INA231 also has a power-down mode that reduces the quiescent current and turns off current into the INA231 inputs, which reduces the impact of supply drain when the device is not being used. Full recovery from power-down mode requires 40 ms. The registers of the INA231 can be written to and read from while the device is in power-down mode. The device remains in power-down mode until one of the active modes settings are written into the Configuration register.

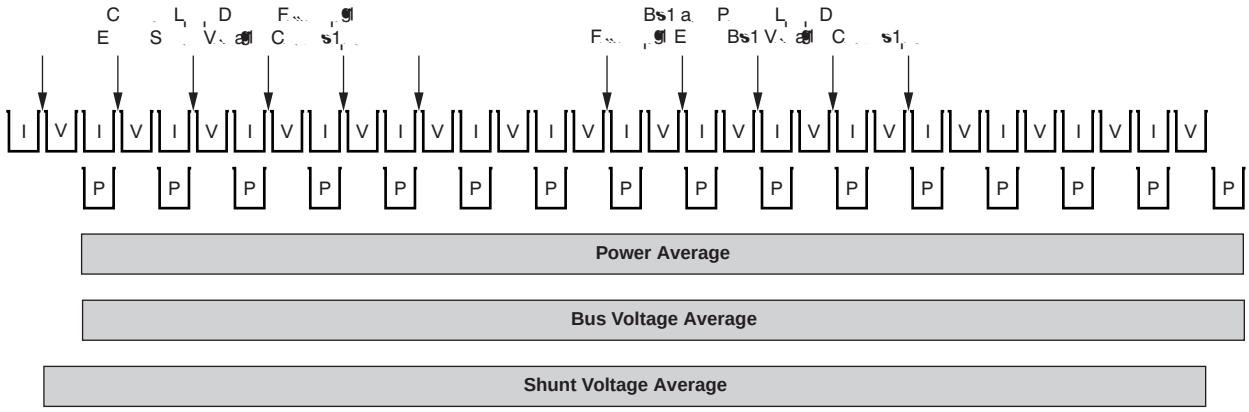
Although the INA231 can be read at any time, and the data from the last conversion remain available, the conversion ready flag bit (CVRF bit, Mask/Enable register) is provided to help coordinate single-shot or triggered conversions. The CVRF bit is set after all conversions, averaging, and multiplication operations are complete for a single cycle.

The CVRF bit clears under these conditions:

1. Writing to the Configuration register, except when configuring the MODE bits for power-down mode; or
2. Reading the Status register.

Power Calculation

The current and power are calculated after shunt voltage and bus voltage measurements, as shown in Figure 20. The current is calculated after a shunt voltage measurement based on the value set in the Calibration register. If there is no value loaded into the Calibration register, the current value stored is zero. Power is calculated following the bus voltage measurement based on the previous current calculation and bus voltage measurement. If there is no F



Averaging and Conversion Time Considerations

The INA231 has programmable conversion times for both the shunt voltage and bus voltage measurements. The conversion times for these measurements can be selected from as fast as 140 µs to as long as 8.244 ms. The conversion time settings, along with the programmable averaging mode, allow the INA231 to be configured to optimize the available timing requirements in a given application. For example, if a system requires that data be read every 5 ms, the INA231 can be configured with the conversion times set to 588 µs and the averaging mode set to 4. This configuration results in the data updating approximately every 4.7 ms. The INA231 can also be configured with a different conversion time setting for the shunt and bus voltage measurements. This type of approach is common in applications where the bus voltage tends to be relatively stable. This situation allows for the time spent measuring the bus voltage to be reduced relative to the shunt voltage measurement. The shunt voltage conversion time can be set to 4.156 ms with the bus voltage conversion time set to 588 µs, and the averaging mode set to 1. This configuration also results in data updating approximately every 4.7 ms.

There are trade-offs associated with the conversion time settings and the averaging mode used. The averaging feature can significantly improve the measurement accuracy by effectively filtering the signal. This approach allows the INA231 to reduce noise in the measurement that may be caused by noise coupling into the signal. A greater number of averages enables the INA231 to be more effective in reducing the noise component of the measurement.

The conversion times selected can also have an impact on the measurement accuracy; this effect can be seen in Figure 21. Multiple conversion times are shown to illustrate the impact of noise on the measurement. In order to achieve the highest accuracy measurement possible, use a combination of the longest allowable conversion times and highest number of averages, based on the timing requirements of the system.

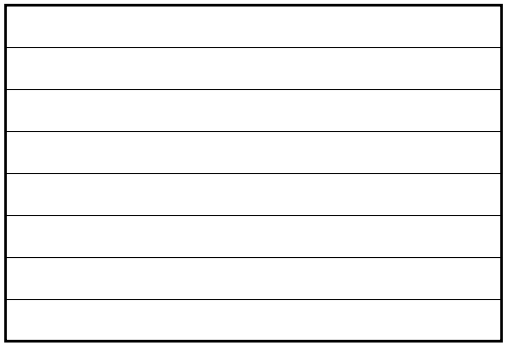
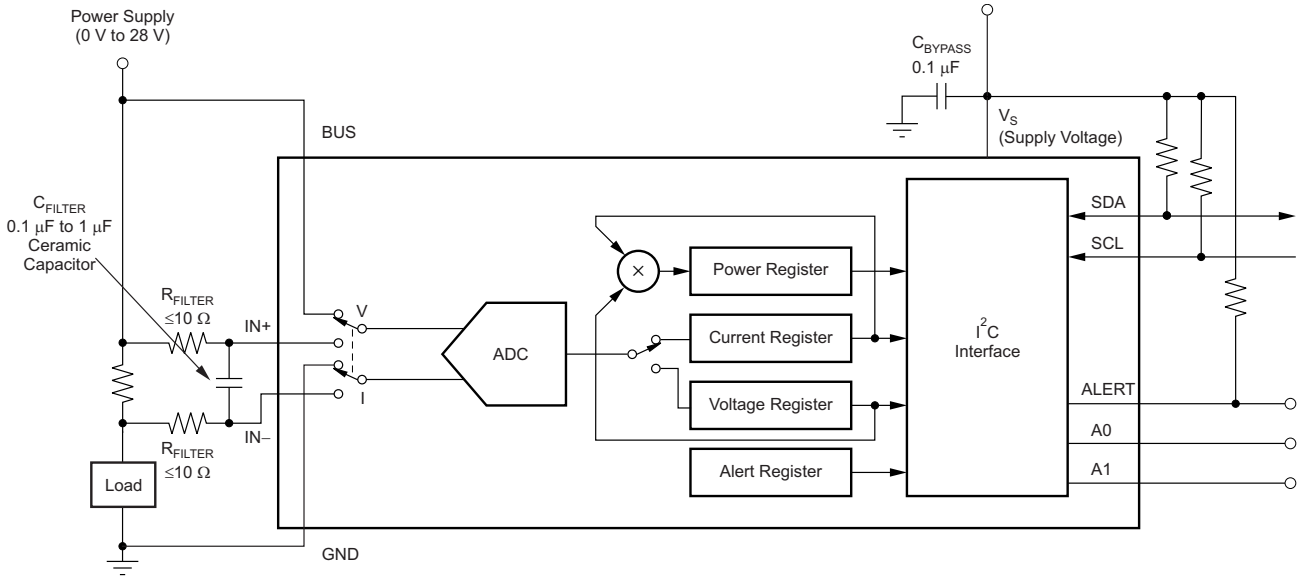


Figure 21. Noise vs Conversion Time

Filtering and Input Considerations

Measuring current is often a noisy task, and such noise can be difficult to define. The INA231 offers several options for filtering by allowing the conversion times and number of averages to be independently selected in the Configuration register. The conversion times can be independently set for the shunt voltage and bus voltage



ALERT PIN

The INA231 has a single Alert Limit register (07h) that allows the ALERT pin to be programmed to respond to a single user-defined event or to a conversion ready notification if desired. The Mask/Enable register allows for selecton from one of the five available functions to monitor and set the conversion ready bit (CNVR, Mask/Enable register) to control the response of the ALERT pin. Based on the function being monitored, a value would then be entered into the Alert Limit register to set the corresponding threshold value that asserts the ALERT pin.

The ALERT pin allows for one of several available alert functions to be monitored to determine if a user-defined threshold has been exceeded. The five alert functions that can be monitored are:

- Shunt voltage overlimit (SOL)
- Shunt voltage underlimit (SUL)
- Bus voltage overlimit (BOL)
- Bus voltage underlimit (BUL)
- Power overlimit (POL)

The ALERT pin is an open-drain output. This pin is asserted when the alert function selected in the Mask/Enable register exceeds the value programmed into the Alert Limit register. Only one of these alert functions can be enabled and monitored at a time. If multiple alert functions are enabled, the selected function in the highest significant bit position takes priority and responds to the Alert Limit register value. For example, if the SOL and the SUL are both selected, the ALERT pin asserts when the Shunt Voltage Over Limit register exceeds the value in the Alert Limit register.

The conversion-ready state of the device can also be monitored at the ALERT pin to inform the user when the device has completed the previous conversion and is ready to begin a new conversion. The conversion ready flag (CVRF) bit can be monitored at the ALERT pin along with one of the alert functions. If an alert function and the CNVR bit are both enabled for monitoring at the ALERT pin, then after the ALERT pin is asserted, the CVRF bit (D3) and the AFF bit (D4) in the Mask/Enable register must be read following the alert to determine the source of the alert. If the conversion ready feature is not desired, and the CNVR bit is not set, the ALERT pin only responds to an exceeded alert limit based on the alert function enabled.

If the alert function is not used, the ALERT pin can be left floating without impacting the operation of the device.

Refer to Figure 20 to see the relative timing of when the value in the Alert Limit register is compared to the corresponding converted value. For example, if the alert function that is enabled is Shunt Voltage Over Limit (SOL), following every shunt voltage conversion the value in the Alert Limit register is compared to the measured shunt voltage to determine if the measurements have exceeded the programmed limit. The AFF bit (D4, Mask/Enable register) asserts high any time the measured voltage exceeds the value programmed into the Alert Limit register. In addition to the AFF bit being asserted, the ALERT pin is asserted based on the Alert Polarity bit (APOL, D1, Mask/Enable register). If the Alert Latch is enabled, the AFF bit and ALERT pin remain asserted until either the Configuration register is written to or the Mask/Enable register is read.

The bus voltage alert functions (BOL and BUL, Mask/Enable register) compare the measured bus voltage to the Alert Limit register following every bus voltage conversion and assert the AFF bit and ALERT pin if the limit threshold is exceeded.

The power overlimit alert function (POL, Mask/Enable Regsiter) is also compared to the calculated power value following every bus voltage measurement conversion and asserts the AFF bit and ALERT pin if the limit threshold is exceeded.

The alert function compares the programmed alert limit value to the result of each corresponding conversion. Therefore, an alert can be issued during a conversion cycle where the averaged value of the signal does not exceed the alert limit. Triggering an alert based on this intermediate conversion allows for out-of-range events to be detected faster than the averaged output data registers are updated. This fast detection can be used to create alert limits for quickly changing conditions through the use of the alert function, as well as to create limits to longer-duration conditions through software monitoring of the averaged output values.

PROGRAMMING THE INA231

An important aspect of the INA231 is that it does not necessarily measure current or power. The INA231 measures both the differential voltage applied between the IN+ and IN– input pins and the voltage applied to the BUS pin. In order for the INA231 to report both current and power values, both the Current register resolution and the value of the shunt resistor present in the application that resulted in the differential voltage being developed must be programmed. The Power register is internally set to be 25 times the programmed least significant bit of the Current register (Current_LSB). Both the Current_LSB and shunt resistor value are used when calculating the Calibration register value. The INA231 uses this value to calculate the corresponding current and power values based on the measured shunt and bus voltages.

The Calibration register is calculated based on Equation 1. This equation includes the term Current_LSB, the programmed value for the LSB for the Current register. This is the value used to convert the value in the Current register to the actual current in amps. The highest resolution for the Current register can be obtained by using the smallest allowable Current_LSB based on the maximum expected current, as shown in Equation 2. While this value yields the highest resolution, it is common to select a value for the Current_LSB to the nearest round number above this value to simplify the conversion of the Current register and Power register to amps and watts, respectively. R_{SHUNT} is the value of the external shunt used to develop the differential voltage across the input pins. The 0.00512 value in Equation 1 is an internal fixed value used to ensure scaling is maintained properly.

$$CAL = \frac{0.00512}{Current\_LSB \bullet R_{SHUNT}} \quad (1)$$

$$C\_LSB = \frac{Ma + E + C}{2^{15}} \quad (2)$$

After the Calibration register has been programmed, the Current register and Power register are updated accordingly based on the corresponding shunt voltage and bus voltage measurements. Until the Calibration register is programmed, the Current and Power registers remain at zero.

CONFIGURE/MEASURE/CALCULATE EXAMPLE

In this example, shown in Figure 23, a nominal 10-A load creates a differential voltage of 20 mV across a 2-mΩ shunt resistor. The bus voltage for the INA231 is measured at the external BUS input pin; in this example, BUS is connected to the IN– pin to measure the voltage level delivered to the load. For this example, the BUS pin measures less than 12 V because the voltage at the IN– pin is 11.98 V as a result of the voltage drop across the shunt resistor.

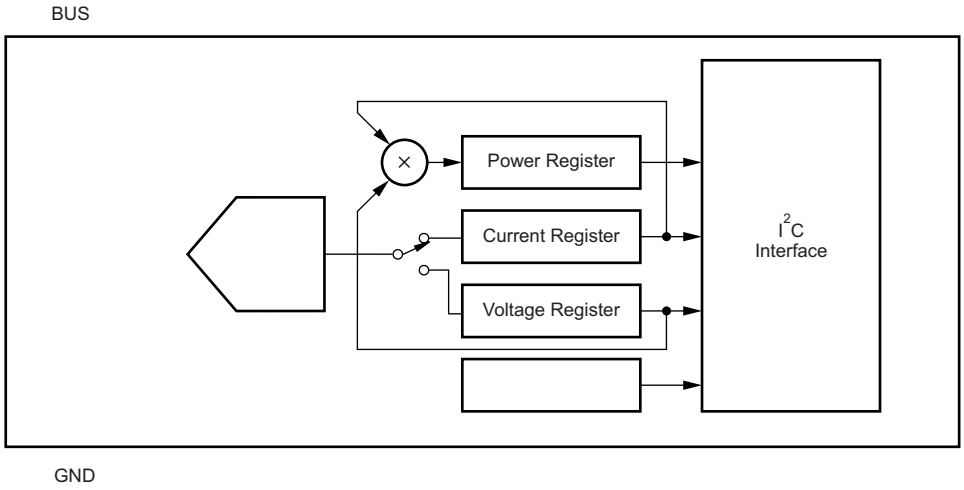


Figure 23. Example Circuit Configuration

For this example, assuming a maximum expected current of 15 A, the Current_LSB is calculated to be 457.7 µA/bit using Equation 2. Using a value of 500 µA/bit or 1 mA/bit for the Current_LSB significantly simplifies the conversion from the Current register and Power register to

$$\text{Current} = \frac{\text{ShuntVoltage} \bullet \text{CalibrationRegister}}{2048}$$

The Power register (03h) is then calculated by multiplying the decimal value of the Current register, 10000, by the decimal value of the Bus Voltage register, 9584, and then dividing by 20,000, as defined in Equation 4. For this example, the result for the Power register is 12B8h, or a decimal equivalent of 4792. Multiplying this result by the power LSB (25 times the [1 × 10^{-3} Current_LSB]) results in a power calculation of (4792 × 25 mW/bit), or 119.8 W. The Power register LSB has a fixed ratio to the Current register LSB of 25 W/bit to 1 A/bit. For this example, a programmed Current register LSB of 1 mA/bit results in a Power register LSB of 25 mW/bit. This ratio is internally programmed to ensure that the scaling of the power calculation is within an acceptable range. A manual calculation for the power being delivered to the load would use a bus voltage of 11.98 V ($12V_{CM}$ – 20 mV shunt drop) multiplied by the load current of 10 A to give a result of 119.8 W.

$$\text{Power} = \frac{\text{Current} \bullet \text{BusVoltage}}{20{,}000} \tag{4}$$

Table 1 shows the steps for configuring, measuring, and calculating the values for current and power for this device.

Table 1. Configure, Measure. and Calculate Example(1)

STEP #	REGISTER NAME	ADDRESS	CONTENTS	DEC	LSB	VALUE
Step 1	Configuration	00h	4127h	—	—	—
Step 2	Shunt	01h	1F40h	8000	2.5 µV	20m V
Step 3	Bus	02h	2570h	9584	1.25 mV	11.98 V
Step 4	Calibration	05h	A00h	2560	—	—
Step 5	Current	04h	2710h	10000	1 mA	10 A
Step 6	Power	03h	12B8h	4792	25 mW	119.8 W

(1) Conditions: Load = 10 A, V_{CM} = 12 V, R_{SHUNT} = 2 mΩ, and V_{BUS} =11.98 V.

PROGRAMMING THE INA231 POWER MEASUREMENT ENGINE

Calibration Register and Scaling

The Calibration register makes it possible to set the scaling of the Current and Power registers to the values that are most useful for a given application. One strategy may be to set the Calibration register so that the largest possible number is generated in the Current register or Power register at the expected full-scale point. This approach yields the highest resolution based on the previously-calculated minimum Current_LSB in the equation for the Calibration register (Equation 1). The Calibration register can also be selected to provide values in the Current and Power registers that either provide direct decimal equivalents of the values being measured, or yield a round LSB value for each corresponding register. After these choices have been made, the Calibration register also offers possibilities for Equation 0.0 Tdwme3f 100 Tz 0 0 0 rg 5472 10 Tf 100sy4 0m-level8 0 Td 0 Td (of)Tj sat

Corrected_Full_Scale_Cal = trunc Cal MeasShu_ 2 d 11

Simple Current Shunt Monitor Usage (No Programming Necessary)

The INA231 does not require programming to read a shunt voltage drop and the bus voltage when using the default power-on reset configuration and running continuous conversions of the shunt and bus voltage.

Without programming the INA231 Calibration register, the device is unable to provide either a valid current or power value because these outputs are both derived using the values loaded into the Calibration register.

Default INA231 Settings

The default power-up states of the registers are shown in the *Register Details* section of this data sheet. These registers are volatile, and if programmed to a value other than the default values shown in Table 2, they must be reprogrammed at every device power-up. Detailed information on programming the Calibration register is given in the *Configure/Measure/Calculate Example* section and calculated based on Equation 1.

REGISTER INFORMATION

The INA231 uses a bank of registers for holding configuration settings, measurement results, minimum/maximum limits, and status information. Table 2 summarizes the INA231 registers; refer to Figure 1 for an illustration of the registers.

Table 2. Summary of Register Set

POINTER ADDRESS			POWER-ON RESET		
HEX	REGISTER NAME	FUNCTION	BINARY	HEX	TYPE(1)
00	Configuration	This register resets all registers and controls shunt voltage and bus voltage, ADC conversion times and averaging, as well as the device operating mode.	01000001 00100111	4127	R/$\overline{W}$
01	Shunt Voltage	Shunt voltage measurement data	00000000 00000000	0000	R
02	Bus Voltage	Bus voltage measurement data	00000000 00000000	0000	R
03	Power(2)	This register contains the value of the calculated power being delivered to the load.	00000000 00000000	0000	R
04	Current(2)	This register contains the value of the calculated current flowing through the shunt resistor.	00000000 00000000	0000	R
05	Calibration	This register sets the full-scale range and LSB of the current and power measurements. This register sets the overall system calibration.	00000000 00000000	0000	R/$\overline{W}$
06	Mask/Enable	This register sets the alert configuration and conversion ready flag.	00000000 00000000	0000	R/$\overline{W}$
07	Alert Limit	This register contains the limit value to compare to the selected alert function.	00000000 00000000	0000	R/$\overline{W}$

(1) Type: R = read-only, R/$\overline{W}$ = read/write.
(2) The Current register defaults to '0' because the Calibration register defaults to '0', yielding a zero current and power value until the Calibration register is programmed.

REGISTER DETAILS

All 16-bit INA231 registers are two 8-bit bytes via the I^2C interface.

Configuration Register (00h, Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	—	—	AVG2	AVG1	AVG0	V_{BUS}CT2	V_{BUS}CT1	V_{BUS}CT0	V_{SH}CT2	V_{SH}CT1	V_{SH}CT0	MODE3	MODE2	MODE1
POR VALUE	0	1	0	0	0	0	0	1	0	0	1	0	0	1	1	1

The Configuration register settings control the operating modes for the INA231. This register controls the conversion time settings for both the shunt and bus voltage measurements, as well as the averaging mode used. The operating mode that controls which signals are selected to be measured is also programmed in the Configuration register.

The Configuration register can be read from at any time without impacting or affecting the device settings or a conversion in progress. Writing to the Configuration register halts any conversion in progress until the write sequence is complete, resulting in the start of a new conversion based on the new contents of the Configuration register. This feature prevents any uncertainty in the conditions used for the next completed conversion.

Bit Descriptions

RST: **Reset Bit**

Bit 15 Setting this bit to '1' generates a system reset that is the same as a power-on reset; all registers are reset to default values. This bit self-clears.

AVG: **Averaging Mode**

Bits 9–11 These bits set the number of samples that are collected and averaged together. Table 3 summarizes the AVG bit settings and related number of averages for each bit.

Table 3. AVG Bit Settings [11:9](1)

AVG2 (D11)	AVG1 (D10)	AVG0 (D9)	NUMBER OF AVERAGES
0	0	0	1
0	0	1	4
0	1	0	16
0	1	1	64
1	0	0	128
1	0	1	256
1	1	0	512
1	1	1	1024

(1) Shaded values are default.

V_{BUS} CT: **Bus Voltage Conversion Time**

Bits 6–8

These bits set the conversion time for the bus voltage measurement. Table 4 shows the V_{BUS} CT bit options and related conversion times for each bit.

Table 4. V_{BUS} CT Bit Settings [8:6](1)

V_{BUS} CT2 (D8)	V_{BUS} CT1 (D7)	V_{BUS} CT0 (D6)	CONVERSION TIME
0	0	0	140 µs
0	0	1	204 µs
0	1	0	332 µs
0	1	1	588 µs
1	0	0	1.1 ms
1	0	1	2.116 ms
1	1	0	4.156 ms
1	1	1	8.244 ms

(1) Shaded values are default.

V_{SH} CT: **Shunt Voltage Conversion Time**

Bits 3–5

These bits set the conversion time for the shunt voltage measurement. Table 5 shows the V_{SH} CT bit options and related conversion times for each bit.

Table 5. V_{SH} CT Bit Settings [5:3](1)

V_{SH} CT2 (D5)	V_{SH} CT1 (D4)	V_{SH} CT0 (D3)	CONVERSION TIME
0	0	0	140 µs
0	0	1	204 µs
0	1	0	332 µs
0	1	1	588 µs
1	0	0	1.1 ms
1	0	1	2.116 ms
1	1	0	4.156 ms
1	1	1	8.244 ms

(1) Shaded values are default.

MODE: **Operating Mode**

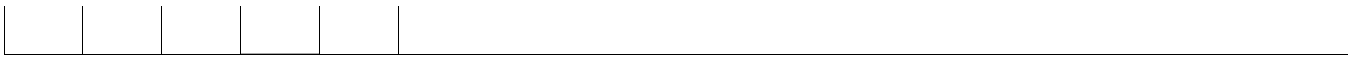
Bits 0–2

These bits select continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in Table 6.

Table 6. Mode Settings [2:0](1)

MODE3 (D2)	MODE2 (D1)	MODE1 (D0)	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	Power-down
1	0	1	Shunt voltage, continuous
1	1	0	Bus voltage, continuous
1	1	1	Shunt and bus, continuous

(1) Shaded values are default.



Current Register (04h, Read-Only)

If averaging is enabled, this register displays the averaged value.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value of the Current register is calculated by multiplying the decimal value in the Shunt Voltage register with the decimal value of the Calibration register, according to Equation 3.

Calibration Register (05h, Read/Write)

This register provides the INA231 with the shunt resistor value that was present to create the measured differential voltage. This register also sets the resolution of the Current register. The Current register LSB and Power register LSB are set through the programming of this register. This register is also used for overall system calibration. See the Configure/Measure/Calculate Example for more information on programming this register.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	—	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Mask/Enable Register (06h, Read/Write)

The Mask/Enable register selects the function that controls the ALERT pin, as well as how that pin functions. If multiple functions are enabled, the highest significant bit position alert function (D15:D11) takes priority and responds to the Alert Limit register.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SOL	SUL	BOL	BUL	POL	CNVR	—	—	—	—	—	AFF	CVRF	OVF	APOL	LEN
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SOL: **Shunt Voltage Over-Voltage**

Bit 15 Setting this bit high configures the ALERT pin to be asserted when the shunt voltage conversion exceeds the value in the Alert Limit register.

SUL: **Shunt Voltage Under-Voltage**

Bit 14 Setting this bit high configures the ALERT pin to be asserted when the shunt voltage conversion drops below the value in the Alert Limit register.

BOL: **Bus Voltage Over-Voltage**

Bit 13 Setting this bit high configures the ALERT pin to be asserted when the bus voltage conversion exceeds the value in the Alert Limit register.

BUL: **Bus Voltage Under-Voltage**

Bit 12 Setting this bit high configures the ALERT pin to be asserted when the bus voltage conversion drops below the value in the Alert Limit register.

POL: **Over-Limit Power**

Bit 11 Setting this bit high configures the ALERT pin to be asserted when the power calculation exceeds the value in the Alert Limit register.

CNVR:	**Conversion Ready**
Bit 10	Setting this bit high configures the ALERT pin to be asserted when the Conversion Ready Flag bit (CVRF, bit 3) is asserted, indicating that the device is ready for the next conversion.
AFF:	**Alert Function Flag**
Bit 4	Although only one alert function at a time can be monitored at the ALERT pin, the Conversion Ready bit (CNVR, bit 10) can also be enabled to assert the ALERT pin. Reading the Alert Function Flag bit after an alert can help determine if the alert function was the source of the alert. When the Alert Latch Enable bit is set to Latch mode, the Alert Function Flag bit clears only when the Mask/Enable register is read. When the Alert Latch Enable bit is set to Transparent mode, the Alert Function Flag bit is cleared after the next conversion that does not result in an alert condition.
CVRF:	**Conversion Ready Flag**
Bit 3	Although the INA231 can be read at any time, and the data from the last conversion are available, this bit is provided to help coordinate single-shot or triggered conversions. This bit is set after all conversions, averaging, and multiplications are complete. This bit clears under the following conditions in single-shot mode: 1) Writing to the Configuration register (except for power-down or disable selections) 2.) Reading the Mask/Enable register
OVF:	**Math Overflow Flag**
Bit 2	This bit is set to '1' if an arithmetic operation results in an overflow error; it indicates that current and power data may be invalid.
APOL:	**Alert Polarity**
Bit 1	Configures the latching feature of the ALERT pin and the flag bits. 1 = Inverted (active-high open collector) 0 = Normal (active-low open collector) (default)
LEN:	**Alert Latch Enable**
Bit 0	Configures the latching feature of the ALERT pin and flag bits. 1 = Latch enabled 0 = Transparent (default) When the Alert Latch Enable bit is set to Transparent mode, the ALERT pin and flag bits reset to their idle states when the fault has been cleared. When the Alert Latch Enable bit is set to Latch mode, the ALERT pin and flag bits remain active following a fault until the Mask/Enable register has been read.

Alert Limit Register (07h, Read/Write)

The Alert Limit register contains the value used to compare to the register selected in the Mask/Enable register to determine if a limit has been exceeded.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	AUL15	AUL14	AUL13	AUL12	AUL11	AUL10	AUL9	AUL8	AUL7	AUL6	AUL5	AUL4	AUL3	AUL2	AUL1	AUL0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

BUS OVERVIEW

The INA231 offers compatibility with both I^2C and SMBus interfaces. The I^2C and SMBus protocols are essentially compatible with one another.

The I^2C interface is used throughout this data sheet as the primary example, with SMBus protocol specified only when a difference between the two systems is discussed. Two bidirectional lines, SCL and SDA, connect the INA231 to the bus. Both SCL and SDA are open-drain connections.

The device that initiates a data transfer is called a *master*, and the devices controlled by the master are *slaves*. The bus must be controlled by a master device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions.

To address a specific device, the master initiates a start condition by pulling the data signal line (SDA) from a high to a low logic level while SCL is high. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an *Acknowledge* bit (ACK) and pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an ACK. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition.

After all data have been transferred, the master generates a stop condition indicated by pulling SDA from low to high while SCL is high. The INA231 includes a 28-ms timeout on its interface to prevent locking up the bus.

Serial Bus Address

In order to communicate with the INA231, the master must first address slave devices using a corresponding slave address byte. The slave address byte consists of seven address bits and a direction bit that indicates whether the action is to be a read or write operation.

The INA231 has two address pins: A0 and A1. Table 7 describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication. Set these pins before any activity on the interface occurs.

Table 7. INA231 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V_S	1000001
GND	SDA	1000010
GND	SCL	1000011
V_S	GND	1000100
V_S	V_S	1000101
V_S	SDA	1000110
V_S	SCL	1000111
SDA	GND	1001000
SDA	V_S	

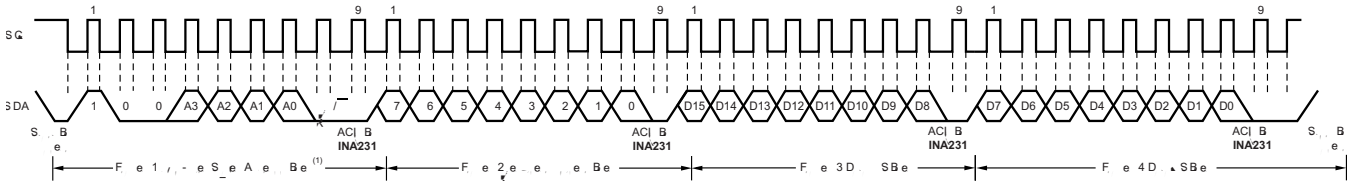
WRITING TO/READING FROM THE INA231

Accessing a specific register on the INA231 is accomplished by writing the appropriate value to the register pointer. Refer to Table 2 for a complete list of registers and corresponding addresses. The value for the register pointer (shown in Figure 27) is the first byte transferred after the slave address byte with the R/$\overline{W}$ bit low. Every write operation to the INA231 requires a value for the register pointer.

Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/$\overline{W}$ bit low. The INA231 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register that data are written to. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The INA231 acknowledges receipt of each data byte. The master may terminate data transfer by generating a start or stop condition.

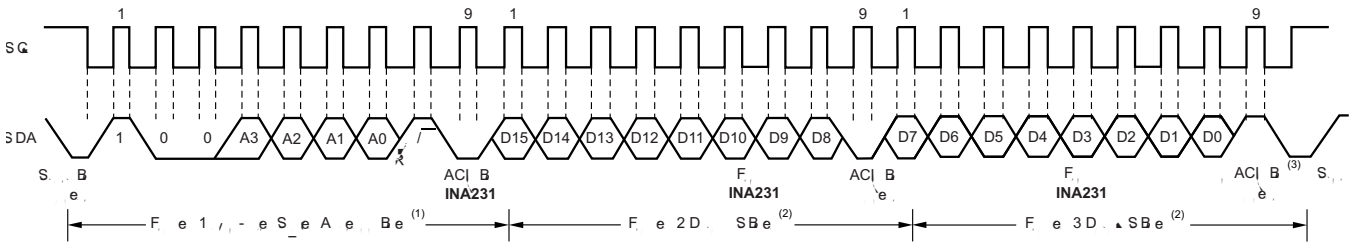
When reading from the INA231, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/$\overline{W}$ bit low, followed by the register pointer byte. No additional data are required. The master then generates a start condition and sends the slave address byte with the R/$\overline{W}$ bit high to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an ACK from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a *Not-Acknowledge* bit (No ACK) after receiving any data byte, or generating a start or stop condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the INA231 retains the register pointer value until it is changed by the next write operation.

Figure 24 and Figure 25 show the write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte.



(1) The value of the slave address byte is determined by the settings of the A0 and A1 pins. Refer to Table 7.

Figure 24. Timing Diagram for Write Word Format



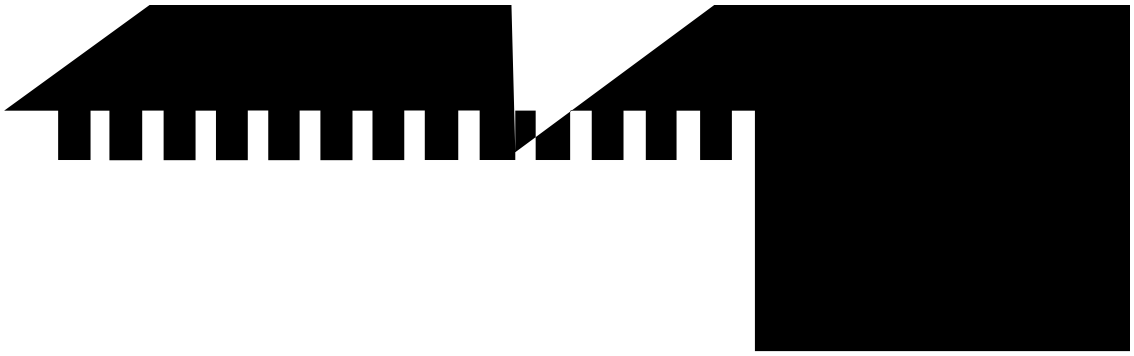
(1) The value of the slave address byte is determined by the settings of the A0 and A1 pins. Refer to Table 7.

(2) Read data are from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 27.

(3) ACK by Master can also be sent.

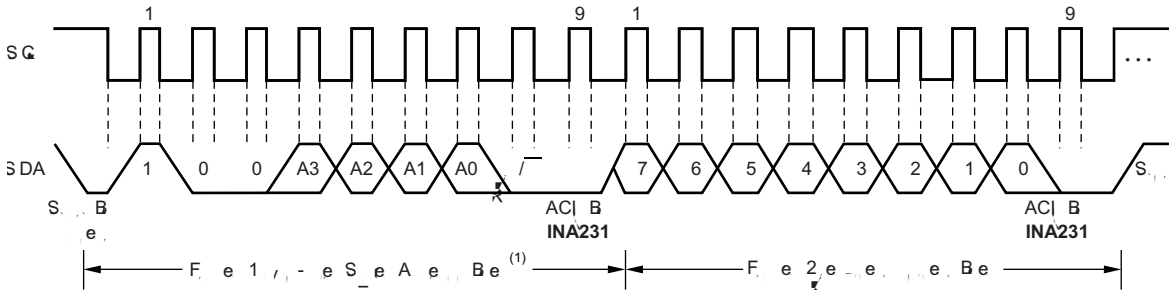
Figure 25. Timing Diagram for Read Word Format

Figure 26 shows the timing diagram for the SMBus alert response operation. Figure 27 illustrates a typical register pointer configuration.



(1) The slave address byte value is determined by the settings of the A0 and A1 pins. Refer to Table 7.

Figure 26. Timing Diagram for SMBus Alert



(1) The slave address byte value is determined by the settings of the A0 and A1 pins. Refer to Table 7.

Figure 27. Typical Register Pointer Set

SMBus Alert Response

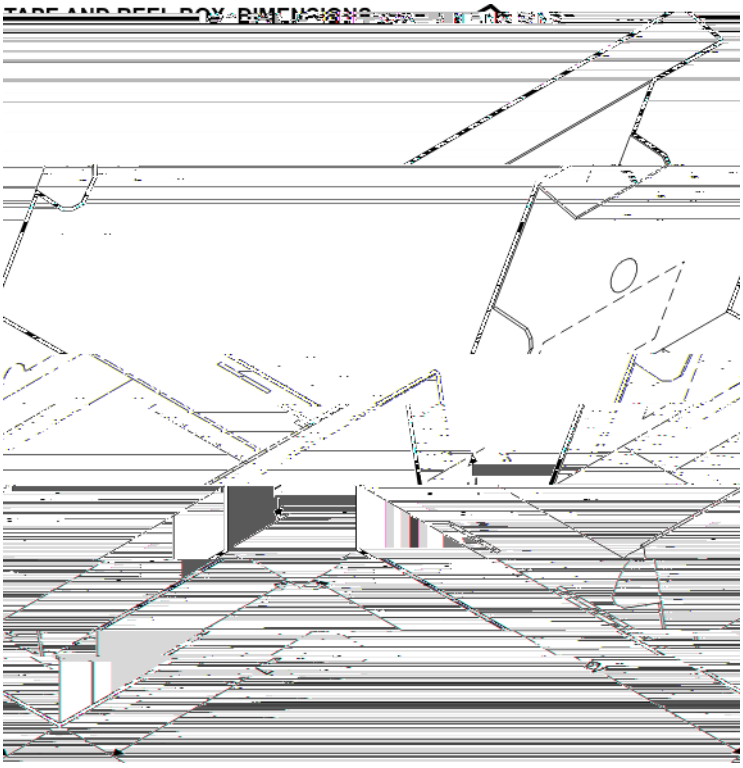
The INA231 is designed to respond to the SMBus alert response address. The SMBus alert response provides a quick fault identification for simple slave devices. When an alert occurs, the master can broadcast the alert response slave address (0001 100) with the Read/Write bit set high. Following this alert response, any slave devices that generated an alert identify themselves by acknowledging the alert response and sending their respective address on the bus.

The alert response can activate several different slave devices simultaneously, similar to the I^2C general call. If more than one slave attempts to respond, bus arbitration rules apply. The losing device does not generate an acknowledge and continues to hold the ALERT line low until the interrupt is cleared.

TAPE AND REEL INFORMATION

*All dimensions are nominal

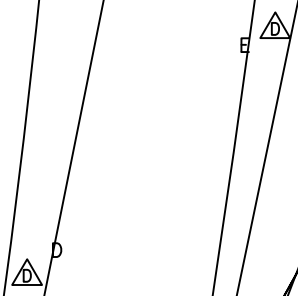
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA231AIYFFR	DSBGA	YFF	12	3000	180.0	8.4	1.48	1.78	0.69	4.0	8.0	Q1
INA231AIYFFT	DSBGA	YFF	12	250	180.0	8.4	1.48	1.78	0.69	4.0	8.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA231AIYFFR	DSBGA	YFF	12	3000	210.0	185.0	35.0
INA231AIYFFT							

YFF (R-XBGA-N12) DIE-SIZE BALL GRID ARRAY



D: Max = 1.675 mm, Min =1.614 mm

E: Max = 1.418 mm, Min =1.358 mm

4207625-7/AK 11/12

A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. Thi
C. NanoFree package configuration.

E. Reference Product Data Sheet for array population.
3 x 4 matrix pattern is shown for illustration only.
F. This package contains Pb-free balls.

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