AOZ1310

Single Channel USB Switch

General Description

The AOZ1310 is a member of Alpha and Omega Semiconductor's single-channel power-distribution switch family intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. This device incorporates a 70 mΩ N-channel MOSFET power switch for power-distribution systems. The switch is controlled by a logic enable input. Gate drive is provided by an internal charge pump designed to control the power-switch rise time and fall time to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

The AOZ1310 is available in an SOT23-5 package and is rated over the -40 °C to +85 °C ambient temperature range.

Features

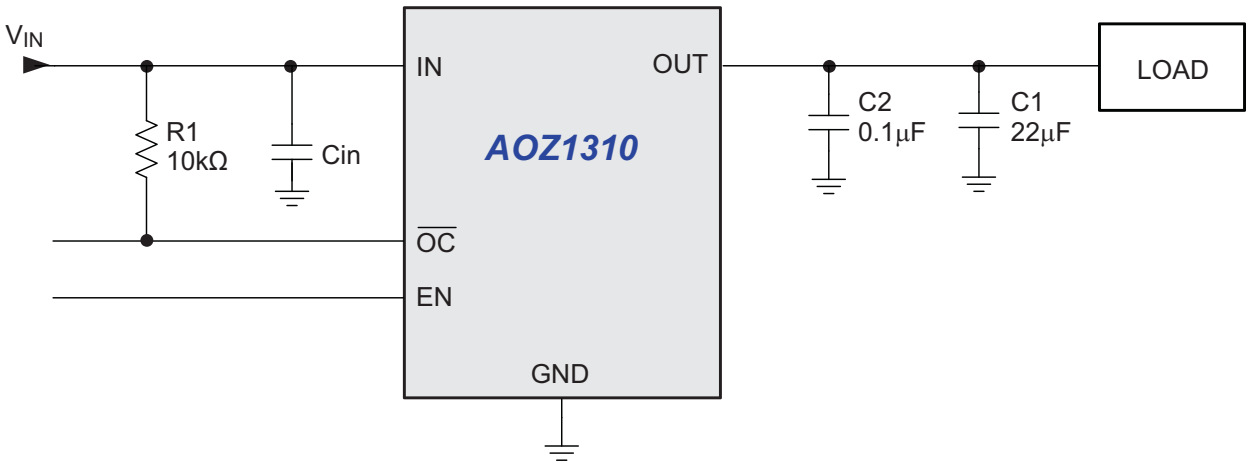
- Typical 80 mΩ (NFET)
- 0.5A maximum continuous current
- Vin range of 2.7 V to 5.5 V
- Open Drain Fault Flag
- Fault Flag deglitched (blanking time)
- Thermal shutdown
- Reverse current blocking
- Package: SOT23-5

Applications

- Notebook Computers
- Desktop Computers

Green Product

Typical Application



Ordering Information

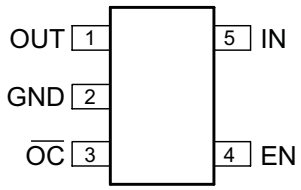
Part Number	Maximum Continuous Current		Typical Short-circuit Current Limit		Enable Setting	Package	Output Discharge	Environmental
	Channel 1	Channel 2	Channel 1	Channel 2				
AOZ1341AI	1 A	1A	1.5 A	1.5 A	Active Low	SO-8	No	Green Product RoHS Compliant
AOZ1341EI						EPAD MSOP-8		
AOZ1341AI-1					Active High	SO-8		
AOZ1341EI-1						EPAD MSOP-8		
AOZ1342PI	1.5 A	1.5A	2 A	2 A	Active Low	EPAD SO-8		
AOZ1342PI-1					Active High	EPAD SO-8		
AOZ1343AI*	1.5 A	0.5A	2 A	0.75 A	Active Low	SO-8		
AOZ1343EI*						EPAD MSOP-8		
AOZ1343AI-1*					Active High	SO-8		
AOZ1343EI-1*						EPAD MSOP-8		
AOZ1312AI-1	1.5 A	None	2 A	None	Active High	SO-8		
AOZ1312EI-1						EPAD MSOP-8		
AOZ1310CI-1	0.5 A	None	0.75 A	None	Active High	SOT23-5		

*Contact factory for availability

AOS Green Products use reduced levels of Halogens, and are also RoHS compliant.
Please visit www.aosmd.com/web/quality/rohs_compliant.jsp for additional information.

Pin Configuration

AOZ1310CI-1



SOT23-5
(Top View)

Pin Description

Pin Name	Pin Number	Pin Function
OUT	1	Power-switch output, IN-OUT
GND	2	Ground
$\overline{OC}$	3	Overcurrent, open-drain output, active low, IN-OUT
EN	4	Enable input, logic high turns on power switch, IN-OUT
IN	5	Input voltage

Absolute Maximum Ratings

Exceeding the Absolute Maximum Ratings may damage the device.

Parameter	Rating
Input Voltage (V_{IN})	6 V
Enable Voltage (V_{EN})	6 V
Storage Temperature (T_S)	-55 °C to +150 °C
ESD Rating[1]	2 kV

Note:

1. Devices are inherently ESD sensitive, handling precautions are required. Human body model is a 100 pF capacitor discharging through a 1.5 kΩ resistor.

Recommended Operating Conditions

The device is not guaranteed to operate beyond the Recommended Operating Conditions.

Parameter	Rating
Input Voltage (V_{IN})	+2.7 V to +5.5 V
Junction Temperature (T_J)	-40 °C to +125 °C
Package Thermal Resistance (Θ_{JA}) SOT23-5	191 °C/W

Electrical Characteristics

T_A = 25 °C, V_{IN} = V_{EN} =5.5 V, unless otherwise specified.

Symbol	Parameter	Conditions[3]		Min.	Typ.	Max.	Units
POWER SWITCH							
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 5.5 V, I_{OUT} = 0.5 A			80	145	mΩ
t_r	Rise Time, Output	V_{IN} = 5.5 V , C_L = 1 µF, R_L = 10 Ω			0.6	1.5	ms
		V_{IN} = 2.7 V, C_L = 1µF, R_L = 10 Ω			0.4	1	
t_f	Fall Time, Output	V_{IN} = 5.5 V		0.05		0.5	ms
		V_{IN} = 2.7 V		0.05		0.5	
	FET Leakage Current	Out connect to ground, $V_{I(ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	-40 °C ≤ T_J ≤ 125 °C[2]		1		µA
ENABLE INPUT $\overline{EN}$							
V_{IH}	High-level Input Voltage	2.7V ≤ V_{IN} ≤ 5.5V		2.0			V
V_{IL}	Low-level Input Voltage	2.7V ≤ V_{IN} ≤ 5.5V				0.8	V
I_I	Input Current			-0.5		-0.5	µA
t_{on}	Turn-on Time	C_L = 100 µF, R_L = 10 Ω				3	ms
t_{off}	Turn-off Time	C_L = 100 µF, R_L = 10 Ω				10	
CURRENT LIMIT							
I_{OS}	Short-circuit Output Current			0.5	0.8	1.0	A
I_{OC_TRIP}	Overcurrent Trip Threshold			0.6	0.85	1.1	A
SUPPLY CURRENT							
	Supply Current, Low-level Output	No load on OUT, $V_{I(ENx)}$ = 5.5 V, or $V_{I(ENx)}$ = 0 V	T_J = 25°C		0.5	1	µA
			-40 °C ≤ T_J ≤ 125 °C[2]		0.5	5	
	Supply Current, High-level Output	No load on OUT, $V_{I(ENx)}$ = 0 V, or $V_{I(ENx)}$ = 5.5 V	T_J = 25°C		50	70	µA
			-40 °C ≤ T_J ≤ 125 °C[2]		50	90	
	Reverse Leakage Current	$V_{I(OUTx)}$ = 5.5V, IN = ground	T_J = 25 °C		0.2		µA
UNDERVOLTAGE LOCKOUT							
	Low-level Voltage, IN			2		2.5	V
	Hysteresis, IN	T_J = 25°C			200		mV

Electrical Characteristics (Continued)

T_A = 25 °C, V_{IN} = V_{EN} =5.5 V, unless otherwise specified.

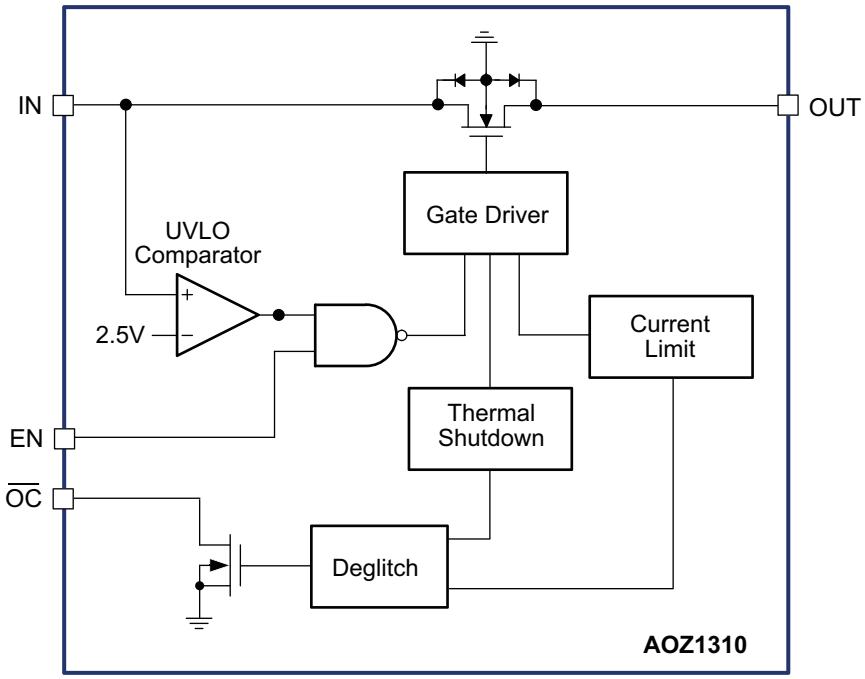
Symbol	Parameter	Conditions[3]	Min.	Typ.	Max.	Units
OVERCURRENT $\overline{OC}$						
	Output low Voltage $V_{OL(OCx)}$	$I_{O(OCx)}$ = 5mA			0.4	V
	Off-state Current	$V_{O(OCx)}$ = 5V or 3.3V			1	µA
	OC_L Deglitch	OCx assertion or deassertion	4	8	15	ms
THERMAL SHUTDOWN						
	Thermal Shutdown Threshold		135			°C
	Recovery from Thermal Shutdown		105			°C
	Hysteresis			30		°C

Note:

2. Parameters are guaranteed by design only and not production tested.

3. Pulse testing techniques maintain junction temperature close to ambient temperature; thermal effects must be taken into account separately.

Functional Block Diagram



Functional Characteristics

Figure 1. Turn-On Delay and Rise Time with 1μF Load (Active High)

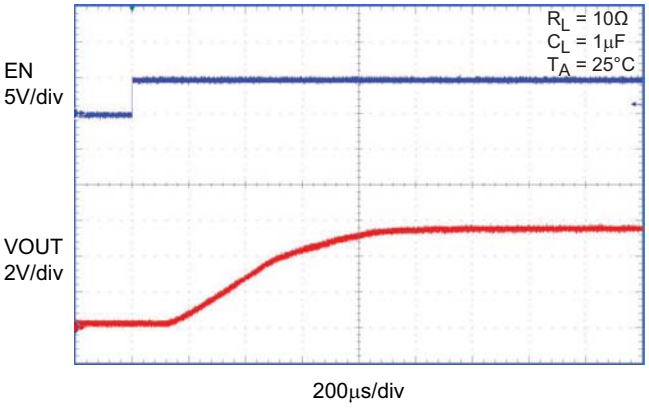


Figure 2. Turn-Off Delay and Fall Time with 1μF Load (Active High)

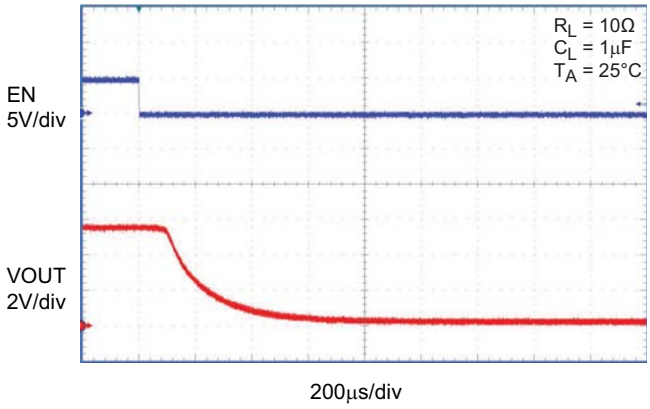


Figure 3. Turn-On Delay and Rise Time with 100μF Load (Active High)

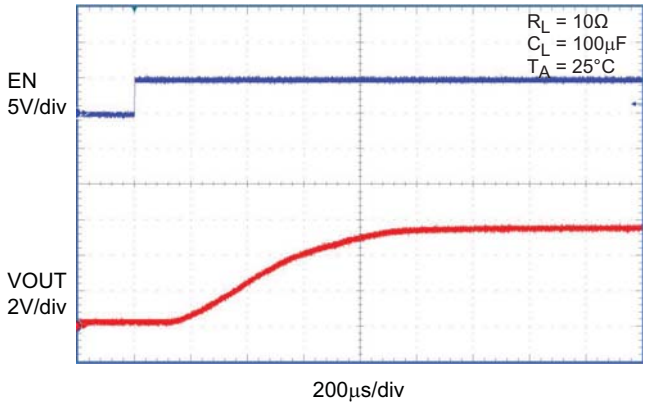
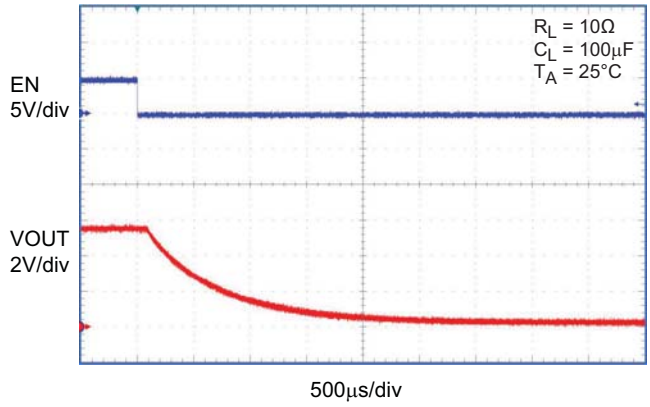


Figure 4. Turn-Off Delay and Fall Time with 100μF Load (Active High)



Typical Characteristics

Figure 5. Supply Current, Output Enabled vs. Junction Temperature

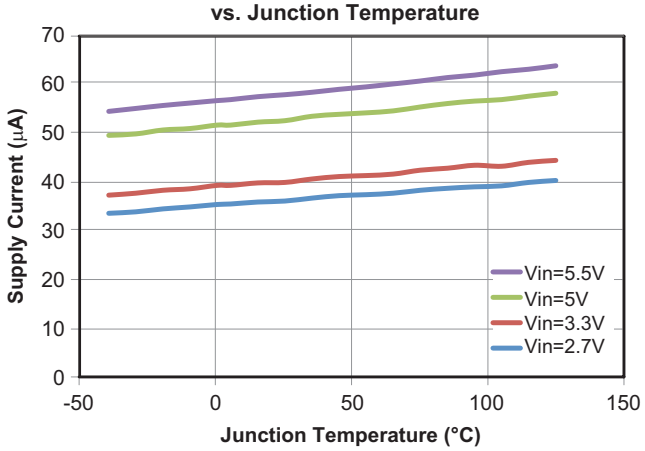


Figure 6. Supply Current, Output Disabled vs. Junction Temperature

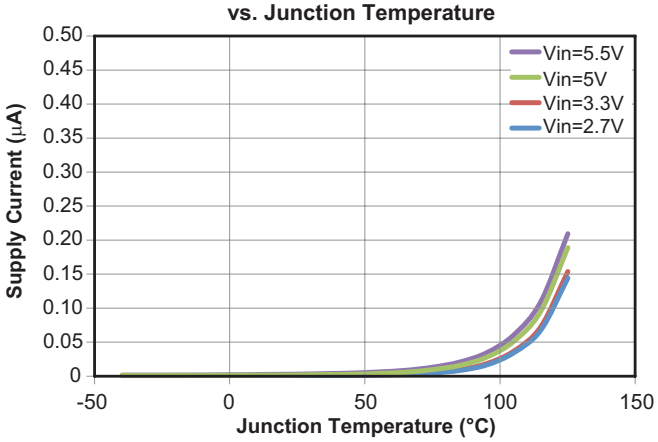
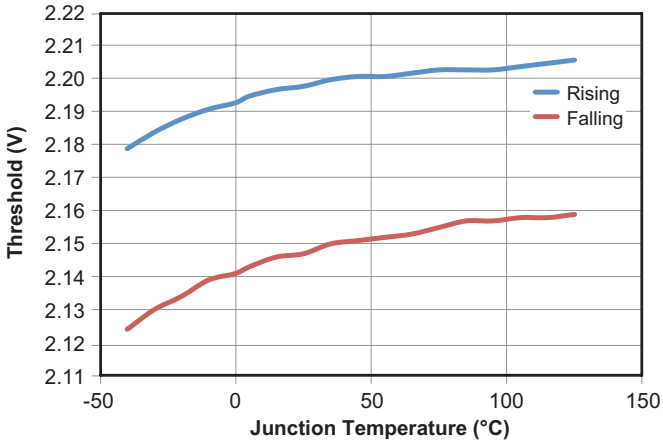


Figure 7. UVLO Threshold vs. Junction Temperature



Detailed Description

The AOZ1310 is a member of Alpha and Omega Semiconductor's single-channel power-distribution switches family. The AOZ1310 is intended for applications where heavy capacitive loads and short-circuits are likely to be encountered. Gate drive is provided by an internal charge pump designed to control the power-switch rise times and fall times to minimize current surges during switching. The charge pump requires no external components and allows operation from supplies as low as 2.7 V.

Power Switch

The power switch is a N-channel MOSFET with a low on-state resistance capable of delivering 1 A of continuous current. Configured as a high-side switch, the MOSFET will go into high impedance when disabled. Thus, preventing current flow from OUT to IN and IN to OUT.

Charge Pump

An internal charge pump supplies power to the circuits and provides the necessary voltage to drive the gate of the MOSFET beyond the source. The charge pump is capable of operating down to a low voltage of 2.7 Volts.

Driver

The driver controls the voltage on the gate to the power MOSFET switch. This is used to limit the large current surges when the switch is being turned On and Off. Proprietary circuitry controls the rise and fall time of the output voltages.

Enable

The logic enable disables the power switch, charge pump, gate driver, logic device, and other circuitry to reduce the supply current. When the enable receives a logic high the supply current is reduced to approximately 1 μA. The enable input is compatible with both TTL and CMOS logic levels.

Over-current

The over-current open drain output is asserted (active low) when an over-current condition occurs. The output will remain asserted until the over-current condition is removed. A 15 ms deglitch circuit prevents the over-current from false triggering.

Thermal Shut-down Protection

When the output load exceeds the current-limit threshold or a short is present, the device limits the output current to a safe level by switching into a constant-current mode, pulling the overcurrent (OC) logic output low.

During current limit or short circuit conditions, the increasing power dissipation in the chip causing the die temperature to rise. When the die temperature reaches a certain level, the thermal shutdown circuitry will shutdown the device. The thermal shutdown will cycle repeatedly until the short circuit condition is resolved.

Applications Information

Input Capacitor Selection

The input capacitor prevents large voltage transients from appearing at the input, and provides the instantaneous current needed each time the switch turns on and to limit input voltage drop. The input capacitor also prevents high-frequency noise on the power line from passing through the output of the power side. The choice of the input capacitor is based on its ripple current and voltage ratings rather than its capacitor value. The input capacitor should be located as close to the V_{IN} pin as possible. A 1 µF and above ceramic cap is recommended. However, higher capacitor values further reduce the voltage drop at the input.

Output Capacitor Selection

The output capacitor acts in a similar way. A small 0.1 µF capacitor prevents high-frequency noise from going into the system. Also, the output capacitor has to supply enough current for a large load that it may encounter during system transients. This bulk capacitor must be large enough to supply fast transient load in order to prevent the output from dropping.

Power Dissipation Calculation

Calculate the power dissipation for normal load condition using the following equation:

$$P_D = R_{ON} \times (I_{OUT})^2$$

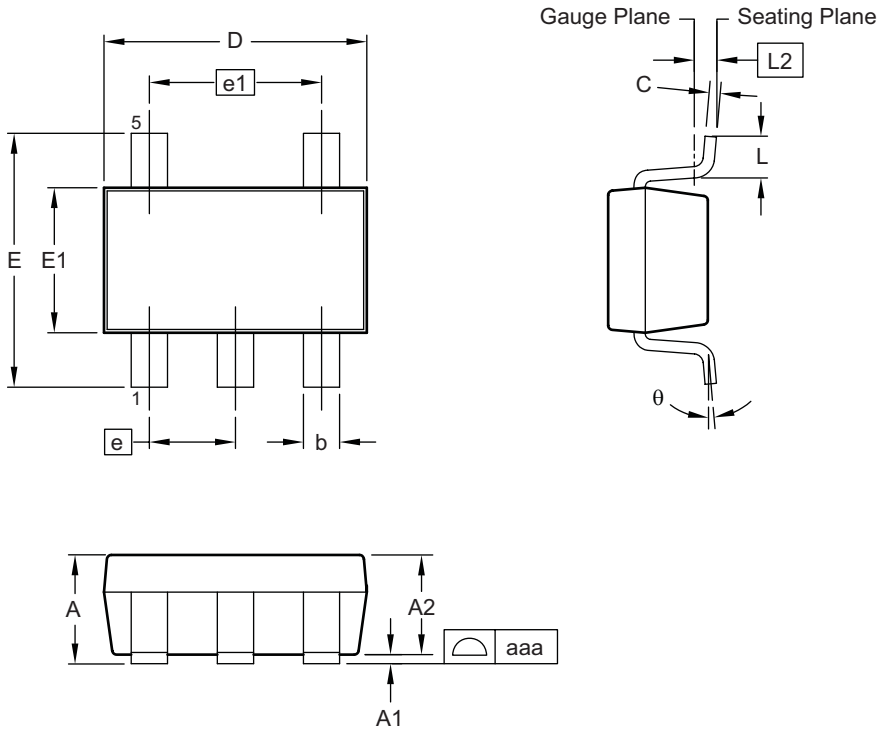
The worst case power dissipation occurs when the load current hits the current limit due to over-current or short circuit faults. The power dissipation under these conditions can be calculated using the following equation:

$$P_D = (V_{IN} - V_{OUT}) \times I_{LIMIT}$$

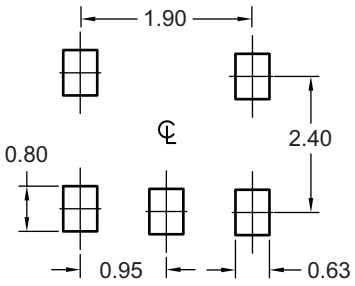
Layout Guidelines

Good PCB layout is important for improving the thermal and overall performance of the AOZ1310. To optimize the switch response time to output short-circuit conditions keep all traces as short as possible to reduce the effect of unwanted parasitic inductance. Place the input and output bypass capacitors as close as possible to the IN and OUT pins. The input and output PCB traces should be as wide as possible for the given PCB space. Use a ground plane to enhance the power dissipation capability of the device.

Package Dimensions, SOT23-5



RECOMMENDED LAND PATTERN



UNIT: mm

Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	—	—	1.00
A1	0.00	—	0.10
A2	0.70	0.88	0.95
b	0.35	0.40	0.50
C	0.10	0.13	0.20
D	2.80	2.90	3.00
E	2.60	2.80	3.00
E1	1.50	1.60	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.40	0.60
L2	0.25 BSC		
aaa	0.10		
θ	0°	—	8°

Dimensions in inches

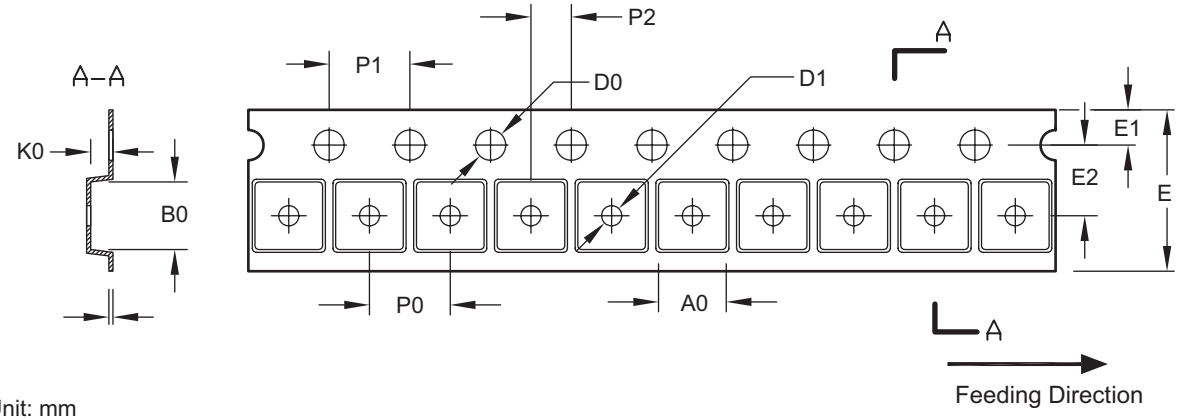
Symbols	Min.	Nom.	Max.
A	—	—	0.039
A1	0.00	—	0.004
A2	0.028	0.035	0.037
b	0.014	0.016	0.020
C	0.004	0.005	0.008
D	0.110	0.114	0.118
E	0.102	0.110	0.118
E1	0.059	0.063	0.067
e	0.037 BSC		
e1	0.075 BSC		
L	0.012	0.016	0.024
L2	0.010 BSC		
aaa	0.004		
θ	0°	—	8°

Notes:

1. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 5 mils.
2. Dimension "L" is measured in gauge plane.
3. Tolerance 0.10mm (4 mil) unless otherwise specified
4. Refer to JEDEC MO-193C AB.
5. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

Tape and Reel Dimensions, SOT23-5

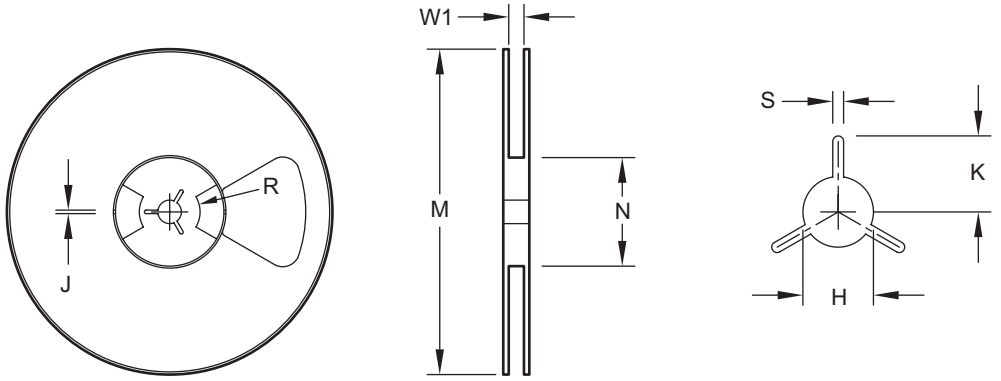
Tape



Unit: mm

Package	A0	B0	K0	D0	D1	E	E1	E2	P0	P1	P2	T
SOT23-5/6L LP	3.15 ±0.10	3.20 ±0.10	1.40 ±0.10	1.50 ±0.05	1.00 +0.10 / -0	8.00 ±0.30	1.75 ±0.10	3.50 ±0.05	4.00 ±0.10	4.00 ±0.10	2.00 ±0.05	0.23 ±0.03

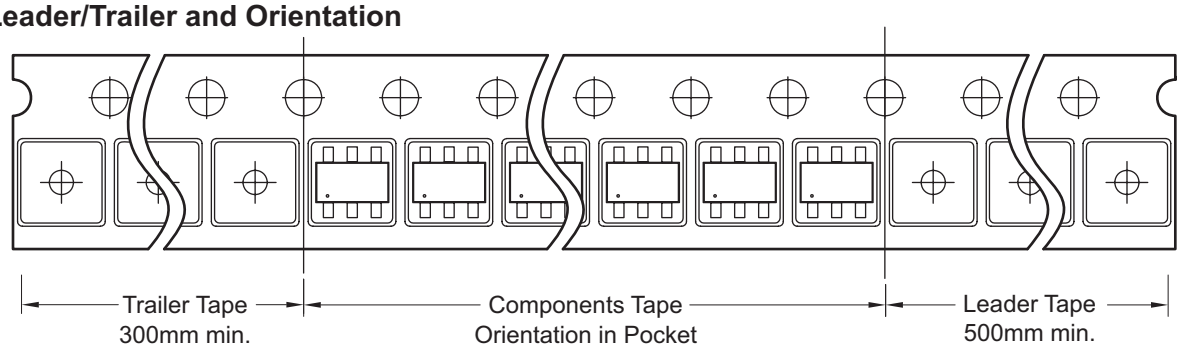
Reel



Unit: mm

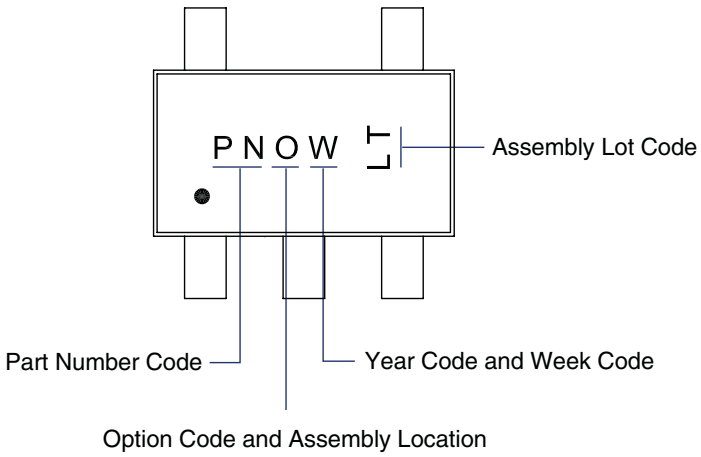
Tape Size	Reel Size	M	N	W1	H	S	K	R	J
8mm	ø177.8	ø177.8 Max.	55.0 Min.	8.4 +1.50 / -0.0	13.0 +0.5 / -0.2	1.5 Min	10.1 Min.	12.7	4.0 ±0.1

Leader/Trailer and Orientation



Part Marking

AOZ1310CI-1
(SOT23-5)



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Alpha & Omega Semiconductor reserves the right to make changes at any time without notice.

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.