

12-Channel TFT-LCD Reference Voltage Generator



The EL5325 is designed to produce the reference voltages required in TFT-LCD applications. Each output is

programmed to the required voltage with 10 bits of resolution. Reference pins determine the high and low voltages of the output range, which are capable of swinging to either supply rail. Programming of each output is performed using the 3-wire, SPI compatible interface.

A number of EL5325 can be stacked for applications requiring more than 12 outputs. The reference inputs can be tied to the rails, enabling each part to output the full voltage range, or alternatively, they can be connected to external resistors to split the output range and enable finer resolutions of the outputs.

The EL5325 has 12 outputs and is available in a 28-pin TSSOP package. They are specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5325IRZ (Note)	28-Pin TSSOP (Pb-Free)	-	MDP0044
EL5325IRZ-T7 (Note)	28-Pin TSSOP (Pb-Free)	7"	MDP0044
EL5325IRZ-T13 (Note)	28-Pin TSSOP (Pb-Free)	13"	MDP0044

NOTE: Intersil Pb-Free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-Free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J Std-020B.

Features

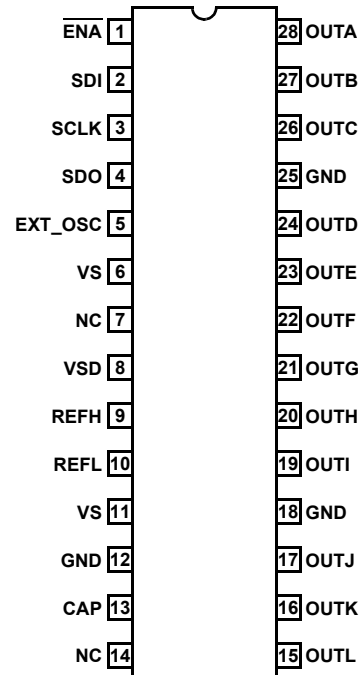
- 12-channel reference outputs
- Accuracy of $\pm 1\%$
- Supply voltage of 5V to 16.5V
- Digital supply 3.3V to 5V
- Low supply current of 10mA
- Rail-to-rail capability
- Internal thermal protection
- Pb-Free Available

Applications

- TFT-LCD drive circuits
- Reference voltage generators

Pinout

EL5325
(28-PIN TSSOP)
TOP VIEW



Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Supply Voltage between V_S & GND 4.5V (min) to 18V (max)
 Supply Voltage between V_{SD} & GND . 3V (min) to V_S and 7V (max)
 Maximum Continuous Output Current 30mA
 Power Dissipation See Curves

Maximum Die Temperature +125°C
 Storage Temperature -65°C to +150°C
 Ambient Operating Temperature -40°C to +85°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications $V_S = 15V, V_{SD} = 5V, V_{REFH} = 13V, V_{REFL} = 2V, R_L = 1.5k\Omega$ and $C_L = 200pF$ to 0V, $T_A = 25^\circ\text{C}$, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_S	Supply Current	No load		10.2	12.5	mA
I_{SD}	Digital Supply Current			0.17	0.35	mA
ANALOG						
V_{OL}	Output Swing Low	Sinking 5mA ($V_{REFH} = 15V, V_{REFL} = 0$)		50	150	mV
V_{OH}	Output Swing High	Sourcing 5mA ($V_{REFH} = 15V, V_{REFL} = 0$)	14.85	14.95		V
I_{SC}	Short Circuit Current	$R_L = 10\Omega$	100	140		mA
PSRR	Power Supply Rejection Ratio	V_S+ is moved from 14V to 16V	45	65		dB
t_D	Program to Out Delay			4		ms
V_{AC}	Accuracy referred to the ideal value	Code = 512		20		mV
ΔV_{MIS}	Channel to Channel Mismatch	Code = 512		2		mV
V_{DROOP}	Droop Voltage			1	2	mV/ms
R_{INH}	Input Resistance @ V_{REFH}, V_{REFL}			32		k Ω
REG	Load Regulation	$I_{OUT} = 5mA$ step		0.5	1.5	mV/mA
CAP	Band Gap	By pass with 0.1 μ F	1	1.3	1.6	V
DIGITAL						
V_{IH}	Logic 1 Input Voltage	$V_{SD} = 5V$	4			V
		$V_{SD} = 3.3V$	2			V
F_{CLK}	Clock Frequency				5	MHz
V_{IL}	Logic 0 Input Voltage	$V_{SD} = 3.3V/5V$			1	V
t_S	Setup Time			20		ns
t_H	Hold Time			20		ns
t_{LC}	Load to Clock Time			20		ns
t_{CE}	Clock to Load Line			20		ns
t_{DCO}	Clock to Out Delay Time	Negative edge of SCLK		10		ns
R_{SDIN}	S_{DIN} Input Resistance			1		G Ω
T_{PULSE}	Minimum Pulse Width for EXT_OSC Signal			5		μ s
Duty Cycle	Duty Cycle for EXT_OSC Signal			50		%
INL	Integral Nonlinearity Error			1.3		LSB
DNL	Differential Nonlinearity Error			0.5		LSB
F_{OSC}	Internal Refresh Oscillator Frequency	OSC_Select = 0		21		kHz

Pin Descriptions

EL5325	PIN NAME	PIN TYPE	PIN FUNCTION
1	$\overline{\text{EN}}\text{A}$	Logic Input	Chip select, low enables data input to logic
2	SDI	Logic Input	Serial data input
3	SCLK	Logic Input	Serial data clock
4	SDO	Logic Output	Serial data output
5	EXT_OSC	Logic Input/Output	External oscillator input or internal oscillator output
6, 11	VS+	Analog Power	Positive supply voltage for analog circuits
7, 14	NC		Not connected
8	VSD	Digital Power	Positive power supply for digital circuits (3.3V - 5V)
9	REFH	Analog Reference Input	High reference voltage
10	REFL	Analog Reference Input	Low reference voltage
12	GND	Ground	Ground
13	CAP	Analog Bypass Pin	Decoupling capacitor for internal reference generator, 0.1 μF
17	OUTJ	Analog Output	Channel J programmable output voltage
19	OUTI	Analog Output	Channel I programmable output voltage
20	OUTH	Analog Output	Channel H programmable output voltage
21	OUTG	Analog Output	Channel G programmable output voltage
22	OUTF	Analog Output	Channel F programmable output voltage
23	OUTE	Analog Output	Channel E programmable output voltage
24	OUTD	Analog Output	Channel D programmable output voltage
26	OUTC	Analog Output	Channel C programmable output voltage
27	OUTB	Analog Output	Channel B programmable output voltage
28	OUTA	Analog Output	Channel A programmable output voltage
15	OUTL	Analog Output	Channel L programmable output voltage
16	OUTK	Analog Output	Channel K programmable output voltage
18, 25	GND	Power	Ground

Typical Performance Curves

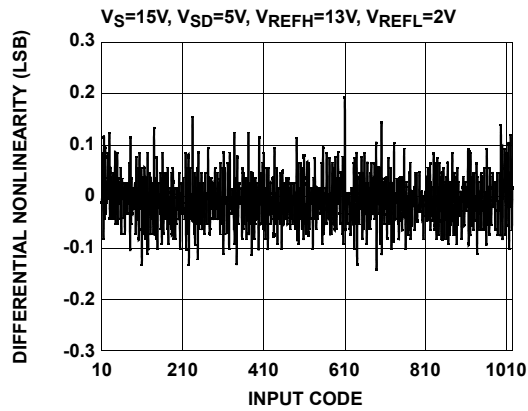


FIGURE 1. DIFFERENTIAL NONLINEARITY vs CODE

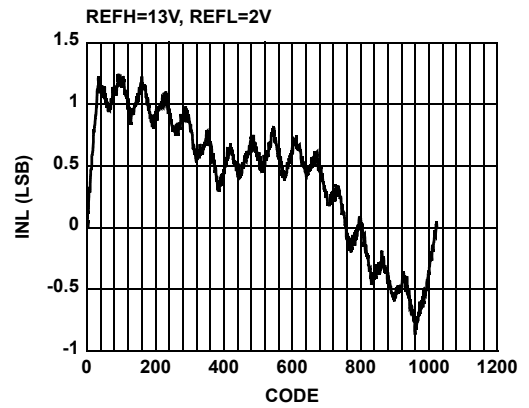


FIGURE 2. INTEGRAL NONLINEARITY ERROR

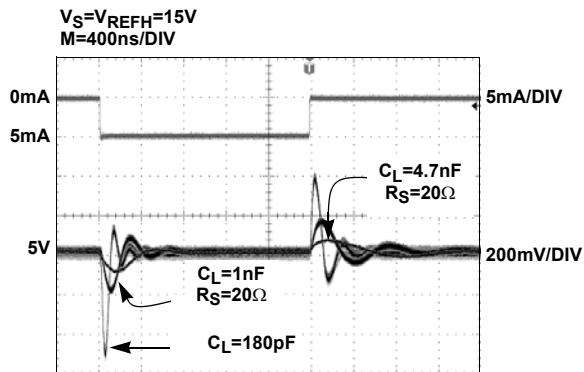


FIGURE 3. TRANSIENT LOAD REGULATION (SOURCING)

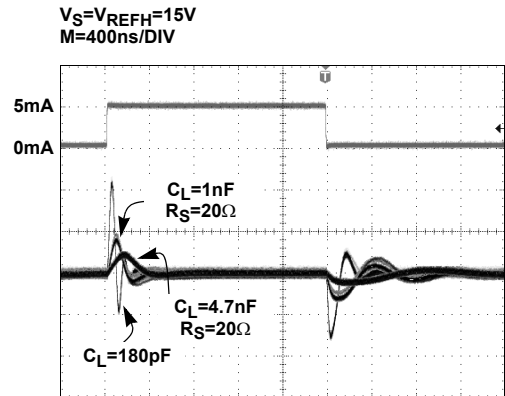


FIGURE 4. TRANSIENT LOAD REGULATION (SINKING)

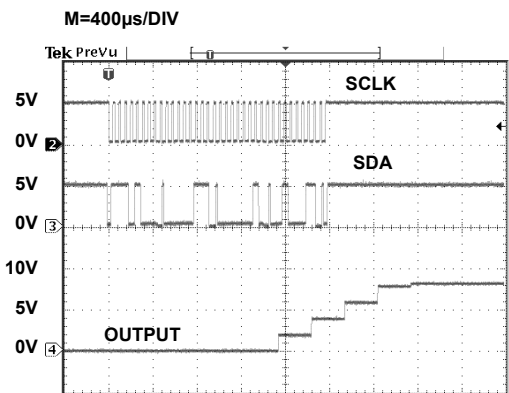


FIGURE 5. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

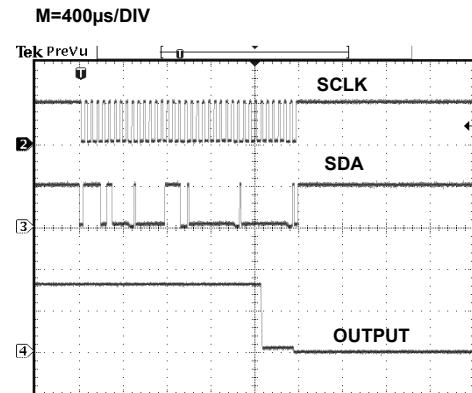


FIGURE 6. LARGE SIGNAL RESPONSE (FALLING FROM 8V TO 0V)

Typical Performance Curves (Continued)

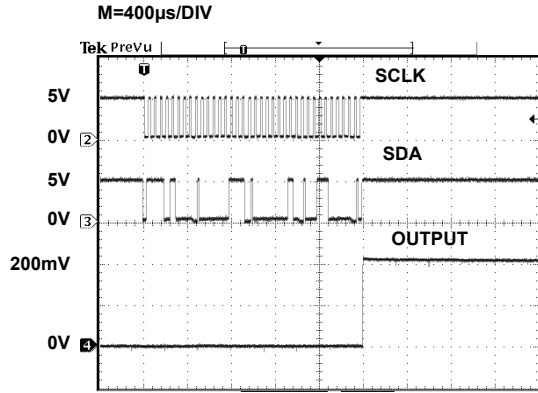


FIGURE 7. SMALL SIGNAL RESPONSE (RISING FROM 0V TO 200mV)

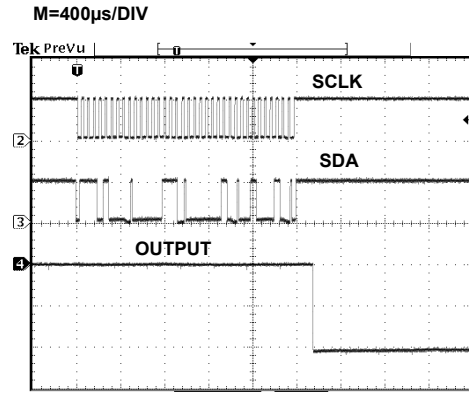


FIGURE 8. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 0V)

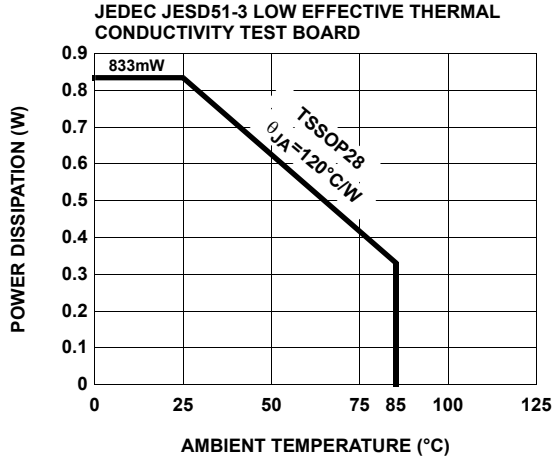


FIGURE 9. POWER DISSIPATION vs AMBIENT TEMPERATURE

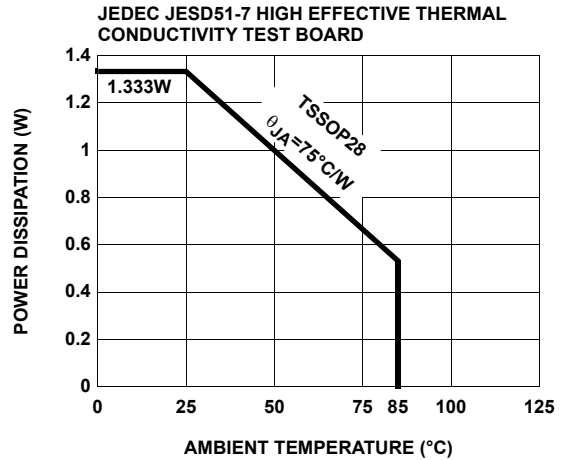


FIGURE 10. POWER DISSIPATION vs AMBIENT TEMPERATURE

General Description

The EL5325 provides a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels. The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear; however, if the panel is to be used in more than one application, the final curve may differ for different applications. By using the EL5325, the V/T curve can be changed to optimize its characteristics according to the required application of the display product. Each of the eight reference voltage outputs can be set with a 10-bit resolution. These outputs can be driven to within 50mV of the power rails of the EL5325. As all of the output buffers are identical, it is also possible to use the EL5325 for applications other than LCDs where multiple voltage references are required that can be set to 10 bit accuracy.

Digital Interface

The EL5325 uses a simple 3-wire SPI compliant digital interface to program the outputs. The EL5325 can support the clock rate up to 5MHz.

Serial Interface

The EL5325 is programmed through a three-wire serial interface. The start and stop conditions are defined by the $\overline{\text{ENA}}$ signal. While the $\overline{\text{ENA}}$ is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The MSB (bit 15) is loaded first and the LSB (bit 0) is loaded last (see Table 1). After the full 16-bit data has been loaded, the $\overline{\text{ENA}}$ is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the $\overline{\text{ENA}}$ is high. The SCLK must be low before the $\overline{\text{ENA}}$ is pulled low.

To facilitate the system designs that use multiple EL5325 chips, a buffered serial output of the shift register (SDO pin) is available. Data appears on the SDO pin at the 16th falling SCLK edge after being applied to the SDI pin.

To control the multiple EL5325 chips from a single three-wire serial port, just connect the $\overline{\text{ENA}}$ pins and the SCLK pins together, connect the SDO pin to the SDI pin on the next chip. While the $\overline{\text{ENA}}$ is held low, the 16m-bit data is loaded to the SDI input of the first chip. The first 16-bit data will go to the last chip and the last 16-bit data will go to the first chip. While the $\overline{\text{ENA}}$ is held high, all addressed outputs will be updated simultaneously.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

The serial data has a minimum length of 16 bits, the MSB (most significant bit) is the first bit in the signal. The bits are allocated to the following functions (also refer to the Control Bits Logic Table)

- Bit 15 is always set to a zero
- Bit 14 controls the source of the clock, see the next section for details
- Bits 13 through 10 select the channel to be written to, these are binary coded with channel A = 0, and channel H = 7
- The 10-bit data is on bits 9 through 0. Some examples of data words are shown in the table of Serial Programming Examples

TABLE 1. CONTROL BITS LOGIC TABLE

BIT	NAME	DESCRIPTION
B15	Test	Always 0
B14	Oscillator	0 = Internal, 1 = External
B13	A3	Channel Address
B12	A2	Channel Address
B11	A1	Channel Address
B10	A0	Channel Address
B9	D9	Data
B8	D8	Data
B7	D7	Data
B6	D6	Data
B5	D5	Data
B4	D4	Data
B3	D3	Data
B2	D2	Data
B1	D1	Data
B0	D0	Data

Serial Timing Diagram

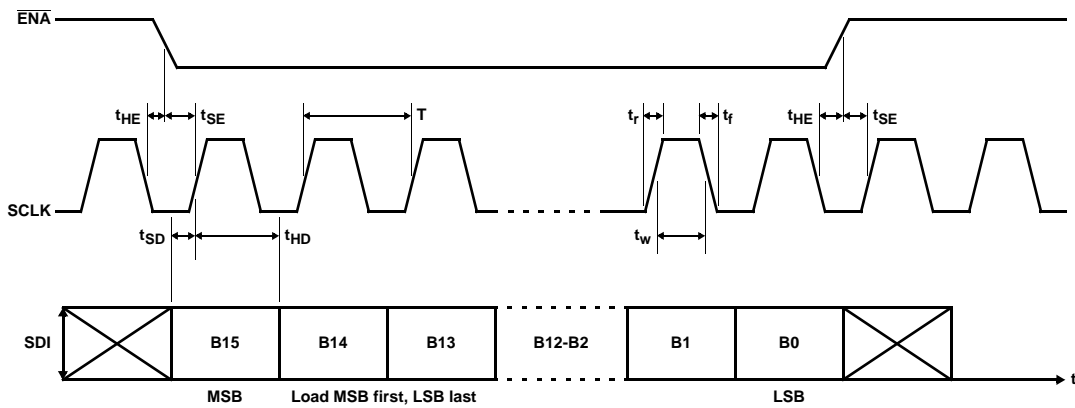


TABLE 2. SERIAL TIMING PARAMETERS

PARAMETER	RECOMMENDED OPERATING RANGE	DESCRIPTION
T	≥200ns	Clock Period
t _r /t _f	0.05 * T	Clock Rise/Fall Time
t _{HE}	≥10ns	$\overline{\text{ENA}}$ Hold Time
t _{SE}	≥10ns	$\overline{\text{ENA}}$ Setup Time
t _{HD}	≥10ns	Data Hold Time
t _{SD}	≥10ns	Data Setup Time
t _W	0.50 * T	Clock Pulse Width

TABLE 3. SERIAL PROGRAMMING EXAMPLES

CONTROL		CHANNEL ADDRESS				DATA										CONDITION	
C1	C0	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Internal Oscillator, Channel A, Value = 0
0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	Internal Oscillator, Channel A, Value = 1023
0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	Internal Oscillator, Channel A, Value = 512
0	0	0	0	1	1	1	0	0	0	0	0	0	0	0	1 ^t	1	Internal Oscillator, Channel C, Value = 513
0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1	Internal Oscillator, Channel H, Value = 31
0	1	0	1	1	1	0	0	0	0	0	1	1	1	1	1	1	External Oscillator, Channel H, Value = 31

Analog Section

TRANSFER FUNCTION

The transfer function is:

$$V_{\text{OUT(IDEAL)}} = V_{\text{REFL}} + \frac{\text{data}}{1024} \times (V_{\text{REFH}} - V_{\text{REFL}})$$

where data is the decimal value of the 10-bit data binary input code.

The output voltages from the EL5325 will be derived from the reference voltages present at the V_{REFL} and V_{REFH} pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5325. GND < V_{REFH} ≤ V_S and GND ≤ V_{REFL} ≤ V_{REFH}.

In some LCD applications that require more than 12 channels, the system can be designed such that one EL5325 will provide the Gamma correction voltages that are more positive than the V_{COM} potential. The second EL5325 can provide the Gamma correction voltage more negative than the V_{COM} potential. The Application Drawing shows a system connected in this way.

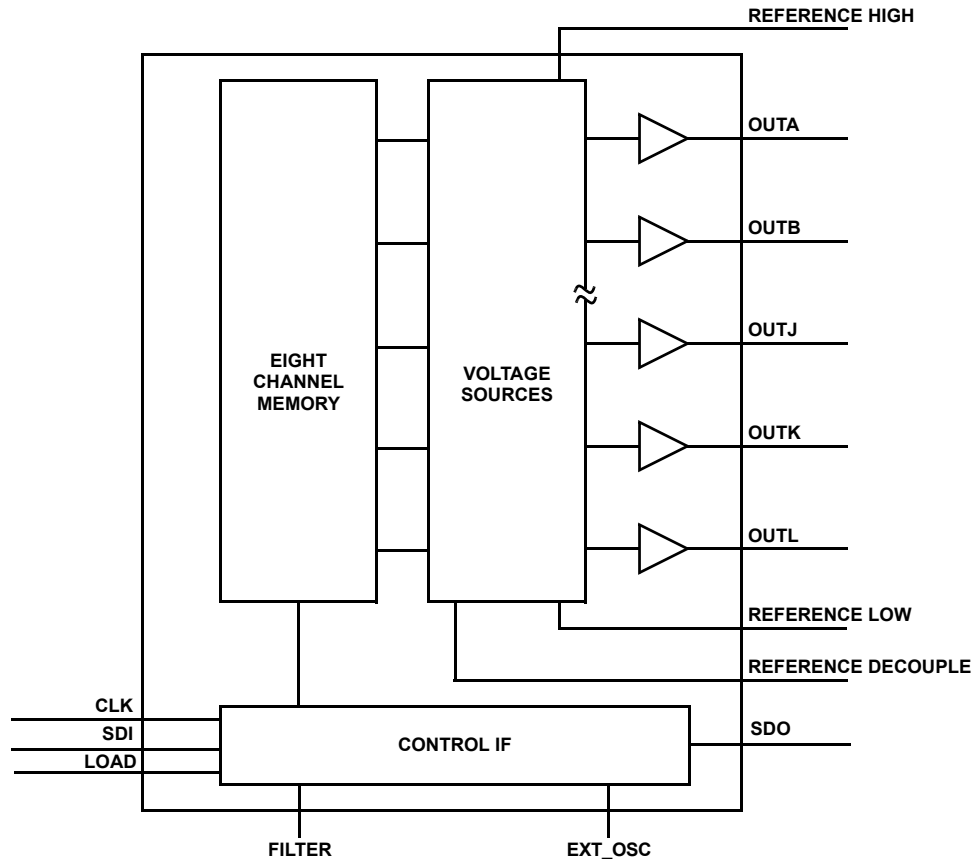
CLOCK OSCILLATOR

The EL5325 requires an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labeled OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the OSC pin. In a 2 chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock Mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the OSC pin will be in a high impedance condition to prevent contention. By setting B14 to high, the chip is on external clock mode. Setting B14 to low, the chip is on internal clock mode.

Block Diagram



CHANNEL OUTPUTS

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 50mV of the power rails, (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 48μs. In the worst-case scenario this will be 576μs when the data has just missed the cycle.

When a large change in output voltage is required, the change will occur in 2V steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16V can take between 4.6ms to 5.2ms depending on the absolute timing relative to the update cycle.

POWER DISSIPATION AND THERMAL SHUTDOWN

With the 30mA maximum continuous output drive capability for each channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

- T_{JMAX} = Maximum junction temperature
- T_{AMAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- P_{DMAX} = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = V_S \times I_S + \sum[(V_S - V_{OUTi}) \times I_{LOADi}]$$

when sourcing, and:

$$P_{D_{MAX}} = V_S \times I_S + \sum (V_{OUTi} \times I_{LOADi})$$

when sinking.

Where:

- $i = 1$ to total 12
- V_S = Supply voltage
- I_S = Quiescent current
- V_{OUTi} = Output voltage of the i channel
- I_{LOADi} = Load current of the i channel

By setting the two $P_{D_{MAX}}$ equations equal to each other, we can solve for the R_{LOADS} to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

The EL5325 has an internal thermal shutdown circuitry that prevents overheating of the part. When the junction temperature goes up to about 150°C, the part will be disabled. When the junction temperature drops down to about 120°C, the part will be enabled. With this feature, any short circuit at the outputs will enable the thermal shutdown circuitry to disable the part.

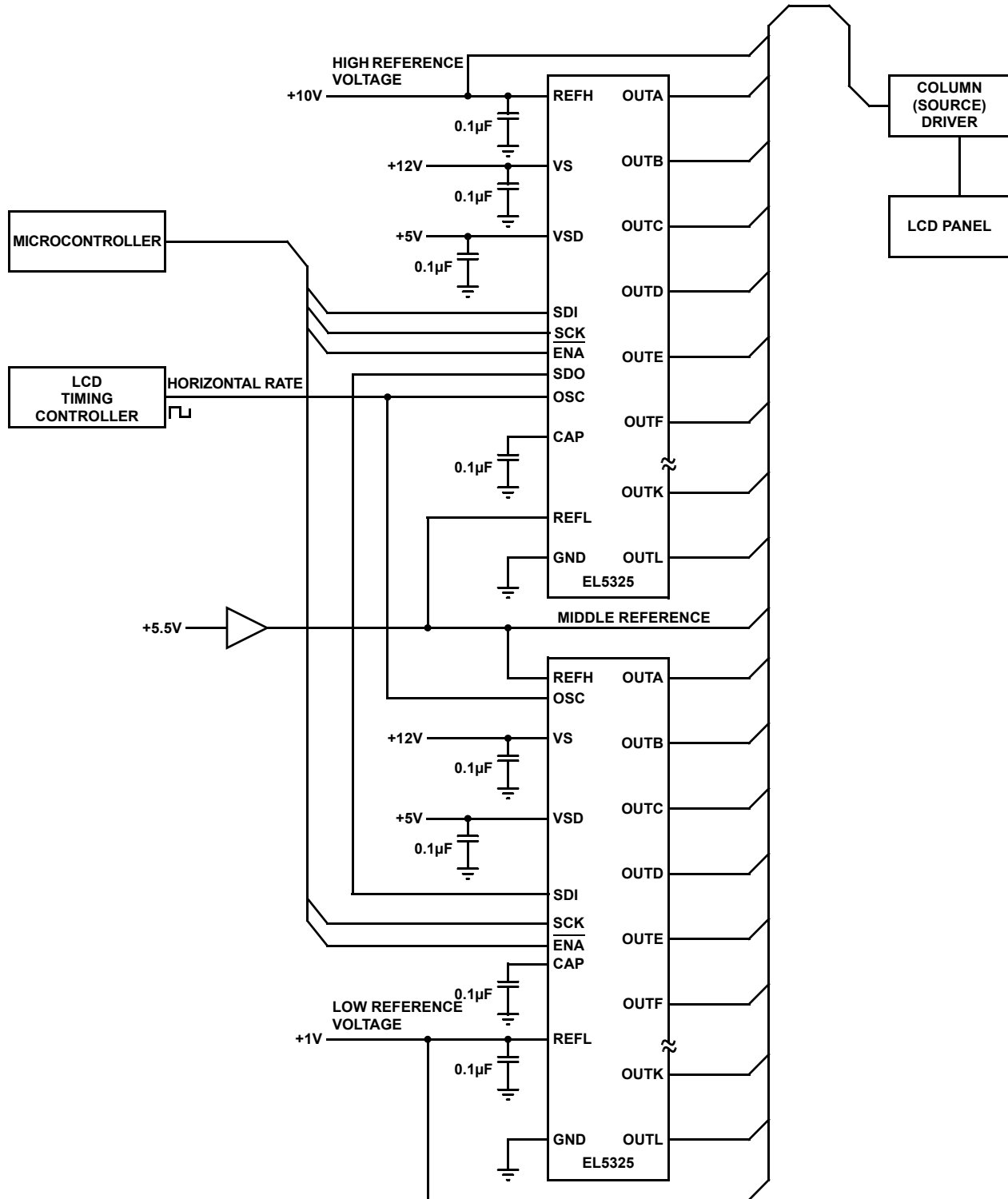
POWER SUPPLY BYPASSING AND PRINTED CIRCUIT BOARD LAYOUT

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5325. The traces from the two ground pins to the ground plane must be very short. The thermal pad of the EL5325 should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1µF ceramic capacitor must be placed very close to the V_S , V_{REFH} , V_{REFL} , and CAP pins. A 4.7µF local bypass tantalum capacitor should be placed to the V_S , V_{REFH} , and V_{REFL} pins.

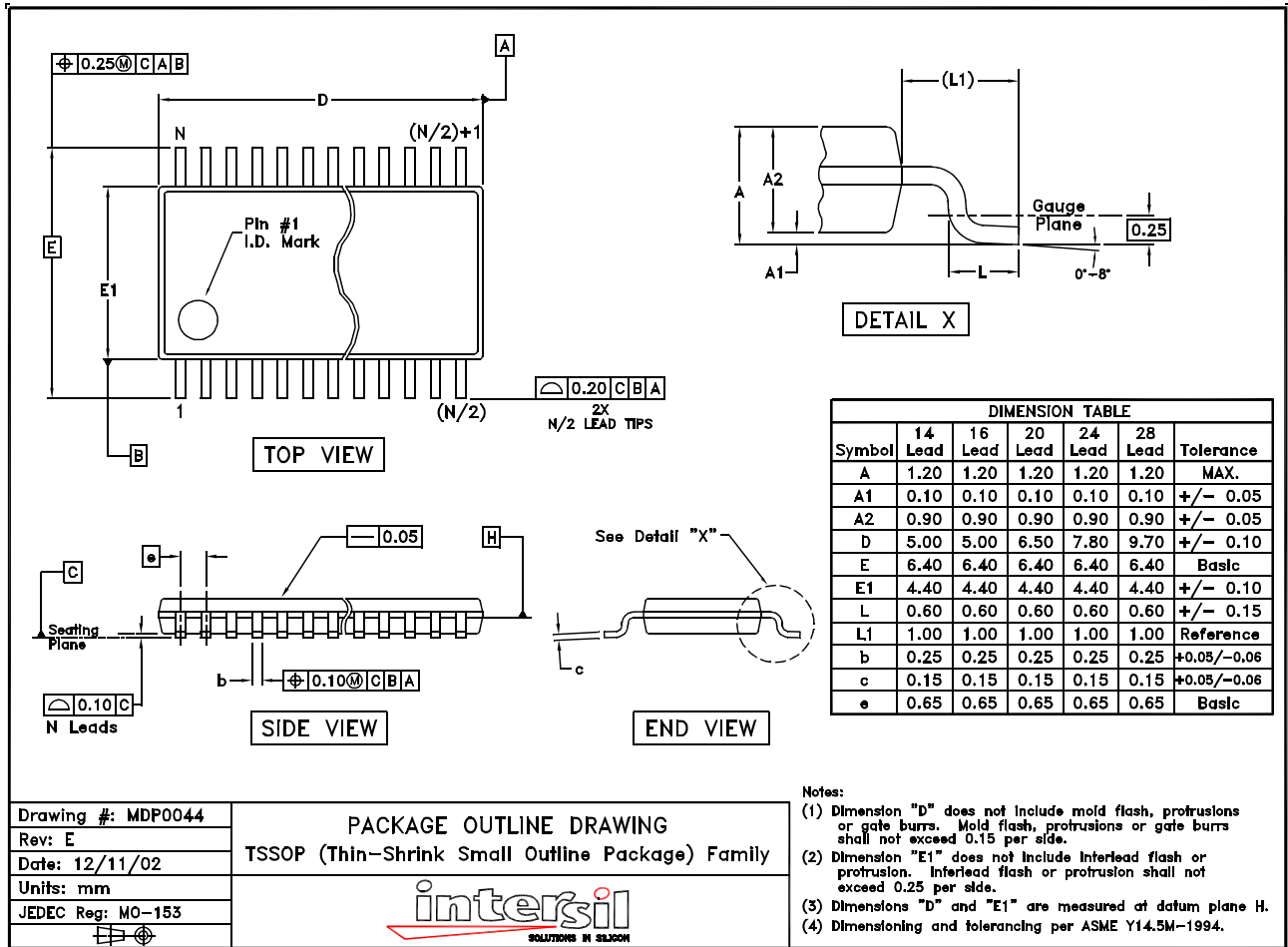
APPLICATION USING THE EL5325

In the first application drawing, the schematic shows the interconnect of a pair of EL5325 chips connected to give 12 gamma corrected voltages above the V_{COM} voltage, and 12 gamma corrected voltages below the V_{COM} voltage.

Application Drawing



TSSOP Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see www.intersil.com