ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		bq26501	UNIT
Supply voltage range, V_{CC} (all with respect to V_{SS})		−0.3 to 7.0	V
Input voltage range at SRP, SRN, RBI, and BAT (all with respect to V_{SS})		−0.3 to V_{CC} + 0.3 V	
Input voltage	HDQ, GPIO (with respect to V_{SS})	−0.3 to 7.0	
	GPIO (with respect to V_{SS}) during EEPROM programming only	−0.3 to 22.0	
Output sink current at GPIO, HDQ		5	mA
Operating free-air temperature range, T_A		−20 to 70	°C
Storage temperature range, T_{stg}		65°C to 150°C	
Junction temperature range, T_J		−40°C to 125°C	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under ”absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under ”recommended operating conditions” is not implied. Exposure to Absolute Maximum Rated conditions for extended periods may affect device reliability

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}	2.6		4.5	V
Operating free-air temperature, T_J	−20		70	°C
Input voltage range at SRP and SRN, (with respect to V_{SS})	−100		100	mV

ELECTRICAL CHARACTERISTICS

T_J = −20°C to 70°C, $T_J = T_A$, 2.6 V ≤ V_{CC} ≤ 4.5 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENTS						
$I_{CC(ACT)}$	Active current	$V_{CC} > V_{CC(min)}$		60	90	µA
$I_{CC(SLP)}$	Sleep current			1.2	2.5	
$I_{CC(SHP)}$	Ship current			0.9	1.7	
$I_{CC(POR)}$	Hibernate current	0 V < V_{CC} < $V_{(POR)}$		0.6	1.5	
	RBI current	RBI pin only, V_{CC} < $V_{(POR)}$			20	nA
$V_{(POR)}$	POR threshold		2.05		2.55	V
	POR threshold hysteresis			100		mV
	Input impedance on BAT pin		10			MΩ
	Input impedance on SRP, SRN pins		10			
VOLTAGE MEASUREMENT						
	Measurement range	$V_{CC} = V_{I(BAT)}$	2.6		4.5	V
	Reported voltage resolution			1		mV
	Reported accuracy		−20		20	
	Voltage update time			2		s
TEMPERATURE MEASUREMENT						
	Reported temperature resolution			0.25		°K
	Reported temperature accuracy		−3		3	
	Temperature update time			2		s

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The bq26501 determines battery capacity by monitoring the amount of charge input to or removed from a Li-Ion or Li-Pol battery. The bq26501 measures discharge and charge currents, monitors the battery for low voltage thresholds, and compensates for temperature and self-discharge rate. Current is measured across a small value series resistor between the negative terminal of the battery and the pack ground (see R_S in Figure 2). Available capacity is reported with a resolution of 0.003/R_S(mAh). Time-to-empty (TTE) reporting in minutes at host-provided at-rate currents allow the requirements for host based calculations to be greatly reduced or eliminated; reading a single register pair provides useful and meaningful information to the application's end user.

Figure 2 shows a typical application circuit. Differential sense of the voltage across the current sense resistor, R_S, improves device performance, leading to an improvement in reported time-to-empty accuracy. In the typical application, the GPIO pin can be used as a general-purpose programmable I/O port. An internal pull-down on the HDQ line ensures that the device detects a logic "0" on the HDQ line and automatically enters the low power sleep mode when the system power is switched off or the pack is removed. A 100-kΩ pull-up to V_{CC} can be added to the HDQ line to disable this feature. The bq26501 can operate directly from a single Li-Ion or Li-Pol cell.

Measurements

As shown in the Figure 3, the bq26501 uses a fully differential, dynamically balanced voltage-to-frequency converter (VFC) for charge and discharge counting and an analog-to-digital converter (ADC) for battery voltage and temperature measurement. Both VFC and ADC are automatically compensated for offset. No user calibration or compensation is required.

Charge and Discharge Counting

The bq26501 uses a voltage-to-frequency converter (VFC) to perform a continuous integration of the voltage waveform across a small value sense resistor in the negative lead of the battery, as shown in Figure 2. The integration of the voltage across the sense resistor is the charge added or removed from the battery. Since the VFC directly integrates the waveform, the shape of the current waveform through the sense resistor has no effect on the measurement accuracy. The low-pass filter that feeds the sense resistor voltage to the bq26501 SRP and SRN inputs serves to filter out system noise and does not affect the measurement accuracy, since the low-pass filter does not change the integrated value of the waveform.

Offset Calibration

The offset voltage of the VFC measurement must be very low to be able to measure small signal levels accurately. The bq26501 provides an auto-compensation feature to cancel the internal voltage offset error across SRP and SRN for maximum charge measurement accuracy.

NOTE:NO CALIBRATION IS REQUIRED. See the *Layout Considerations* section for details on minimizing PCB induced offset across the SRP and SRN pins.

APPLICATION INFORMATION

VDQ is cleared and a capacity learning cycle is disqualified by any of the following conditions:

1. Cold temperature: Temperature less than or equal to the TOFF value programmed in the TCOMP register when the EDV1 threshold voltage is reached.
2. Light load: Average current is less than or equal to 2 times the initial standby load (ISLC) when the EDV1 threshold voltage is reached.
3. Fast voltage drop: VOLT ≤ (EDV1 − 256 mV) when EDV1 is set.
4. Excessive charging: Cumulative charge added is greater than 255 mAh during a learning discharge cycle (alternating discharge-charge-discharge before EDV1 is set).
5. Reset: VDQ is cleared on reset.
6. Excessive self-discharge: NAC reduction from self−discharge estimate exceeds 12.48%.
7. Self-discharge at termination of learning cycle. If self-discharge estimate reduces NAC until NAC ≤ LMD/16.

APPLICATION INFORMATION

Reserved Registers

The addresses 0x14 – 0x6D and addresses 0x6F – 0x75 are reserved and cannot be written by the host.

EEPROM Enable Register (EE_EN) – Address 0x6E

Register used to enable host writes to EEPROM data locations (addresses 0x76 – 0x7F). Host must write data 0xDD to this register to enable EEPROM programming. See the *Programming the EEPROM* section for further information on programming the EEPROM bytes.

EEPROM Data Registers (EE_DATA) – Address 0x76 – 0x7F

The EEPROM data registers contain information vital to the performance of the device. These registers are to be programmed during pack manufacturing to allow flexibility in the design values of the battery to be monitored. The EEPROM data registers are listed in Table 2. Detailed descriptions of what should be programmed follows. See *Programming the EEPROM* for detailed information on writing the values to EEPROM.

Table 2. bq26501 EEPROM Memory Map

ADDRESS	NAME	FUNCTION
0x7F	TCOMP	Temperature compensation constants, ***OR***, ID#1
0x7E	DCOMP	Discharge rate compensation constants, ***OR***, ID#2
0x7D	ID3	ID#3
0x7C	PKCFG	Pack configuration values
0x7B	TAPER	Charge termination taper current
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants
0x79	ISLC	Initial standby load current
0x78	SEDV1	Scaled EDV1 threshold
0x77	SEDVF	Scaled EDVF threshold
0x76	ILMD	Initial last measured discharge high byte

APPLICATION INFORMATION

Digital Magnitude Filter and Self-Discharge Values (DMFSD) – Address 0x7A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DMF[3]	DMF[2]	DMF[1]	DMF[0]	SD[3]	SD[2]	SD[1]	SD[0]

MODE REGISTER	DESCRIPTION
DMF[3] DMF[2] DMF[1] DMF[0]	Sets the digital magnitude filter (DMF) threshold. See *Digital Magnitude Filter* section for more information on the function of the DMF. The value to be programmed is: $DMF[3:0] = \frac{\text{Design Threshold}}{6}, \ \mu V$
SD[3] SD[2] SD[1] SD[0]	Sets the self-discharge rate %/day value at 25°C. NAC is reduced with an estimated self-discharge correction to adjust for the expected self-discharge of the battery. This estimation is only performed when the battery is not being charged. The rate programmed in EEPROM for DMFSD determines the self-discharge when 20°C ≤ TEMP < 30°C. The self-discharge estimation is doubled for each 10°C decade hotter than the 20°C−30°C decade, up to a maximum of 16 times the programmed rate for TEMP ≥ 60°C and is halved for each 10°C decade colder than the 20°C−30°C decade, down to a minimum of one-quarter the programmed rate for TEMP < 0°C. The self-discharge estimation is performed by reducing NAC by NAC/512 at a time interval that achieves the desired estimation. If DMFSD is programmed with 12 decimal, the self-discharge rate is 0.195% per day in the 20°C−30°C decade. This is accomplished by reducing NAC by NAC/512 (100/512 = 0.195%) a single time every 24 hours. If temperature rises by 10°C, the 0.195% NAC reduction is made every 12 hours. The value to be programmed is: $SD[3:0] = \frac{2.34}{\text{Design SD}}, \ \%/\text{day}$

Taper Current (TAPER) − Address 0x7B

This register contains the scaled end equipment design charge taper current. This value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming this value is:

$$TAPER = \frac{I_{TAPER}\ (mA) \times R_S\ (m\Omega)}{192\ (\mu V)} \quad (8)$$

where R_S is the value of the sense resistor used in the system.

NAME

APPLICATION INFORMATION

Identification Byte #3 (ID3) − Address 0x7D

This register may be programmed to any desired value.The contents do not affect the operation of the bq26501.

Discharge Rate Compensation Constants (DCOMP) or ID2 − Address 0x7E

This register is used to set the compensation coefficients for discharge rate. These coefficients are applied to the nominal available charge (NAC) to more accurately predict capacity at high discharge rates.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DCGN[5]	DCGN[4]	DCGN[3]	DCGN[2]	DCGN[1]	DCGN[0]	DCOFF[1]	DCOFF[0]

MODE REGISTER	DESCRIPTION
DCGN[5]	Discharge rate compensation gain. Used to set the slope of the discharge capacity compensation as a percentage of discharge current. The gain factor adjustment is in increments of 0.39% of discharge current in excess of the DCOFF value. The equation for programming the value is: DCGN[5:0] = 2.56 × design discharge compensation gain %
DCGN[4]	
DCGN[3]	
DCGN[2]	
DCGN[1]	
DCGN[0]	
DCOFF[1]	These bits set the discharge threshold of compensating the nominal available charge for discharge rate. The threshold is set as shown in Table 4.
DCOFF[0]	

Table 4. Discharge Rate Compensation Thresholds

DCOFF[1]	DCOFF[0]	DCOFF THRESHOLD
0	0	0
0	1	LMD/2
1	0	LMD/4
1	1	LMD/8

Discharge compensation, DCMP, is computed from these coefficients as follows:

$$DCMP = \frac{DCGN \times (AI - DCOFF)}{256} \tag{9}$$

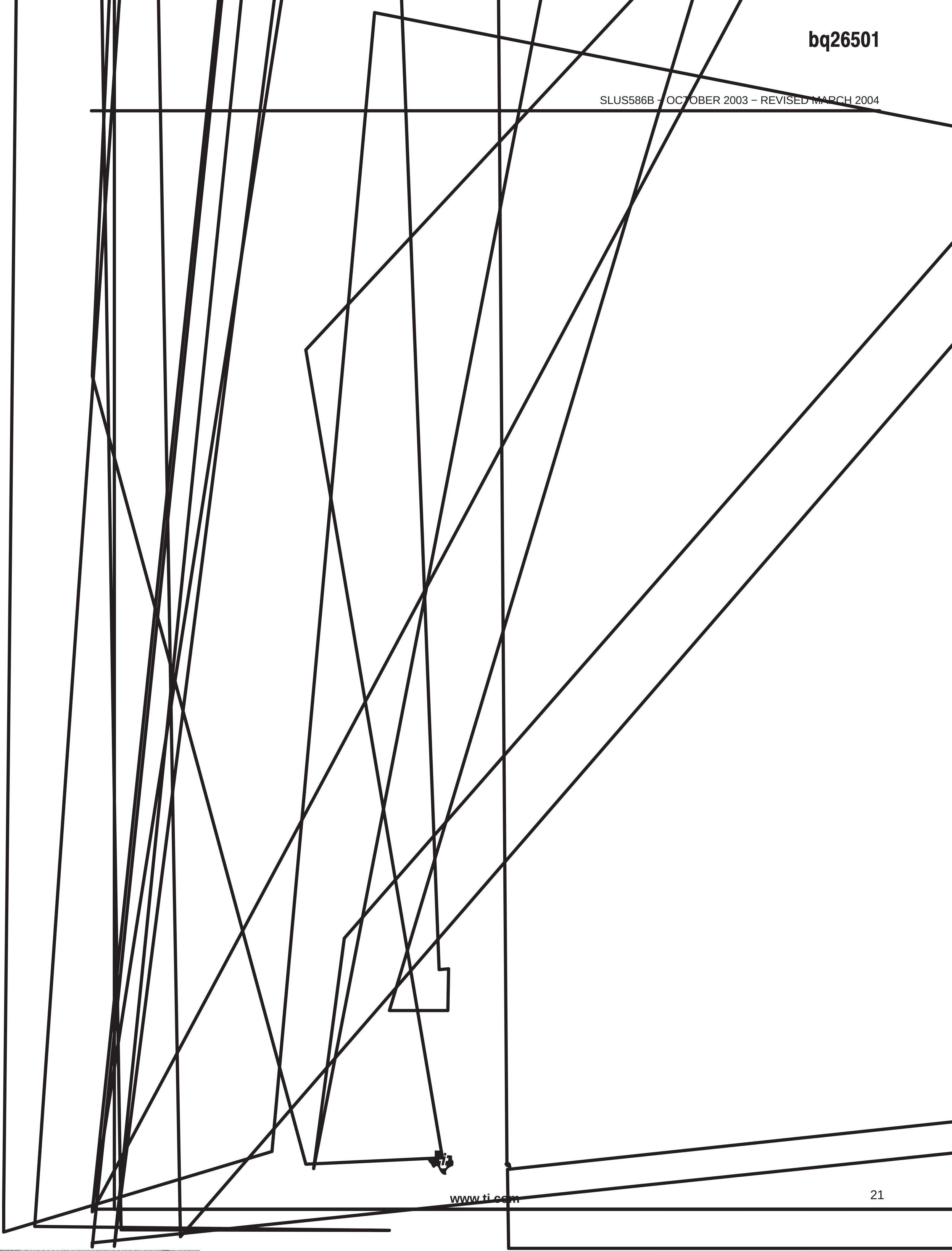
where DCMP is restricted to ≥ 0. AI is the average discharge current. The CACD register then takes on the value:

$$CACD = NAC - (DCMP - DCMPADJ),\ \text{if}\ DCMP > DCMPADJ\ \text{or} \tag{10}$$

$$CACD = NAC,\ \text{if}\ DCMP \le DCMPADJ \tag{11}$$

where DCMPADJ is the value of DCMP at a previous EDV1 detection. This allows the compensation for CACD to adapt as the LMD value is learned.

If PKCFG[1]=1, the device assumes a fixed value of 0x42 for DCOMP, giving a discharge rate compensation gain of 6.25% with a compensation threshold of C/4. This frees the EEPROM location of 0x7E for a user-defined identification byte, ID2.



APPLICATION[illegible]ATION

Command Byte

The command by[illegible]he bq26501 consists[illegible]ht contiguous valid comm[illegible]ts. The command byte contains two field[illegible] command and addres[illegible]ommand byte values a[illegible]n in the following table:

	[illegible]T 7	BIT 6	BIT 5	[illegible]	BIT 3	BIT[illegible]	BIT 1	BIT 0
NAME	[illegible]/R	AD6	AD5	[illegible]	AD3	AD[illegible]	AD1	AD0

MODE

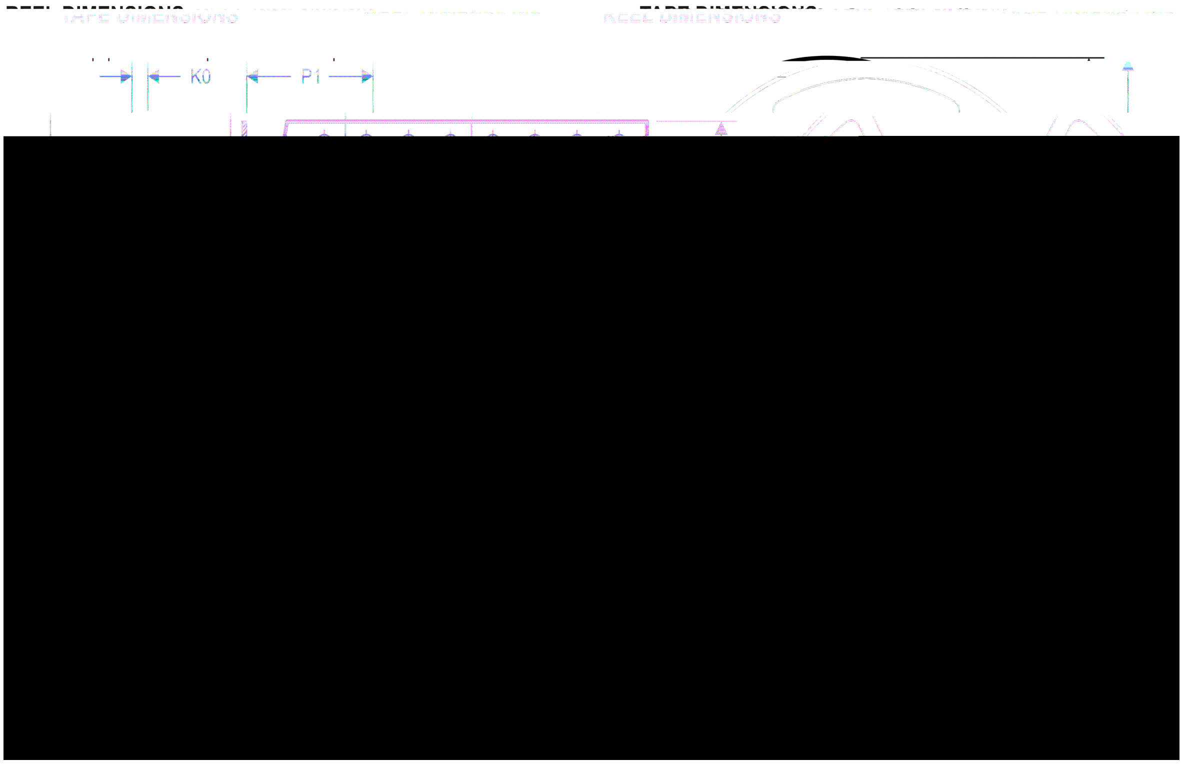
PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ26501PW	ACTIVE	TSSOP	PW	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ26501PWG4	ACTIVE	TSSOP	PW	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ26501PWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ26501PWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements

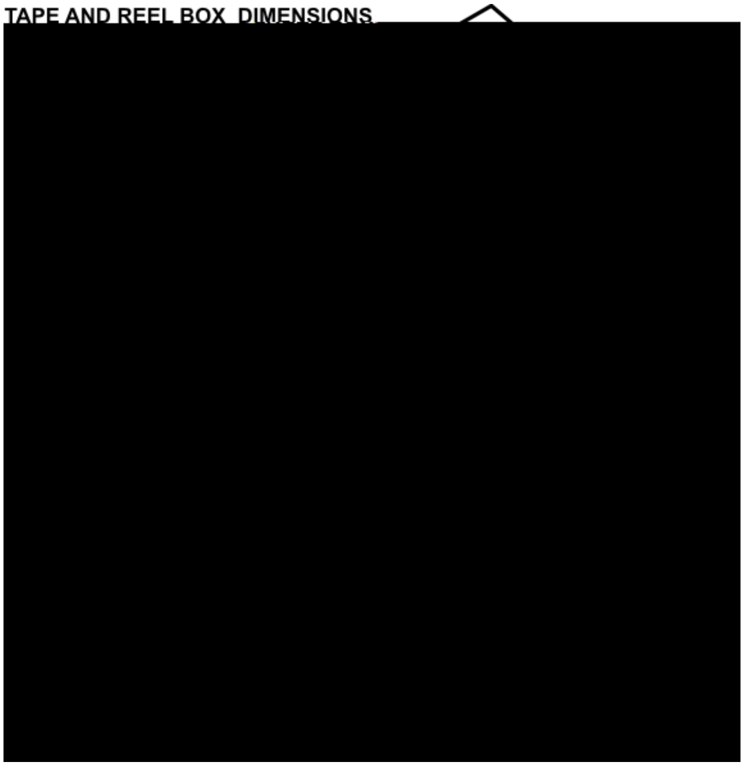
TAPE AND REEL INFORMATION



*All dimensions are nominal

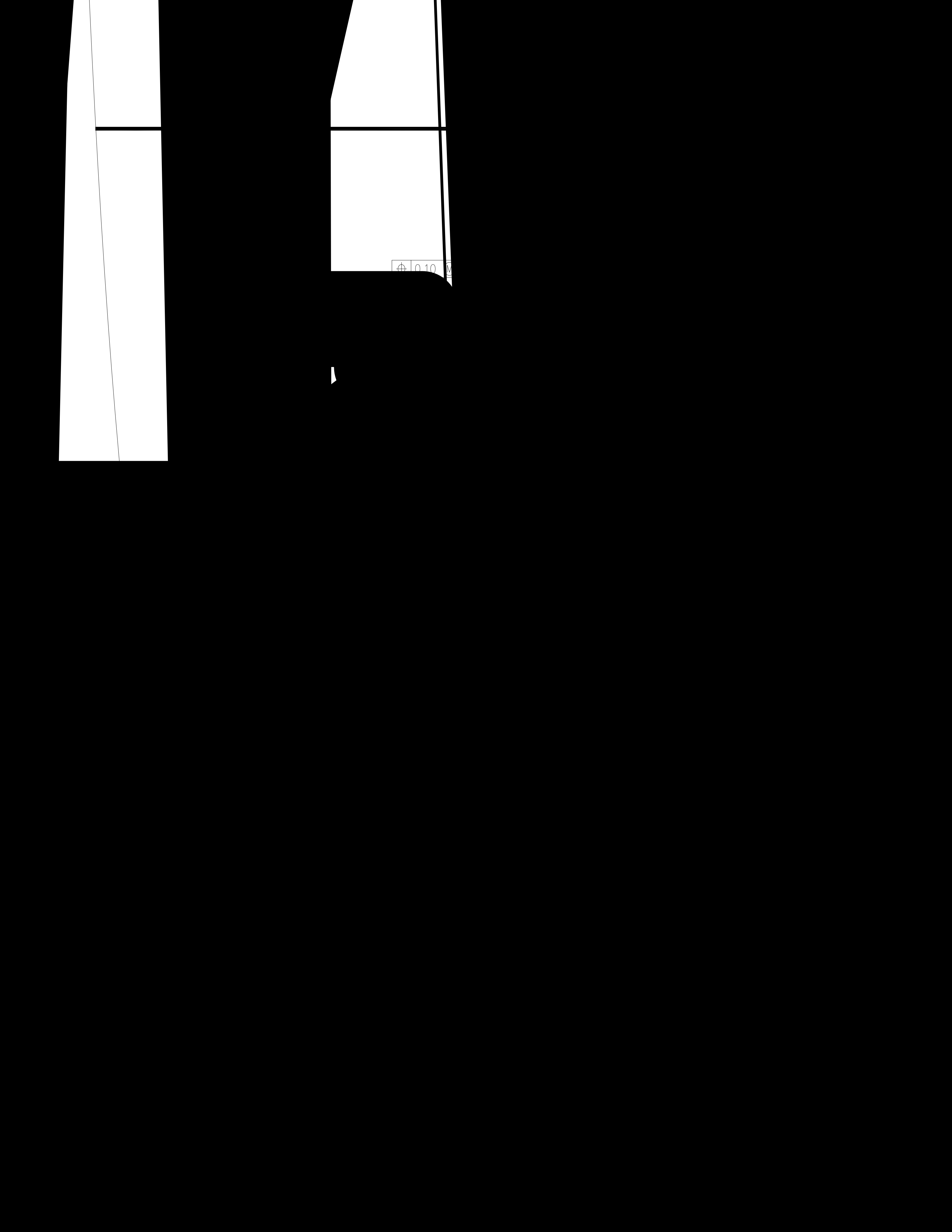
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ26501PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ26501PWR	TSSOP	PW	8	2000	367.0	367.0	35.0


0.10 M

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