SINGLE CELL Li-Ion AND Li-Pol BATTERY GAS GAUGE IC FOR PORTABLE APPLICATIONS (bqJUNIOR)

FEATURES

- **HDQ (bq27000) or I²C (bq27200) Communication**
- **Reports Accurate *Time-to-Empty* With Measured Load and Historical Maximum and Standby Loads**
- **Reports Temperature, Voltage, and Current**
- **High Accuracy Charge and Discharge Current Integration with Automatic Offset Calibration**
- **Requires No User Calibration**
- **Programmable Input/Output Port**
- **Internal User EEPROM Configuration Memory**
- **Automatic Capacity Reduction With Age**
- **Stable Oscillator Without External Components**
- **Dynamic End-of-Discharge Detection Delay to Allow Use in a High-Dynamic Load Environment**
- **Automatic Sleep Mode When Communication Lines are Low**
- **Available in a Small 3 mm x 4 mm QFN Package**
- **Five Low-Power Operating Modes**
  - **Active: < 90 µA**
  - **Sleep: < 2.5 µA**
  - **Ship: < 2 µA (bq27000 only)**
  - **Hibernate: < 1.5 µA**
  - **Data Retention: < 20 nA**

APPLICATIONS

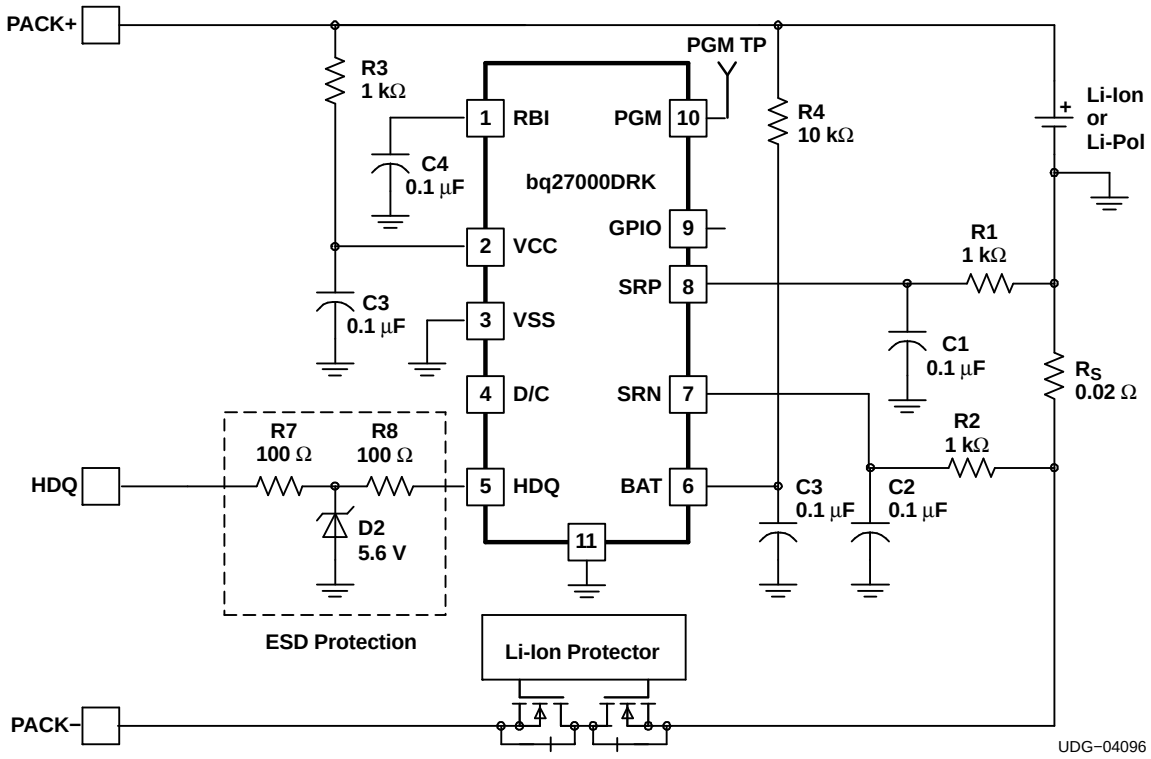
- **PDA**
- **Smart Phones**
- **MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Handheld Devices**

DESCRIPTION

The bqJUNIOR™ series are highly accurate stand-alone single-cell Li-Ion and Li-Pol battery capacity monitoring and reporting devices targeted at space-limited, portable applications. The IC monitors a voltage drop across a small current sense resistor connected in series with the battery to determine charge and discharge activity of the battery. Compensations for battery temperature, self-discharge, and discharge rate are applied to the capacity measurments to provide available time-to-empty information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or learned, in the course of a discharge cycle from full to empty. Internal registers include current, capacity, time-to-empty, state-of-charge, cell temperature and voltage, status, and more.

The bqJUNIOR can operate directly from single-cell Li-Ion and Li-Pol batteries and communicates to the system over a HDQ one-wire or I²C serial interface.

TYPICAL APPLICATION



ORDERING INFORMATION

TA	COMMUNICATION INTERFACE	PACKAGED DEVICES(1)	MARKINGS
-20°C to 70°C	HDQ	bq27000DRKR	27000
	I^2C	bq27200DRKR	27200

(1) The DRK package is available taped and reeled only. Quantities are 2,000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			bq27000 bq27200	UNITS
V_{CC}	Supply voltage	(with respect to V_{SS})	-0.3 to 7	V
V_{IN}	Input voltage	SRP, SRN, RBI, BAT (all with respect to V_{SS})	-0.3 to V_{CC}+0.3	
		HDQ, SCL, SDA, GPIO (all with respect to V_{SS})	-0.3 to 7	
		PGM (with respect to V_{SS}) during EEPROM programming	-0.3 to 22	
I_{SINK}	Output sink current	GPIO, SCL, SDA, HDQ	5	mA
T_A	Operating free-air temperature range		-20 to 70	°C
T_{stg}	Storage temperature range		-65 to 150	
T_J	Operating junction temperature range		-40 to 125	
	Lead temperature (soldering, 10 sec)		300	

CONDITIONS

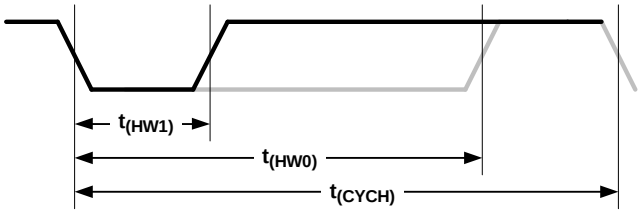
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range and supply voltage range (unless otherwise noted)

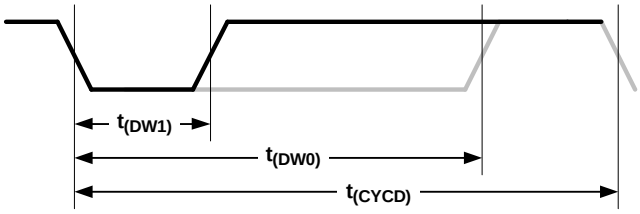
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STANDARD HDQ SERIAL COMMUNICATION TIMING (bq27000 only)						
$t_{(B)}$	Break timing		190			µs
$t_{(BR)}$	Break recovery		40			
$t_{(CYCH)}$	Host bit window		190			
$t_{(HW1)}$	Host sends 1		0.5		50	
$t_{(HW0)}$	Host sends 0		86		145	
$t_{(RSPS)}$	bqJUNIOR to host response		190		320	
$t_{(CYCD)}$	bqJUNIOR bit window		190		250	
$t_{(DW1)}$	bqJUNIOR sends 1		32		50	
$t_{(DW0)}$	bqJUNIOR sends 0		80		145	
STANDARD I^2C SERIAL COMMUNICATION TIMING (bq27200 only)						
t_r	SCL/SDA rise time				1	µs
t_f	SCL/SDA fall time				300	ns
$t_{w(H)}$	SCL pulse width (high)		4			µs
$t_{w(L)}$	SCL pulse width (low)		4.7			
$t_{su(STA)}$	Setup for repeated start		4.7			
$t_{d(STA)}$	Start to first falling edge of SCL		4			
$t_{su(DAT)}$	Data setup time		250			ns
$t_{h(DAT)}$	Data hold time		300			
$t_{su(STOP)}$	Setup time for stop		4			µs
$t_{(BUF)}$	Bus free time between stop and start		4.7			
$f_{(SCL)}$	Clock frequency				100	kHz
$t_{(BUSERR)}$	Bus error timeout		17.3		21.2	s

TIMING DIAGRAMS

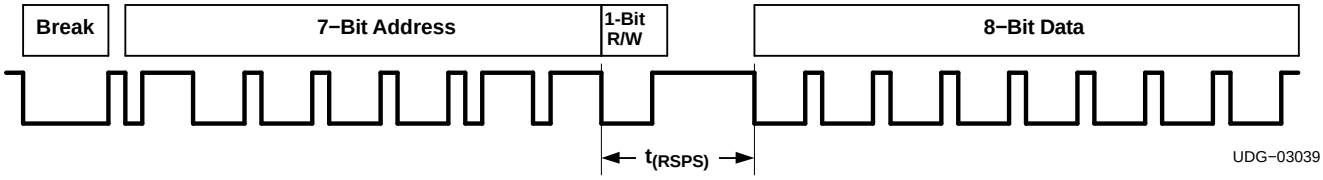
(a) Break and Break Recovery



(b) Host Transmitted Bit

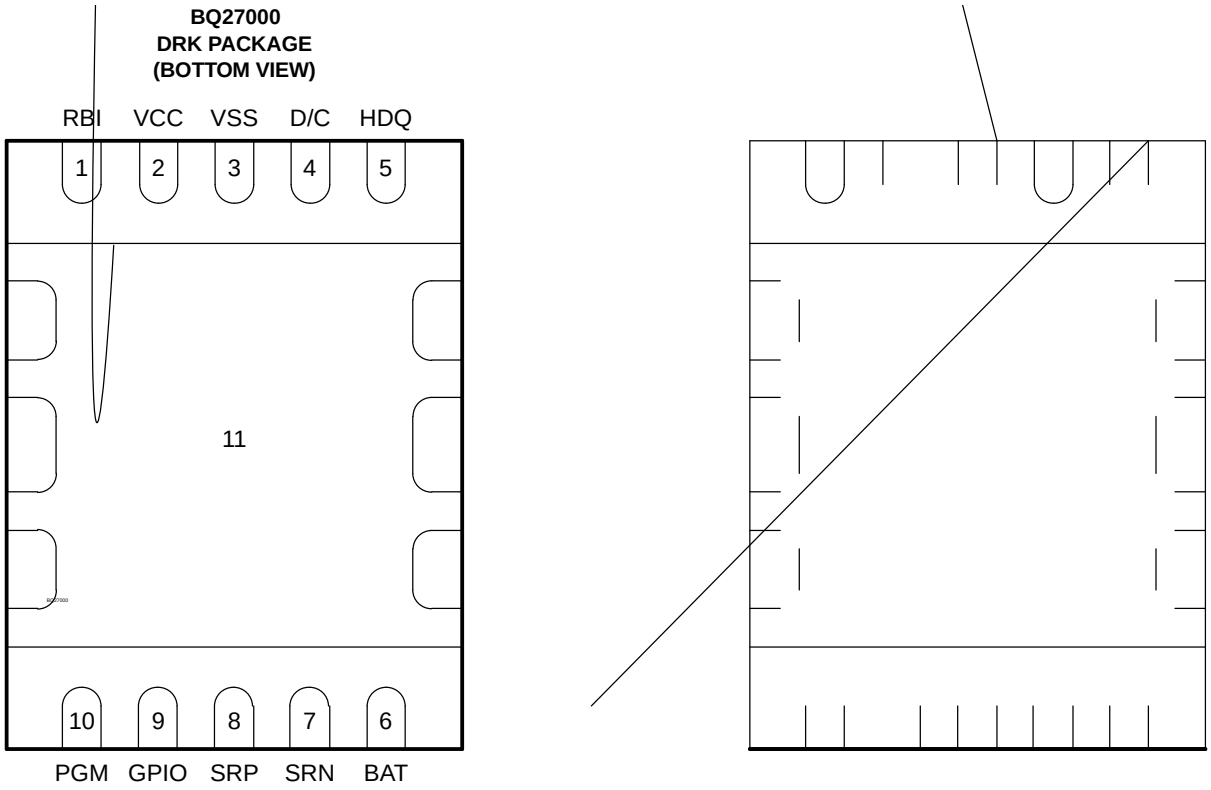


(c) bqJUNIOR Transmitted Bit

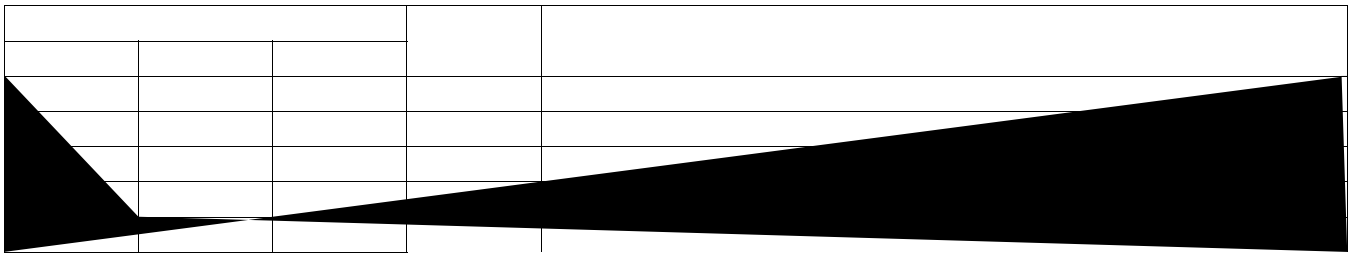


(d) bqJUNIOR to Host Response

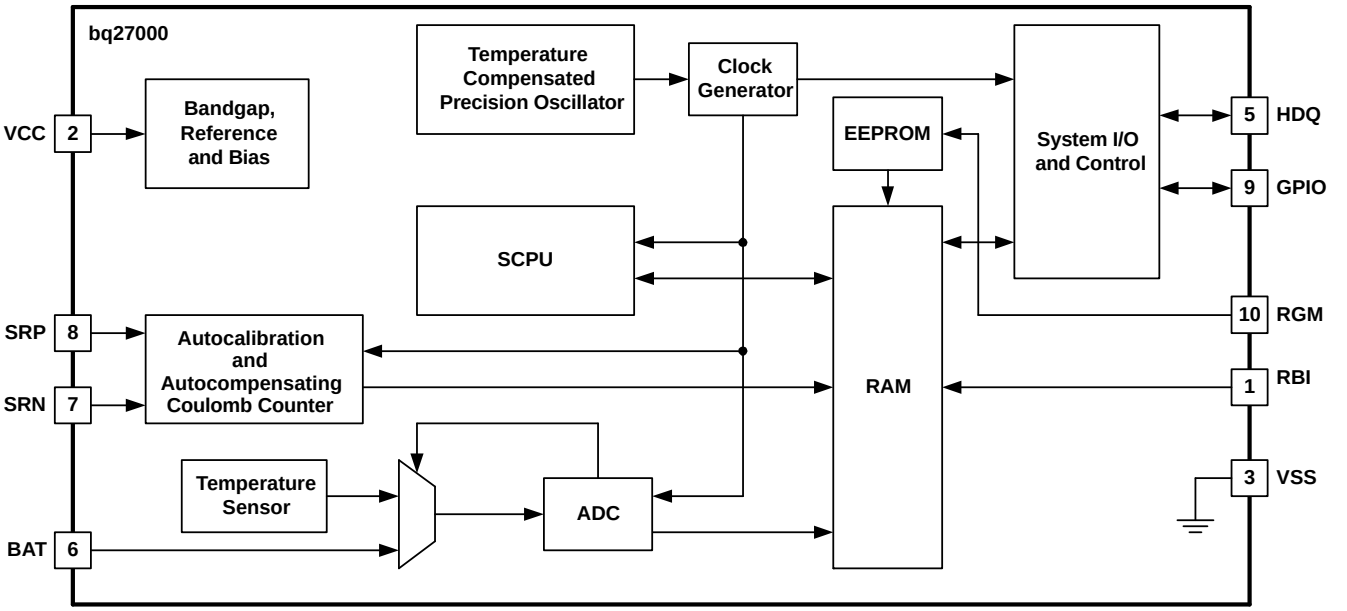
UDG−04122

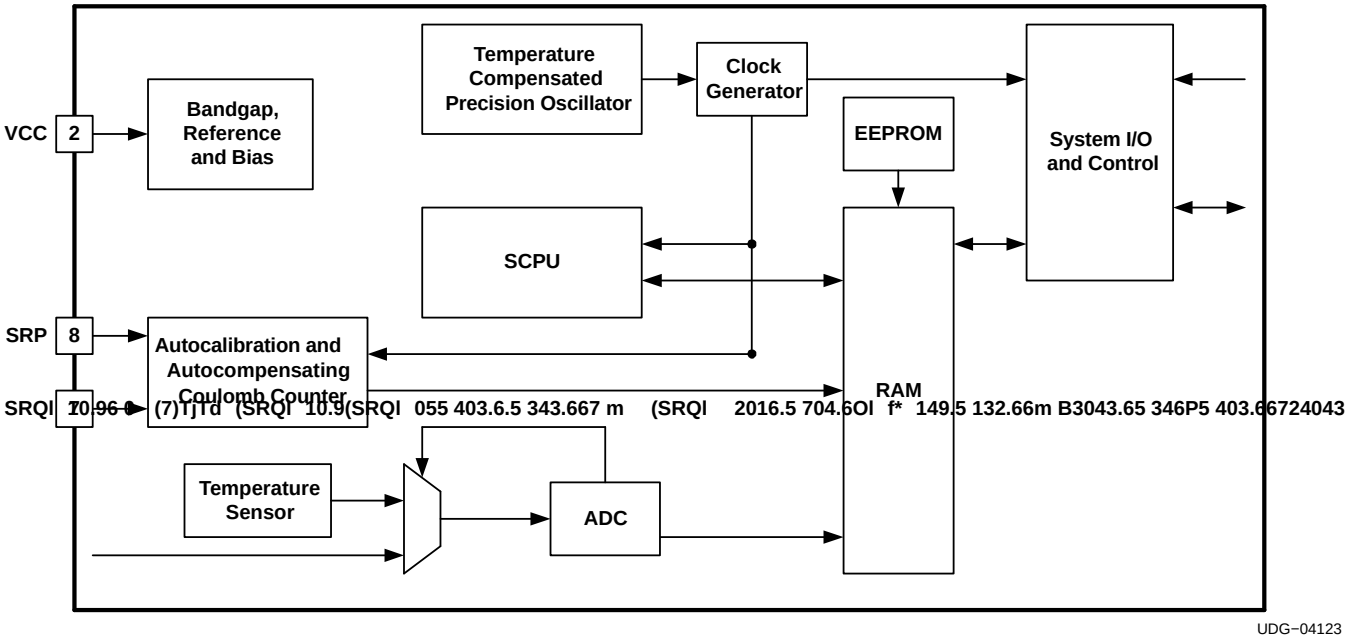


DEVICE INFORMATION



FUNCTIONAL BLOCK DIAGRAMS





FUNCTIONAL DESCRIPTION

The bqJUNIOR determines battery capacity by monitoring the amount of charge input to or removed from a Li-Ion or Li-Pol battery. The bqJUNIOR measures discharge and charge currents, monitors the battery for low voltage thresholds, and compensates for self-discharge, aging, temperature, and discharge rate. Current is measured across a small value series resistor between the negative terminal of the battery and the pack ground (see R_S in Figure 3). Available capacity is reported with a resolution of 3.57 µVh. Time-To-Empty reporting in minutes at standby, peak, actual, and at-rate currents allows the requirements for host-based calculations to be greatly reduced or eliminated; reading a single register pair provides useful and meaningful information to the end user of the application.

FUNCTIONAL DESCRIPTION (continued)

Figure 3 shows a typical application circuit. Differential sense of the voltage across the current sense resistor, R_S, improves device performance, leading to an improvement in reported time-to-empty accuracy. An internal, 3 µA pull-down on the HDQ or SDA and SCL lines ensures that the device detects a logic *0* on the communication lines and allows the device to automatically enter the low-power sleep mode when the system power is switched off or the pack is removed. A 100 kΩ pullup to V_{CC} can be added to the communication lines if this feature needs to be disabled. The bqJUNIOR can operate directly from a single Li-Ion or Li-Pol cell.

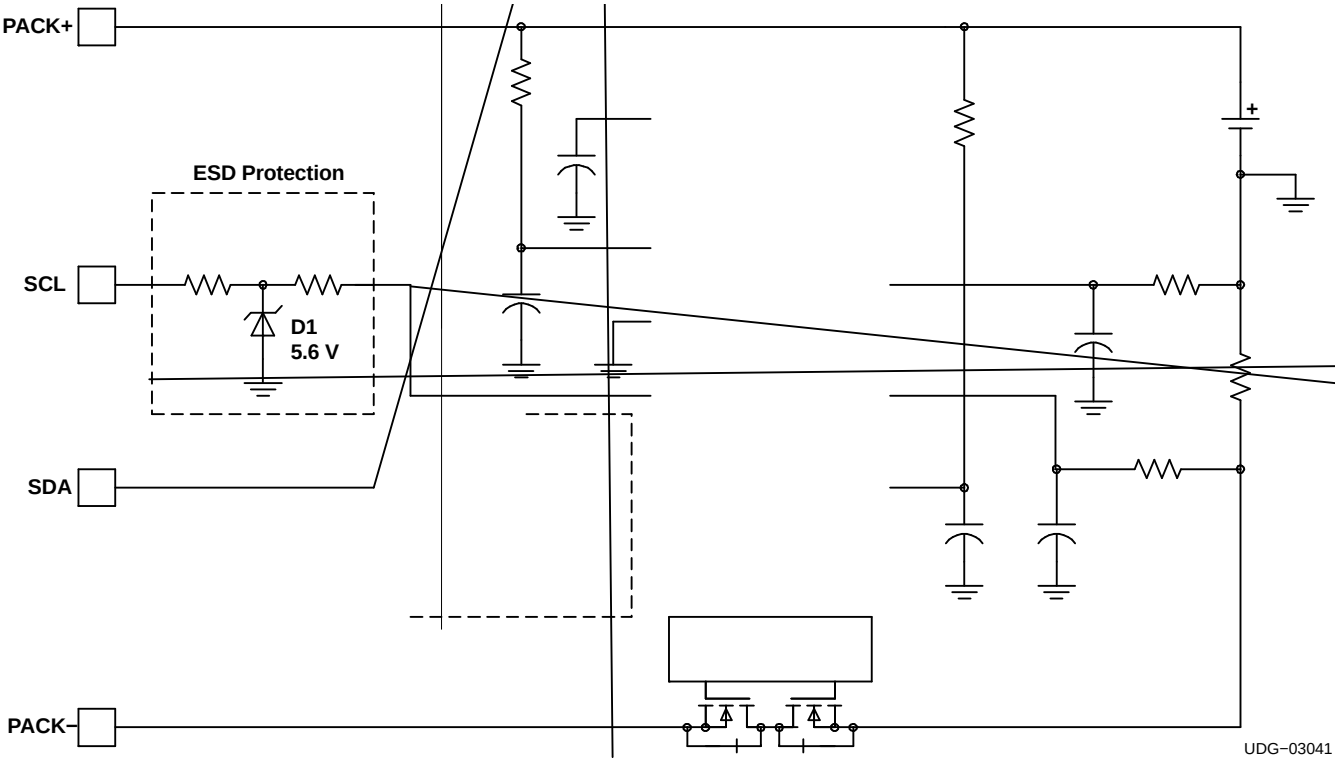


Figure 3. Typical Application Circuit (bq27200)

Measurements

As shown in the functional block diagram, the bqJUNIOR uses a dedicated fully differential Delta-Sigma Coulomb Counter (DSCC) for charge and discharge current and coulometric measurements and an analog-to-digital converter (ADC) for battery voltage and temperature measurements. Both DSCC and ADC are automatically compensated for offset. No user calibration or compensation is required. An EEPROM offset value can be programmed to compensate for contributions to the DSCC offset due to the PCB layout.

Charge and Discharge Coulometric and Current Measurements

The bqJUNIOR uses a DSCC to perform a continuous integration of the voltage waveform across a small value sense resistor in the negative lead of the battery, as shown in Figure 3. The integration of the voltage across the sense resistor is the charge added or removed from the battery. Because the DSCC does a direct integration of the waveform, the shape of the current waveform through the sense resistor does not have any effect on the coulometric measurement accuracy. The low-pass filter that feeds the sense resistor voltage to the bqJUNIOR SRP and SRN inputs filters out system noise and does not affect the coulometric measurement accuracy, because the low-pass filter does not change the integrated value of the waveform. The bqJUNIOR also uses the DSCC to measure current. The reported current is determined by the average voltage across the sense resistor over a 5.12 second interval.

FUNCTIONAL DESCRIPTION (continued)

Offset Calibration

The offset voltage of the DSCC measurement must be very low to be able to measure small signal levels accurately. The bqJUNIOR provides an auto-calibration feature to cancel the internal voltage offset error across SRP and SRN for maximum charge measurement accuracy. **NO CALIBRATION IS REQUIRED**. External voltage offset error caused by the PCB layout cannot be automatically calibrated out by the gauge, but the external offset can be determined using a built-in user offset measurement command and can be

Digital Magnitude Filter

Voltage

Temperature

FUNCTIONAL DESCRIPTION (continued)

RBI Input

The RBI input pin is used with an external capacitor to provide backup potential to the internal registers when V_{CC} drops below $V_{(POR)}$. V_{CC} is output on RBI when V_{CC} is above $V_{(POR)}$, charging the capacitor. An optional 1 MΩ resistor can be added from the RBI pin to V_{CC}. This allows the IC to maintain RAM register data for an indefinite period when the battery voltage is below $V_{(POR)}$ and above 1.3 V. The bqJUNIOR checks for RAM corruption by storing a redundant copy of the high byte of NAC and a checkbyte computed from LMD, CYCL, CYCT, and other critical data. After a reset, the bqJUNIOR compares the redundant NAC and checkbyte values. If the checks are correct, NAC, LMD, CYCL, and CYCT are retained; and the CI bit in FLAGS is left unchanged. If these checks are not correct, NAC, CYCL, and CYCT are cleared; LMD is initialized from EEPROM and the CI bit in FLAGS is set to 1. All other RAM is initialized on all resets.

GPIO

The GPIO pin can be used as an input or an output. The initial state can be established by programming bit 7 in the PKCFG EEPROM location. The input/output state can be changed at any time by changing the value in bit 7 of MODE.

Layout Considerations

The auto-calibrating DSCC approach effectively cancels the internal offset voltage within the bqJUNIOR, but any external offset caused by PCB layout must be programmed in the EEPROM to be cancelled. The magnitude and variability of the external offset makes it critical to pay special attention to the PCB layout. To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the filter capacitors from SRP and SRN to V_{SS} should be placed as closely as possible to the bqJUNIOR, with short trace runs to both signal and V_{SS} pins. All low-current V_{SS} connections should be kept separate from the high-current discharge path from the battery and should tie into the high-current trace at a point directly next to the sense resistor. This should be a trace connection to the edge or inside of the sense resistor connection, so that no part of the V_{SS} interconnections carry any load current and no portion of the high-current PCB trace is included in the effective sense resistor (i.e. Kelvin connection).

Gas Gauge Operation

Figure 4 illustrates an operational overview of the gas gauge function.

The bqJUNIOR measures the capacity of the battery during actual use conditions and updates the Last Measured Discharge (LMD) register with the latest measured value. The bqJUNIOR retains the learned LMD value unless a full reset occurs. By measuring the capacity that the battery delivers as it is discharged from full to the EDV1 threshold without any disqualifying events, the bqJUNIOR learns the capacity of the battery. The bqJUNIOR does not need to learn a new capacity on each full discharge, and only a discharge during normal use conditions should be used to learn a new capacity. In the event that some abnormal situation occurs that could cause a significant reduction in learned capacity, the LMD value is restricted to a maximum LMD learn-down during any single learning discharge of LMD/8. The Capacity Inaccurate (CI) bit in FLAGS is cleared after a learning cycle. This bit remains cleared unless a full reset occurs or the cycle count since the last learning cycle (CYCL) reaches a count of 32.

The *full* condition is defined as Nominal Available Capacity (NAC) = LMD. The Valid Discharge Flag (VDQ) in the FLAGS register is set when this condition occurs and remains set until the learning discharge cycle completes or an event occurs that disqualifies the learning cycle.

The learning discharge cycle completes when the battery is discharged to the condition where VOLT ≤ EDV1 threshold. The EDV1 threshold should be set at a voltage that ensures at least 6.25% of battery capacity below that threshold. The EDVF threshold should be set at a voltage that the system sees as the zero-capacity battery voltage. The bqJUNIOR EDV detection is designed to prevent premature detection of the EDV thresholds due to dynamic load variations. EDV detection has a dynamically adjusted delay of up to 21.5 s with RSOC ≥ 6% and down to 3 s when RSOC = 0%.

The bqJUNIOR does not learn the capacity between EDV1 and EDVF thresholds, but assumes that the capacity is 6.25% of LMD; so, care should be taken to set EDV1 based on the characteristics of the battery. The measured LMD value is determined by measuring the capacity delivered from the battery from NAC = LMD until VOLT = EDV1, plus LMD/16 to account for the 6.25% capacity remaining below the EDV1 threshold.

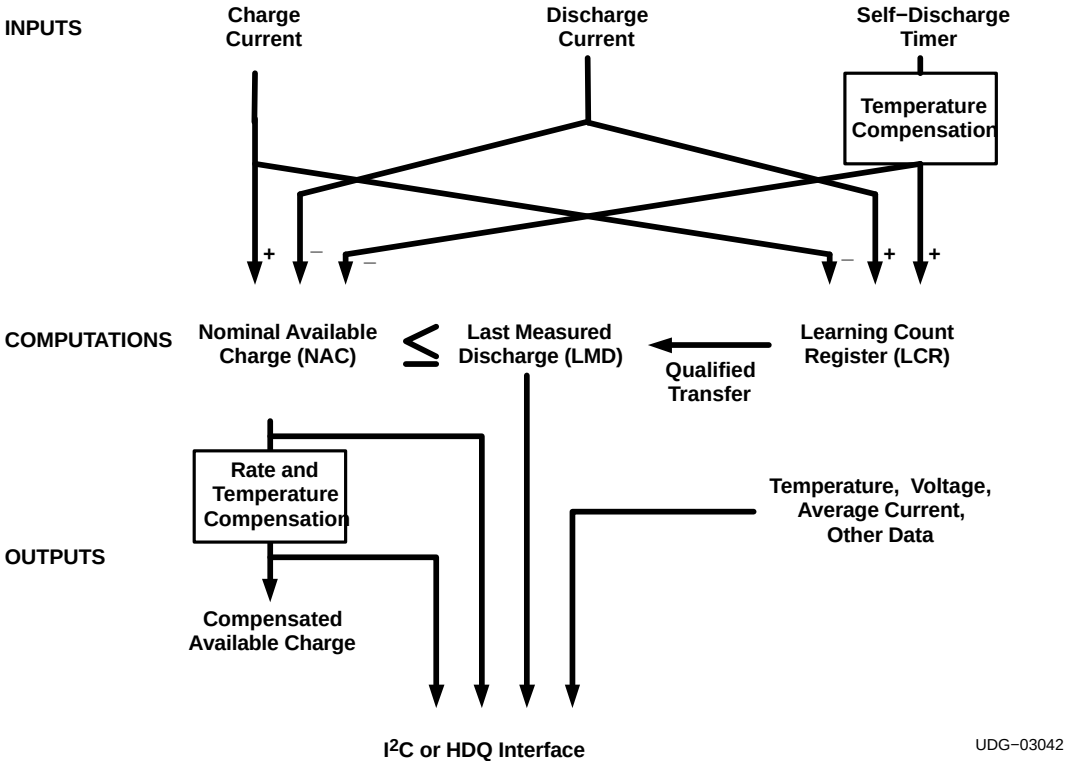
FUNCTIONAL DESCRIPTION (continued)

A learning cycle can be disqualified by any of the following conditions:

1. Cold temperature: Temperature ≤ TCOMP[3:0] (°C) when the EDV1 threshold voltage is reached.
2. Light load: A capacity learning cycle is disqualified if average current is less than or equal to 2 times the initial standby load when the EDV1 threshold voltage is reached.
3. Fast voltage drop: VOLT ≤ (EDV1 – 256 mV) before EDV1 is set.
4. Excessive charging: Cumulative Charge > 255 NAC counts (910 µVh) during a learning discharge cycle (alternating discharge/charge/discharge before EDV1 is set).
5. Reset: VDQ is cleared on all resets.
6. Excessive self-discharge: NAC reduction from self-discharge estimate (0.195%) performed 64 times.
7. Self-discharge at termination of learning cycle. If self-discharge estimate causes NAC ≤ LMD/16, VDQ is

LM (of) Tj 0 0 1 93.82 232.2 Tm /F2 -10 Tif (all)Tj 1 0 0 1 273.82 232.2 Tm /F2 -10 Tif (is)Tj 1 0 0 1 143.82 232.2 Tm /F2 -10 Tf (if)Tj

NAC is adjusted by charge and discharge coulometric measurements except when battery full or empty conditions are detected. NAC = LMD is forced when IMIN = 1 (full detection) unless Temperature ≤



Register Interface

FUNCTIONAL DESCRIPTION (continued)

Table 1. bq27000/bq27200 Memory Map

ADDRESS	NAME	FUNCTION	UNITS	ACCESS

APPLICATION INFORMATION

Control and MODE Registers (CTRL/MODE) — Address 0x00/0x01

The device control register is used by the host system to request special operations by the bqJUNIOR. The highest priority command set in the MODE register is performed when the host writes data 0xA9 or 0x56 as indicated to the control register. The CTRL register is cleared when the command is accepted. The host must set the appropriate command bit in MODE before sending the command key to CTRL.

Mode Register (MODE) — Address 0x01

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMMAND KEY = 0xA9	GPIEN	GPSTAT	WRTNAC	DONE	PRST	POR	FRST	SHIP(1)
COMMAND KEY = 0x56	GPIEN	GPSTAT	CEO	CIO	N/A	POR	N/A	N/A

(1) bq27000 only

GPIEN GPIEN sets the state of the GPIO pin. A *1* configures the GPIO pin as input, while a *0* configures the GPIO pin as an open-drain output. This bit is initialized to the value of bit 7 of the PKCFG register in the EEPROM. The user should keep this bit set or cleared as desired when other bits in this register are written.

GPSTAT GPSTAT sets the state of the open drain output of the GPIO pin (GPIEN = 0). A *1* turns off the open drain output, while a *0* turns the output on. This bit is set to *1* on POR. When the GPIO pin is an input (GPIEN=1), this bit returns the logic state of the GPIO pin. The user should keep this bit set or cleared as desired when other bits in this register are written.

WRTNAC WRTNAC is used to transfer data from the AR registers to NAC. Other registers are updated as appropriate. This command is useful during the pack manufacture and test to initialize the gauge to match the estimated battery capacity.

DONE DONE is used to write NAC equal to LMD. Useful if the host uses a charge termination method that does not allow the monitor to detect the taper current. The host system could use this command when the charging is complete to force update of internal registers to a full battery condition.

PRST Partial reset. This command requests a reset of all RAM registers except NAC, LMD, and the CI bit in FLAGS. This command is intended for manufacturing use.

POR The POR status bit is set to *1* by the bqJUNIOR following a Power on Reset. This is a flag to the host that V_{CC} was less than $V_{(POR)}$ and caused a reset. The bit is cleared to *0* by the bqJUNIOR when a full charge condition is reached or it may be cleared by the host. The bit is also cleared to *0* after exiting from EEPROM programming or ship. The host may set this bit, but it has no effect on the bqJUNIOR operation. The user should keep this bit set or cleared as desired when other bits in this register are set.

FRST Full reset. This command bit requests a full reset. A full reset reinitializes all RAM registers, including the NAC, LMD, and FLAGS registers. This command is intended for manufacturing use.

SHIP This command bit requests that the device (bq27000 only) should be put in ship mode. See the *Power Mode* section for a description of the ship mode. This command is intended for manufacturing use.

CEO This command bit requests that the external offset value is measured. Care should be taken to insure that no charge or discharge current flows during the time this measurement is made. The external offset value is the total offset of the DSCC plus any external PCB affects. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use.

CIO This command bit requests that the internal offset value is measured. The internal offset value is the offset of the DSCC with an internal short applied from SRP to SRN. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use.

WRTNAC, DONE, PRST, FRST, and SHIP (bq27000 only) commands are prioritized in bit order. This means

that WRTNAC (bit 5) has higher priority than DONE (bit 4); PRST (bit 3) has higher priority than FRST (bit 1), and so on. Only the highest priority mode set is enabled each time the CTRL register is written with data 0xA9, and the firmware clears all other mode bits and the CTRL register when that action is complete. The host system must make two writes for every mode to be enabled: one write to the MODE register to set the appropriate bit and a second write to the CTRL register to signal that the command in the mode register should be executed.

The CIO value may be subtracted from the CEO value to determine the external board offset. This value can be programmed into the PKCFG[4-2] in the EEPROM for automatic compensation of this external offset value.

At-Rate Registers (ARL/ARH) — Address 0x02/0x03

The host can write the current in units of 3.57 µV per bit to this register for predictive calculation time-to-empty. The part uses this value to predict the time-to-empty at any desired current; it does not affect the time-to-empty calculation based on the actual

At Rate Time-to-Empty Registers (ARTTEL/ARTTEH) — Address 0x04/0x05

Reported Temperature Registers (TEMPL/TEMPH) — Address 0x06/0x07

Reported Battery Voltage registers (VOLTL/VOLTH) — Address 0x08/0x09

Status Flag Register (FLAGS) — Address 0x0A

CI Capacity Inaccurate flag. A *1* indicates that the firmware has not been through a valid learning cycle and is basing all calculations on initial design values programmed into EEPROM or that there have been at least 32 cycle-count increments since the last learning cycle. This bit is cleared only on a LMD update following a learning cycle. This bit is set to *1* on a full reset. The previous value is retained if no RAM corruption is detected after a reset.

CALIP Calibration-In-Progress flag. This flag is set whenever an automatic or commanded offset calibration measurement is being made. This bit is set to *0* on all resets.

VDQ Valid Discharge flag. A *1* indicates that the bqJUNIOR has met all necessary requirements for the firmware to learn the battery capacity. This bit clears to *0* on a LMD update or condition that disqualifies a learning cycle. This bit is cleared to *0* on all resets.

EDV1 First End-of-Discharge-Voltage flag. A *1* indicates that voltage on the BAT pin is less than or equal to the EDV1 voltage programmed in EEPROM and the battery has less than or equal to 6.25% of LMD capacity remaining. LMD updates immediately if the VDQ bit is set when this bit transitions from *0* to 1. This bit is cleared to *0* on all resets.

EDVF Final End-of-Discharge-Voltage flag. A *1* indicates that the battery has discharged to the empty capacity threshold. This bit is cleared to *0* on all resets.

The host system has read-only access to this register.

Relative State-of-Charge (RSOC) — Address 0x0B

RSOC reports the nominal available capacity as a percentage of the last measured discharge value (LMD). The equation is:

RSOC (%) = 100 * NAC/LMD

The host system has read-only access to this register.

Nominal Available Capacity Registers (NACL/NACH) — Address 0x0C/0x0D

This register pair increments during charge ($V_{SRP} > V_{SRN}$) if Voltage > EDVF threshold and decrements during discharge ($V_{SRP} < V_{SRN}$). The NAC registers are cleared by a reset if RAM corruption is detected. The register value is retained after a reset if RAM corruption is not detected. The host system has read-only access to this register pair. NAC is reported in units of 3.57 µVh per count.

Discharge Rate Compensated Available Capacity Registers (CACDL/CACDH) — Address 0x0E/0x0F

This register pair reports available capacity in the battery, compensated for discharge rate. This register pair follows NAC during charge and is reduced from NAC during discharge by an amount computed from AI and the discharge rate compensation value programmed into EEPROM. CACD is not allowed to increase while discharging, so that if the discharge rate decreases, the available capacity does not increase. CACD equals NAC if the CHGS bit is 1. If CHGS is 0, CACD is the smaller of the previous and new computed values. The host system has read-only access to this register pair. CACD is reported in units of 3.57 µVh per count.

Temperature Compensated CACD Registers (CACTL/CACTH) — Address 0x10/0x11

This register pair reports available capacity in the battery, compensated for both discharge rate and temperature. This register pair follows CACD during both charge and discharge unless the temperature has fallen below the threshold programmed into EEPROM. Once the temperature falls below the programmed threshold, the CACT value is reduced from CACD by an amount computed from ILMD and the temperature compensation constants programmed into EEPROM. This is the base capacity value used to calculate time-to-empty and compensated state-of-charge. The host system has read-only access to this register pair. CACT is reported in units of 3.57 µVh per count.

Last Measured Discharge Registers (LMDL/LMDH) — Address 0x12/0x13

Last measured discharge is the measured discharge capacity of the battery from full to empty. LMD is updated on a valid learning cycle, which occurs when the battery reaches the EDV1 level while the VDQ bit is set. It is used with NAC to calculate Relative State-Of-Charge (RSOC). The host system has read-only access to this register pair. LMD is reported in units of 3.57 µVh per count.

Average Current Registers (AIL/AIH) — Address 0x14/0x15

This register pair reports the magnitude of the average current through the sense resistor. The value is reported with a resolution of 3.57 µV per count. Use the following equation to convert the value to mA, where R_S is the sense resistor value in milliohms:

Average Current = (256*AIH + AIL) * 3.57/ R_S

The current reported is an average over the last 5.12 seconds. The host system has read-only access to this register pair.

Time-to-Empty Registers (TTEL/TTEH) — Address 0x16/0x17

This register pair reports calculated time-to-empty at the measured discharge rate. This value is based on the temperature and discharge rate compensated available charge and the average current. The equation to calculate TTE is:

TTE = 60 * CACT/AI

TTE is reported in minutes. The host system has read-only access to this register pair.

Time-to-Full Registers (TTFL/TTFH) — Address 0x18/0x19

This register pair reports calculated time-to-full at the measured charge rate. The time computed at the average current charge rate is extended by 50% to estimate the effect of the current taper. TTF is reported in minutes. The equation for TTF is:

TTF = 60 * 1.50 * (LMD-NAC)/AI

The host system has read-only access to this register pair.

Standby Current Registers (SIL/SIH) — Address 0x1A/0x1B

This register pair reports measured standby current through the sense resistor. The standby current is an adaptive measurement. Initially, the register pair reports the standby current programmed in EEPROM and after spending some time in standby, the register pair reports the measured standby current. The register value is updated every 5.12 seconds when the measured current is above the DMF threshold and is less than or equal to 2x the initial programmed standby current value. Each new SI value is computed as follows:

SI_{NEW} = (15/16)*SI_{OLD} + (1/16)*AI

This filter function allows the reported standby current to shift towards the actual measured current with a time constant of approximately 67 seconds. The value is reported with a resolution of 3.57 µV per bit. Use the following equation to convert the value to mA, where R_S is the sense resistor value in milliohms:

Standby Load Current = (256*SIH + SIL) * (3.57/ R_S)

The host system has read-only access to this register pair.

Standby Time-to-Empty Registers (STTEL/STTEH) — Address 0x1C/0x1D

This register pair reports calculated time-to-empty at the measured standby current value. This value is based on the nominal available charge and the standby current. STTE is reported in minutes. STTE is calculated by:

STTE = 60 * NAC/SI

The host system has read-only access to this register pair.

Max Load Current Registers (MLIL/MLIH) — Address 0x1E/0x1F

Max Load Time to Empty Registers (MLTTEL/MLTTEH) — Address 0x20/0x21

Available Energy Registers (SAEL/SAEH) — Address 0x22/0x23

Average Power Registers (APL/APH)

Cycle Count Since Learning Cycle Registers (CYCLL/CYCLH) — Address 0x28/0x29

CYCL is the cycle count since the last learning cycle. Each count indicates an increment of CYCT since there was a learning cycle. This register is cleared every time there is a learning cycle. When this count reaches 32, it forces the CI flag in FLAGS to a 1. The host system has read-only access to this register pair.

Cycle Count Total Registers (CYCTL/CYCTH) — Address 0x2A/0x2B

CYCT is the cycle count since a full reset. A full reset clears this register. Each count indicates a cumulative discharge equal to the Design Capacity (256 * ILMD). The host system has read-only access to this register pair.

Compensated State-of-Charge (CSOC) — Address 0x2C

CSOC reports the compensated available capacity as a percentage of the last measured discharge value (LMD). The equation is:

CSOC (%) = 100 * CACT/LMD

The host system has read-only access to this register.

Reserved Registers

Addresses 0x2D — 0x6D and Address 0x6F — 0x75 are reserved and cannot be written by host.

EEPROM Enable Register (EE_EN) — Address 0x6E

This register is used to enable host writes to EEPROM data locations (addresses 0x76 — 0x7F). The host must write data 0xDD to this register to enable EEPROM programming. See the *Programming the EEPROM* section for further information on programming the EEPROM bytes. Care should be taken to insure that no value except 0xDD is written to this location.

EEPROM Data Registers (EE_DATA) — Address 0x76 — 0x7F

The EEPROM data registers contain information vital to the performance of the device. These registers are to be programmed during pack manufacturing to allow flexibility in the design values of the battery to be monitored. The EEPROM data registers are listed in Table 2. Detailed descriptions of what should be programmed follow. See the *Programming the EEPROM* section for detailed information on writing the values to EEPROM.

Table 2. bq27000/bq27200 EEPROM Memory Map

Address	Name	Function
0x7F	TCOMP	Temperature compensation constants, OR, ID#1
0x7E	DCOMP	Discharge rate compensation constants, OR, ID#2
0x7D	IMLC	Initial max load current, OR, ID#3
0x7C	PKCFG	Pack configuration values
0x7B	TAPER	Aging estimate enable [7], charge termination taper current [6:0]
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants
0x79	ISLC	Initial standby load current
0x78	SEDV1	Scaled EDV1 threshold
0x77	SEDVF	Scaled EDVF threshold
0x76	ILMD	Initial last measured discharge high byte

Initial Last Measured Discharge High Byte (ILMD) — Address 0x76

This register contains the scaled design capacity of the battery to be monitored. The equation to calculate the initial LMD is:

ILMD = Design Capacity(mAh) * R_S(mΩ) / (256*3.57)

where R_S is the value of the sense resistor used in the system. This value is used to initialize the high byte of LMD. The initial low byte value of LMD is 0.

Scaled EDVF Threshold (SEDVF) — Address 0x77

This register contains the scaled value of the threshold for zero battery capacity. To calculate the value to program, use the following equation:

SEDVF = Design EDVF(mV)/8 – 256

Scaled EDV1 Threshold (SEDV1) — Address 0x78

This register contains the scaled value of the voltage when the battery has 6.25% remaining capacity. When the battery reaches this threshold during a valid discharge, the device learns the full battery capacity, including the remaining 6.25%. See the *bqJUNIOR Capacity Learning* section for more information on the learning cycles of the device. To calculate the value to program, use the following equation:

SEDV1 = Design EDV1(mV)/8 – 256

Initial Standby Load Current (ISLC) — Address 0x79

This register contains the scaled, end-equipment-design standby current. On a reset or POR, this value is transferred to the SI register and is used to calculate Standby Time-to-Empty. The gauge learns a new standby load if the discharge activity is above the DMF threshold and less than or equal to 2 times the initial standby load.

A capacity learning cycle is disqualified if average current is less than or equal to 2 times the initial standby load when the EDV1 threshold voltage is reached. The equation for programming this value is:

ISLC = Design Standby Current (mA) * R_S(mΩ) / 7.14

where R_S is the value of the sense resistor used in the system.

Digital Magnitude Filter and Self-Discharge Values (DMFSD) — Address 0x7A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DMF[3]	DMF[2]	DMF[1]	DMF[0]	SD[3]	SD[2]	SD[1]	SD[0]

DMF[3:0] Sets the digital magnitude filter threshold. See the *bqJUNIOR Digital Magnitude Filter* section for more information on the function of the DMF. The value to be programmed is: DMF[3:0] = Design Threshold/4.9

SD[3:0] Sets the self-discharge rate %/day value at 25°C. The value to be programmed is: SD[3:0] = 1.61/Design SD

NAC is reduced with an estimated self-discharge correction to adjust for the expected self-discharge of the battery. This estimation is performed only when the battery is not being charged. The rate programmed in EEPROM for DMFSD determines the self-discharge when 20°C ≤ TEMP < 30°C. The self-discharge estimation is doubled for each 10°C decade hotter than the 20-30°C decade, up to a maximum of 16 times the programmed rate for TEMP ≥ 60°C and is halved for each 10°C decade colder than the 20-30°C decade, down to a minimum of 1/4th the programmed rate for TEMP < 0°C. The self-discharge estimation is performed by reducing NAC by NAC/512 at a time interval that achieves the desired estimation. If DMFSD is programmed with 8 decimal, the self-discharge rate is 0.195% per day in the 20-30°C decade. This is accomplished by reducing NAC by NAC/512 (100/512 = 0.195%) a single time every 23.3 hours (0.195 * 24/23.3 = 0.2). If temperature rises by 10°C, the 0.195% NAC reduction is made every 11.65 hours for a 0.4% per day reduction. If TAPER[7] = 1, capacity aging is enabled, and there is an LMD reduction of 0.1% (Design Capacity/1024) every time there are 8 NAC self-discharge estimate reductions without charging the battery to full.

Taper Current (TAPER) — Address 0x7B

This register contains the enable bit for the capacity aging estimate and the charge taper current value. The taper current value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming the taper current is:

TAPER[6-0] = Design Taper Current (mA) * R_S(mΩ)/228 µV

where R_S is the value of the sense resistor used in the system.

Discharge Rate Compensation

Temperature compensation, TCMP, is computed from these coefficients as follows:

TCMP = TCGN * ILMD(273 + TOFF - T)/4

where T is the temperature in °K and TCMP ≥ 0. CACT is then computed as follows:

CACT = CACD – TCMP

If PKCFG[0] = 1, the device assumes a fixed value of 0x7C for TCOMP, giving a temperature compensation gain of 0.68% DC/°C with an offset of 12°C. This frees the EEPROM location of 0x7F for use as a programmable identification byte.

Power Modes

The bqJUNIOR has five power modes:

Active Mode

During normal operation, the device is in active mode, which corresponds to the highest power consumption. Normal gas gauging is performed in this mode. If system requirements mandate that bqJUNIOR should not enter Sleep or Ship modes, then an external pullup resistor from V_{CC} to keep HDQ or CLK and DTA at a logic *1* is required on the bqJUNIOR side of the system. The resistor value chosen should be small enough to force a logic *1* even with the internal pulldown current and any external ESD protection circuitry loading.

Sleep Mode

This low power mode is entered when the HDQ or CLK and/or DTA line is pulled low for at least 18 seconds and the charge or discharge activity is below the DMF threshold. Normal gas gauging ceases, but battery self-discharge, based on the temperature when the device entered sleep mode, is maintained internally. The the device wakes every 43.6 minutes to update the temperature measurement and goes back to sleep after about 18 seconds if the HDQ or CLK and/or DTA line is still low and the charge or discharge activity is still below the DMF threshold. The bqJUNIOR has an internal 3 °A pulldown current on each communication line, eliminating the need to add external pulldown resistors to force a logic *0* on open communication lines.

When the device wakes, it stays in active mode long enough to confirm that the charge or discharge activity is still below the digital magnitude filter threshold. This is meant to minimize possible error if the battery pack is removed from the end equipment for a short period of time and then reinserted, and there is not a transient on the communication lines to pull the device into the active mode. This is an issue only if the system has some current drain from the battery even though the communication lines are low. The gauge reenters sleep mode when the charge or discharge activity falls below the digital magnitude filter threshold.

When all communication lines are pulled high, the device leaves the sleep mode. If the DMF threshold is set to zero and a communication line is pulled low, the device does not enter sleep mode until the average current value is less than 3.57 µV/Rsr.

If the battery pack can be removed and placed on an external charger, the charger should have a pull-up resistor on the HDQ or SCL and SDA lines to wake the part from sleep. A 100 kΩ pullup resistor from communication line(s) to V_{CC} can be added in the battery pack to disable the sleep function.

Ship Mode (bq27000 only)

This low power mode is to be used when the pack manufacturer has completed assembly and test of the pack. The ship mode is enabled by setting the SHIP bit in the MODE register and issuing the control command (data 0xA9 to register 0x00). Ship mode is entered only when the ship mode is enabled and the HDQ or CLK and/or DTA line has been pulled low for at least 18 seconds. This allows the pack manufacturer to enable the

Hibernate Mode

Programming the EEPROM

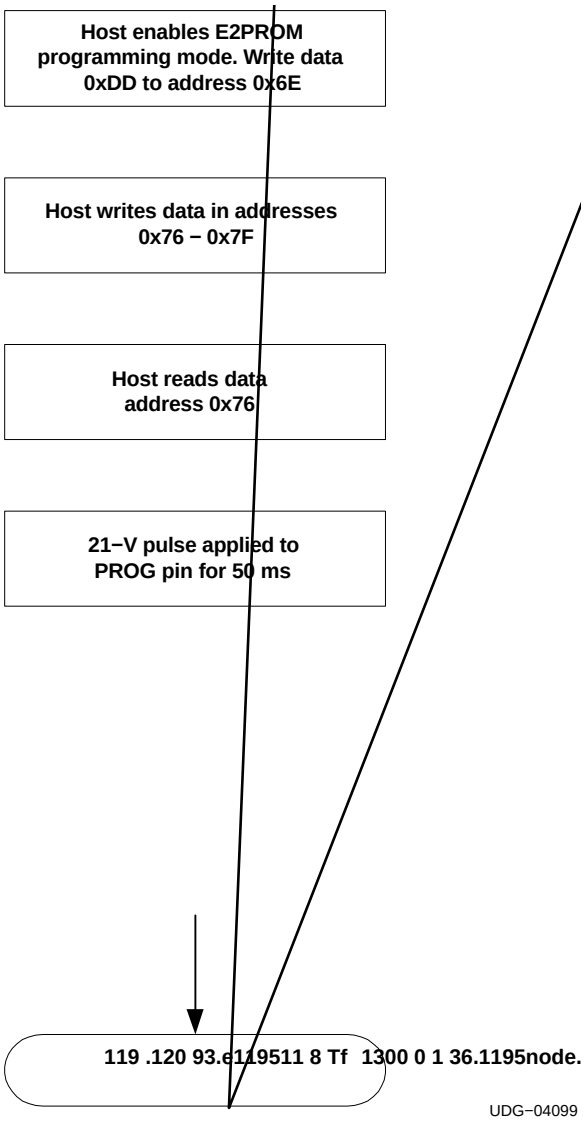


Figure 6. EEPROM Programming Flow

It is not required that addresses 0x76 — 0x7F be programmed at the same

Communicating With the bq27000 (HDQ interface)

If a communication timeout occurs (for example, if the host waits longer than $T_{(RSPS)}$ for the bq27000 to respond) or if this is the first access command, then a BREAK should be sent by the host. The host may then resend the command. The bq27000 detects a BREAK when the HDQ pin is driven to a logic-low state for a time $T_{(B)}$ or greater. The HDQ pin then returns to its normal ready-high logic state for a time $T_{(BR)}$.The bq27000 is then ready for a command from the host processor.

The return-to-one data-bit frame consists of three distinct sections:

1. The first section starts the transmission by either the host or the bq27000 taking the HDQ pin to a logic-low state for a period equal to $T_{(HW1)}$ or $T_{(DW1)}$.
2. The next section is the actual data transmission, where the data should be valid for $T_{(HW0)}$- $T_{(HW1)}$ or $T_{(DW0)}$- $T_{(DW1)}$.
3. The final section stops the transmission by returning the HDQ pin to a logic-high state and holding it high until the time from bit start to bit end is equal to $T_{(CYCH)}$ or $T_{(CYCD)}$.

The HDQ line can remain high for an indefinite period of time between each bit of address or between each bit of data on a write cycle. After the last bit of address is sent on a read cycle, the bq27000 starts outputting the data after $T_{(RSPS)}$ with timing as specified. The serial communication timing specification and illustration sections give the timings for data and break communication. Communication with the bq27000 always occurs with the least-significant bit being transmitted first.

Plugging in the battery pack can be seen as the start of a communication due to contact bounce. It is recommended that each communication or string of communications be preceded by a break to reset the HDQ engine.

Command byte

The Command byte of the bqJUNIOR consists of eight contiguous valid command bits. The command byte contains two fields: W/R Command and address. The Command byte values are shown as follows:

7	6	5	4	3	2	1	0
W/R	AD6	AD5	AD4	AD3	AD2	AD1	AD0

W/R Indicates whether the command bytes is a read or write command. A *1* indicates a write command and that the following eight bits should be written to the register specified by the address field of the Command byte, whereas a *0* indicates that the command is a read. On a read command, the bqJUNIOR outputs the requested register contents specified by the address field portion of the Command byte.

AD6-AD0 The seven bits labeled AD6—AD0 containing the address portion of the register to be accessed.

Reading 16-bit Registers

Because 16-bit values are read only 8 bits at a time with the HDQ interface, it is possible that the device can update the register value between the time the host reads the first and second bytes. To prevent any system issues, any 16-bit values read by the host should be read with the following procedure.

1. Read high byte (H0).
2. Read low byte (L0).
3. Read high byte (H1).
4. If H1=H0, then valid result is H0, L0.
5. Otherwise, read low byte (L1) and valid result is H1, L1.

This procedure assumes that the 3 or 4 reads are made more quickly than the update rate of the value. The maximum update rate of any value in the bq27000/bq27200 is 1.28 seconds.

The bq27200 circumvents this issue if a 16-bit value is read using the I^2C incremental read procedure. Both low and high bytes are captured simultaneously when the low byte is read.

Communicating with the bq27200 (I^2C interface)

The bq27200 supports the standard I^2C read, incremental read, quick read, and one byte write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively. (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop)

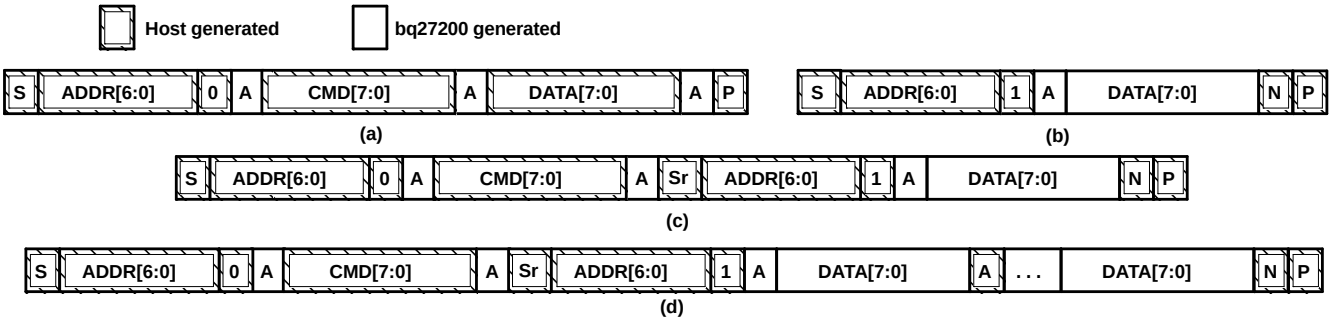
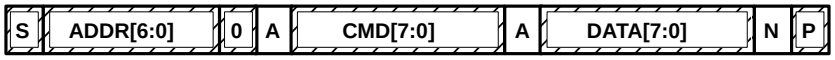


Figure 7. Supported I2C formats :
(a) 1-byte write; (b) quick read; (c) 1-byte read; (d) incremental read

The incremental read protocol is recommended for reading all 16-bit values, as this ensures that the 16-bit value is not updated during the time interval between reading the two bytes of data (see previous section on reading 16-bit values). The quick read returns data at the address indicated by the internal address pointer. The address pointer is incremented after each data byte is read or written. Reading an even address causes the communication engine to simultaneously capture the data byte from the requested even address and the data byte from the next odd address, and the address pointer is incremented twice. The data byte captured from the next odd address is output if the communication continues, without a stop, after the host acknowledges the even address byte.

Due to the memory map setup of the device, several boundary conditions must be enforced by the communication engine.

Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x7F (NACK command):

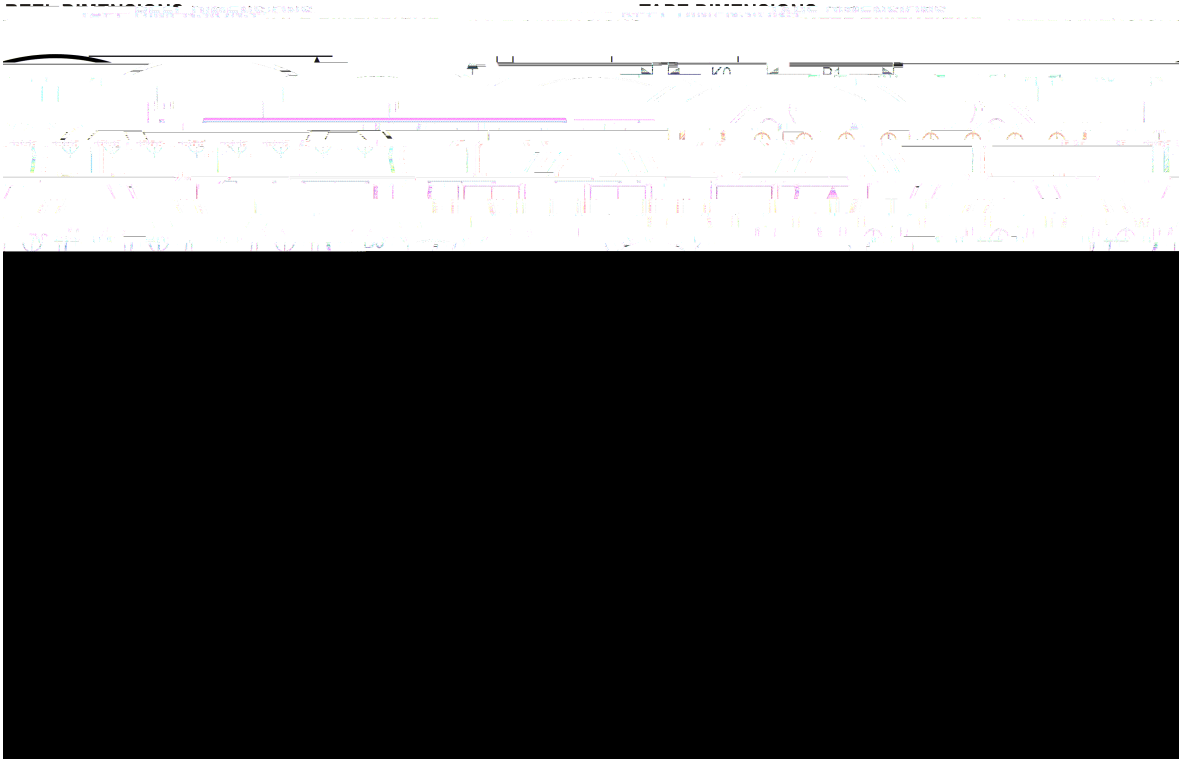
Attempt at incremental writes (NACK all extra data bytes sent):

Incremental read at the maximum allowed read address:

The I^2C engine releases both SDA and SCL if the I^2C bus is held low for $T_{(BUSERR)}$. If the bq27200 was holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I^2C engine enters the low-power sleep mode if the measured charge and discharge activity level are less than the DMF threshold.

PACKAGING INFORMATION

TAPE AND REEL INFORMATION

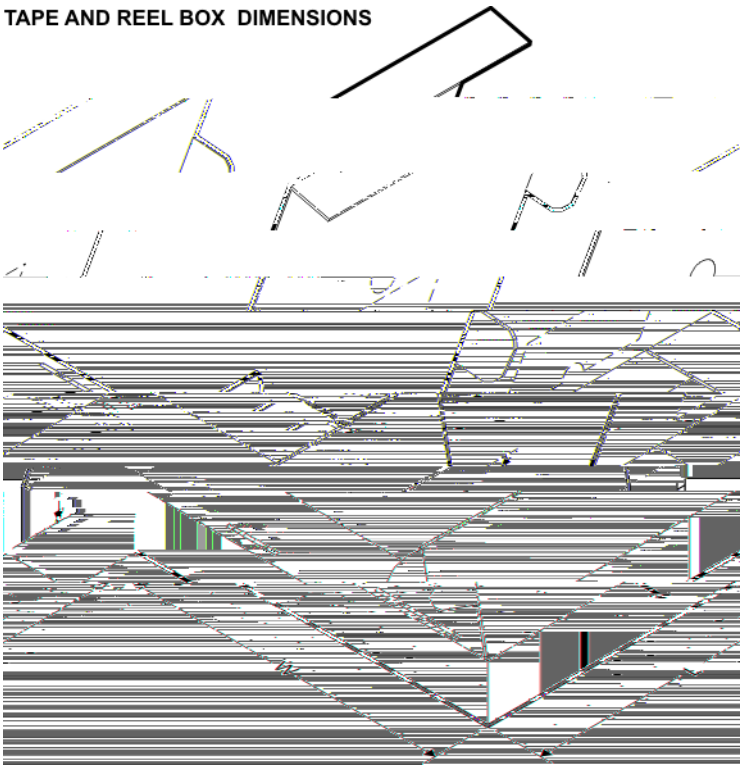


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27000DRKR	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q2
BQ27200DRKR	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q2

PACKAGE MATERIALS S.4.3 85.039 .6.6

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27000DRKR	VSON	DRK	10	3000	338.1	338.1	20.6
BQ27200DRKR	VSON	DRK	10	3000	338.1	338.1	20.6

DRK (S–PVSON–N10)

THERMAL INFORMATION

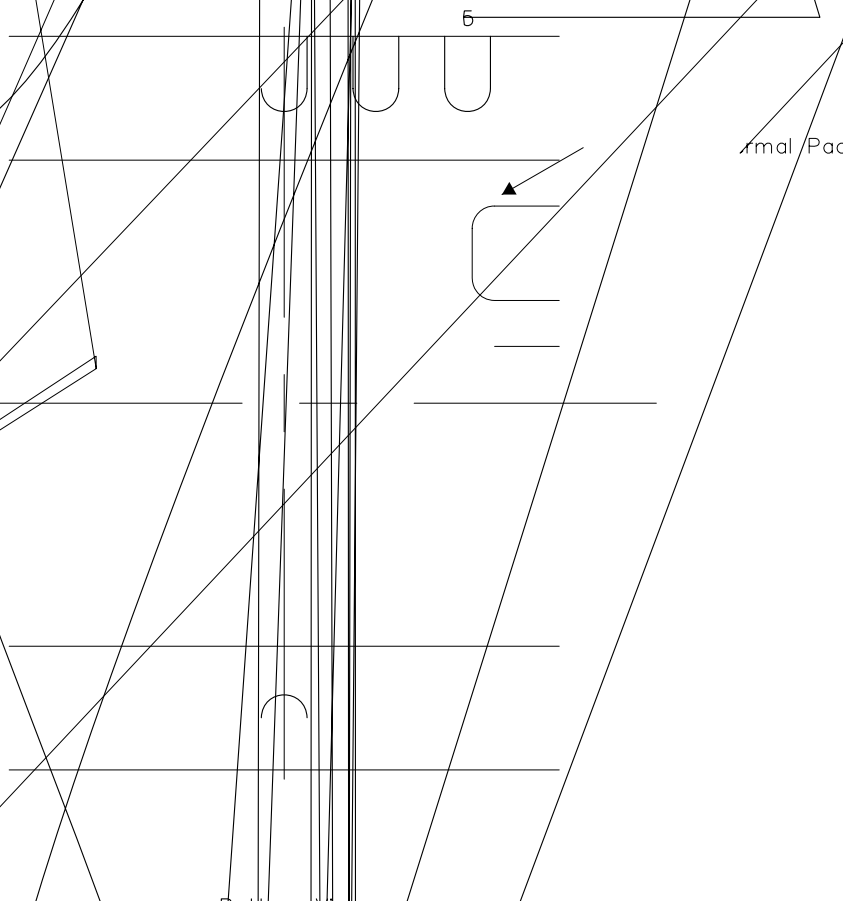
This package incorporates an exposed thermal pad that is desig
heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached

ansfer from the

integrated circuit (IC).

QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

ons for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

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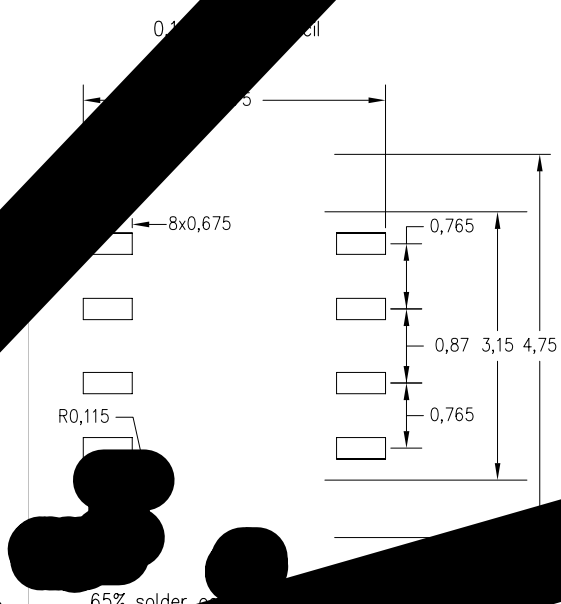

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