SYNCHRONOUS SWITCHMODE, LI-ION AND LI-POLYMER CHARGE-MANAGEMENT IC WITH INTEGRATED POWER FETs (bqSWITCHER™)

Check for Samples: bq24105-Q1

FEATURES

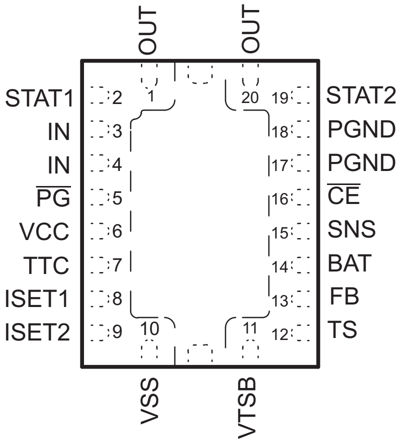
- **Qualified for Automotive Applications**
- **Ideal For Highly Efficient Charger Designs For Single-, Two-, or Three-Cell Li-Ion and Li-Polymer Battery Packs**
- **Also for LiFePO$_4$ Battery (see Using bq24105 to Charge LiFePO4 Battery)**
- **Integrated Synchronous Fixed-Frequency PWM Controller Operating at 1.1 MHz With 0% to 100% Duty Cycle**
- **Integrated Power FETs For Up To 2-A Charge Rate**
- **High-Accuracy Voltage and Current Regulation**
- **Stand-Alone (Built-In Charge Management and Control) Version**
- **Status Outputs For LED or Host Processor Interface Indicates Charge-In-Progress, Charge Completion, Fault, and AC-Adapter Present Conditions**
- **20-V Maximum Voltage Rating on IN and OUT Pins**
- **High-Side Battery Current Sensing**
- **Battery Temperature Monitoring**
- **Automatic Sleep Mode for Low Power Consumption**
- **Reverse Leakage Protection Prevents Battery Drainage**
- **Thermal Shutdown and Protection**
- **Built-In Battery Detection**
- **Available in 20-Pin, 3.5 mm × 4.5 mm, QFN Package**

DESCRIPTION

The bqSWITCHER™ series are highly integrated Li-ion and Li-polymer switch-mode charge management devices targeted at a wide range of portable applications. The bqSWITCHER™ series offers integrated synchronous PWM controller and power FETs, high-accuracy current and voltage regulation, charge preconditioning, charge status, and charge termination, in a small, thermally enhanced QFN package.

The bqSWITCHER charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on user-selectable minimum current level. A programmable charge timer provides a safety backup for charge termination. The bqSWITCHER automatically restarts the charge cycle if the battery voltage falls below an internal threshold. The bqSWITCHER automatically enters sleep mode when V_{CC} supply is removed.

RHL PACKAGE
(TOP VIEW)



ELECTRICAL CHARACTERISTICS (continued)

T_J = 0°C to 125°C and recommended supply voltage range (unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{(VCC)}$	V_{CC} supply current	$V_{CC} > V_{CC(min)}$, PWM switching		10		mA
		$V_{CC} > V_{CC(min)}$, PWM NOT switching			5	
		$V_{CC} > V_{CC(min)}$, $\overline{CE}$ = HIGH			315	A
	Battery discharge sleep current, (SNS,	0°C T_J 65°C, $V_{I(BAT)}$ = 4.2 V, $V_{CC} < V_{(SLP)}$ or $V_{CC} > V_{(SLP)}$ but not in charge			$C_{(SLP)}$ 65 [illegible]	
		0°C C $_{(SLP)}$ =				
		$V_{IREG} = \frac{1V}{RSET1} \times 1000,$				
		$V_{IREG-PRE} = \frac{0.1V}{RSET2} \times 1000,$				

[redacted]

[redacted]

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	**NO.**		
BAT	14	I	Battery voltage sense input. Bypass it with a 0.1 F capacitor to PGND if there are long *inductive* leads to battery.
$\overline{\text{CE}}$	16	I	Charger enable input. This active low input, if set high, suspends charge and places the device in the low-power sleep mode. Do not pull up this input to VTSB.
FB	13	I	Output voltage analog feedback adjustment. Connect the output of a resistive voltage divider powered from the battery terminals to this node to adjust the output battery voltage regulation.
IN	3, 4	I	Charger input voltage.
ISET1	8	I/O	Charger current set point 1 (fast charge). Use a resistor to ground to set this value.
ISET2	9	I/O	Charge current set point 2 (precharge and termination), set by a resistor connected to ground.
OUT	1, 20	O	Charge current output inductor connection. Connect a zener TVS diode between OUT pin and PGND pin to clamp the voltage spike to protect the power MOSFETs during abnormal conditions.
$\overline{\text{PG}}$	5	O	Power-good status output (open drain). The transistor turns on when a valid V_{CC} is detected. It is turned off in the sleep mode. $\overline{\text{PG}}$ can be used to drive a LED or communicate with a host processor.
PGND	17,18		Power ground input
SNS	15	I	Charge current-sense input. Battery current is sensed via the voltage drop developed on this pin by an external sense resistor in series with the battery pack. A 0.1- F capacitor to PGND is required.
STAT1	2	O	Charge status 1 (open-drain output). When the transistor turns on indicates charge in process. When it is off and with the condition of STAT2 indicates various charger conditions (see Table 1).
STAT2	19	O	Charge status 2 (open-drain output). When the transistor turns on indicates charge is done. When it is off and with the condition of STAT1 indicates various charger conditions (see Table 1).
TS	12	I	Temperature sense input. This input monitors its voltage against an internal threshold to determine if charging is allowed. Use an NTC thermistor and a voltage divider powered from VTSB to develop this voltage (see Figure 6).
TTC	7	I	Timer and termination control. Connect a capacitor from this node to GND to set the bqSWITCHER timer. When this input is low, the timer and termination detection are disabled.
VCC	6	I	Analog device input. A 0.1- F capacitor to VSS is required.
VSS	10		Analog ground input
VTSB	11	O	TS internal bias regulator voltage. Connect capacitor (with a value between a 0.1- F and 1- F) between this output and VSS.
Exposed Thermal Pad	Pad		There is an internal electrical connection between the exposed thermal pad and VSS. The exposed thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. The power pad can be used as a *star* ground connection between V_{SS} and PGND. A common ground plane may be used. VSS pin must be connected to ground at all times.

TYPICAL APPLICATION CIRCUIT

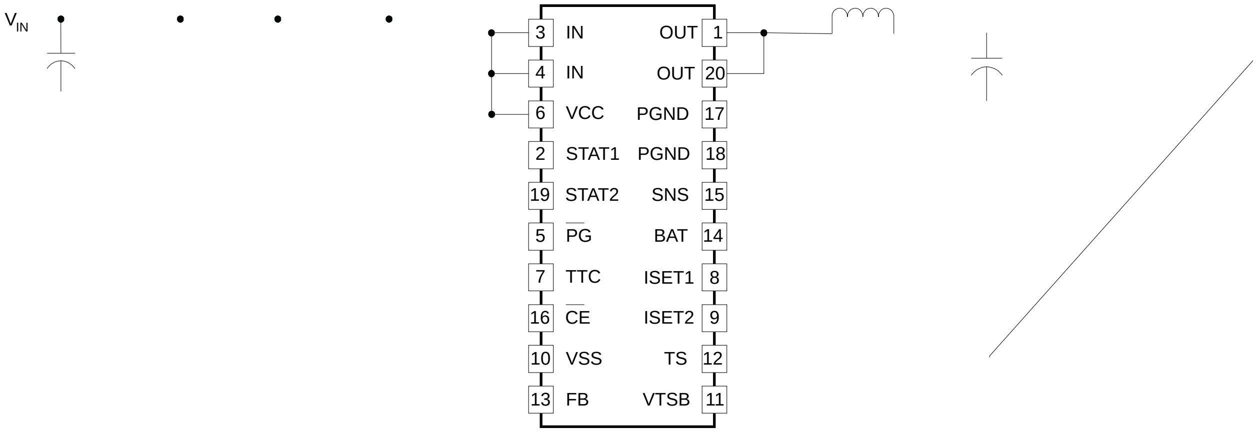


Figure 1. Stand-Alone 2-Cell Application

TYPICAL OPERATING PERFORMANCE

EFFICIENCY
vs
CHARGE CURRENT

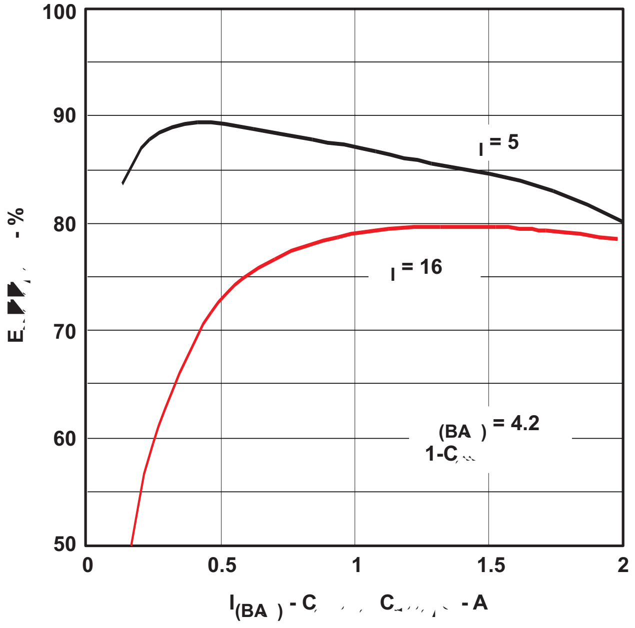


Figure 2.

EFFICIENCY
vs
CHARGE CURRENT

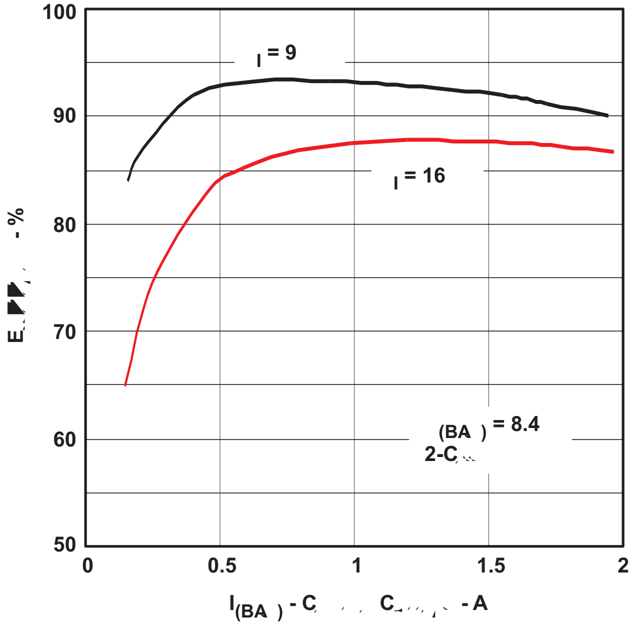
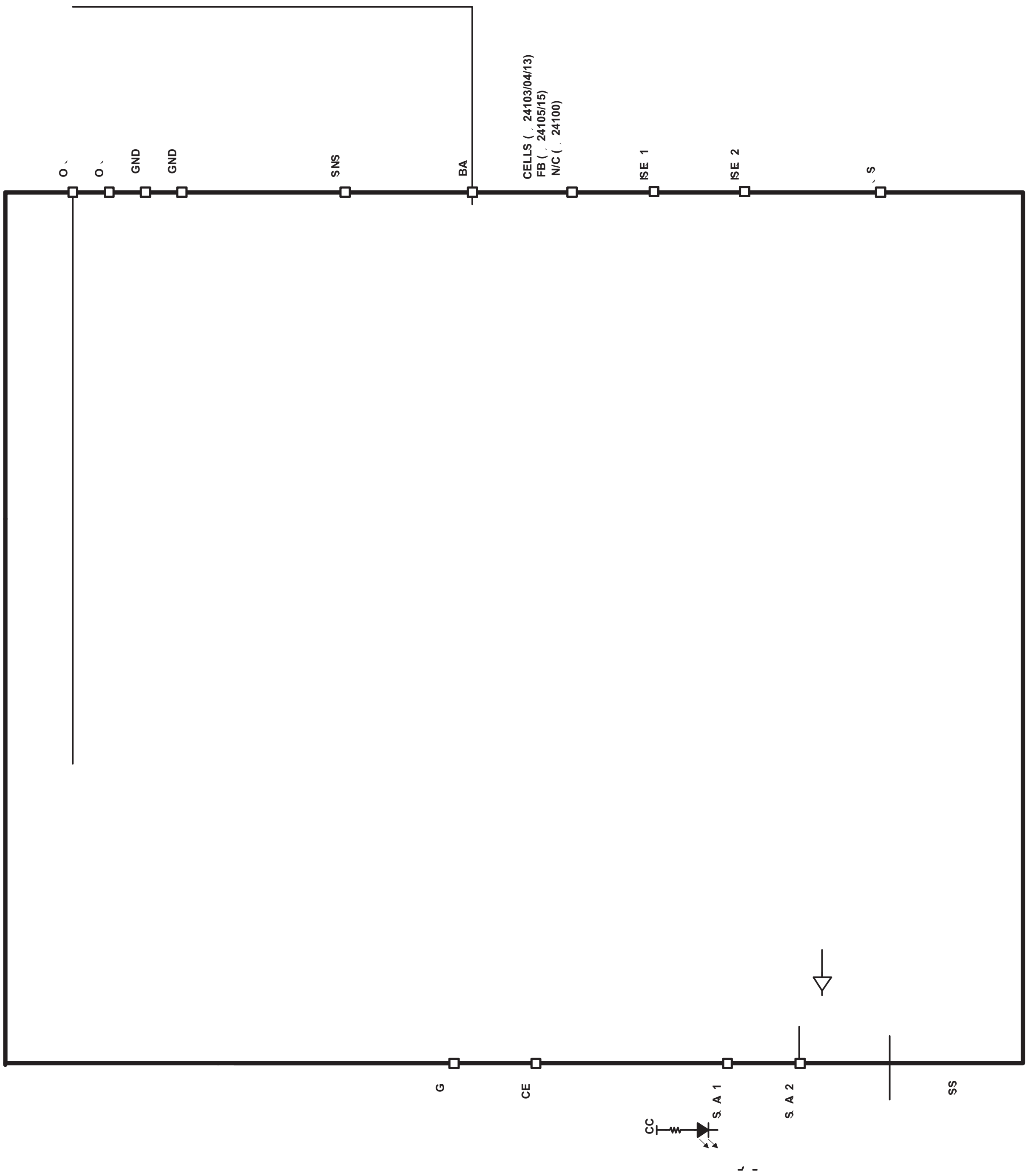
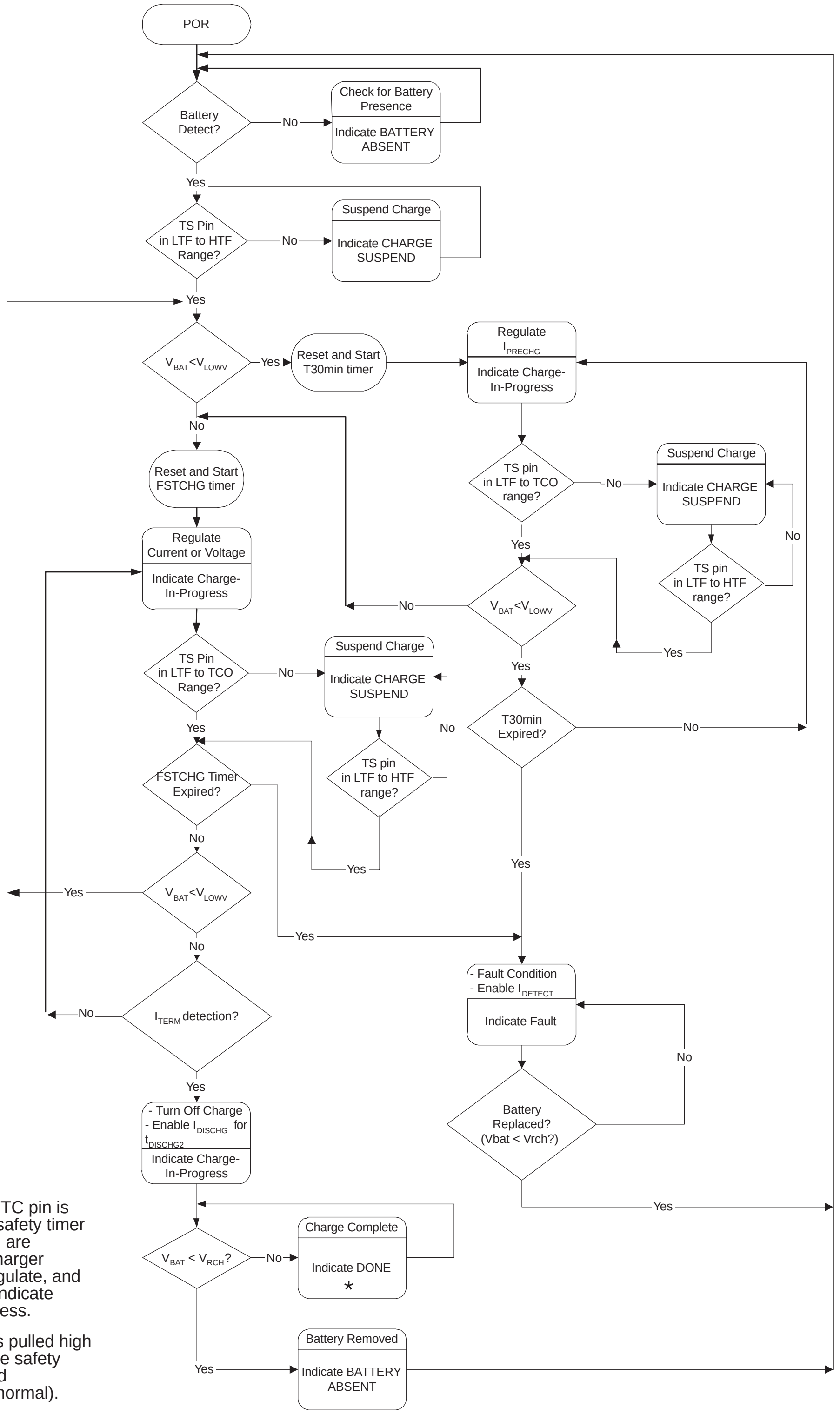


Figure 3.

FUNCTIONAL BLOCK DIAGRAM



OPERATIONAL FLOW CHART



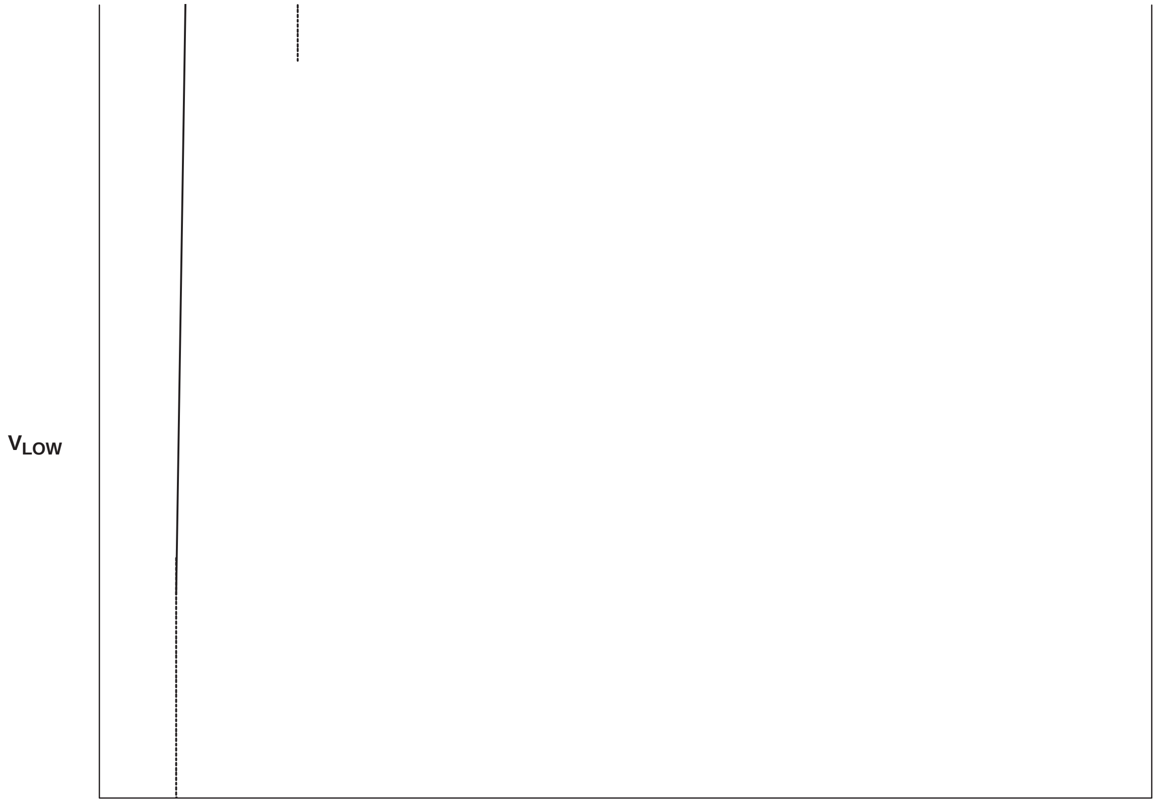
*NOTE: If the TTC pin is pulled low, the safety timer and termination are disabled; the charger continues to regulate, and the STAT pins indicate charge in progress.

If the TTC pin is pulled high (VTSB), only the safety timer is disabled (termination is normal).

Figure 4. Stand-Alone Version Operational Flow Chart

DETAILED DESCRIPTION

The bqSWITCHER™ supports a precision Li-ion or Li-polymer charging system for one-, two-, or three-cell applications. See Figure 4 for a typical charge profile.



UDG-04037

Figure 5. Typical Charging Profile

PWM Controller

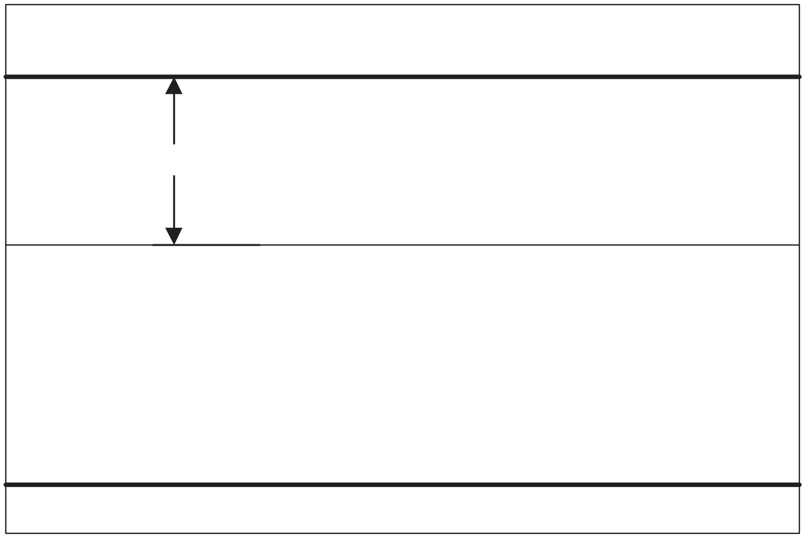
The bq24105 provides an integrated fixed 1MHz frequency voltage-mode controller with Feed-Forward function to regulate charge current or voltage. This type of controller is used to help improve line transient response, thereby simplifying the compensation network used for both continuous and discontinuous current conduction operation. The voltage and current loops are internally compensated using a Type-III compensation scheme that provides enough phase boost for stable operation, allowing the use of small ceramic capacitors with very low ESR. There is a 0.5-V offset on the bottom of the PWM ramp to allow the device to operate between 0% to 100% duty cycle.

The internal PWM gate drive can directly control the internal PMOS and NMOS power MOSFETs. The high-side gate voltage swings from V_{CC} (when off), to V_{CC} – 6 (when on and V_{CC} is greater than 6 V) to help reduce the conduction losses of the converter by enhancing the gate an extra volt beyond the standard 5V. The low-side gate voltage swings from 6 V, to turn on the NMOS, down to PGND to turn it off. The bq24105 has two back to back common-drain P-MOSFETs on the high side. An input P-MOSFET prevents battery discharge when IN is lower than BAT. The second P-MOSFET behaves as the switching control FET, eliminating the need of a bootstrap capacitor.

Cycle-by-cycle current limit is sensed through the internal high-side sense FET. The threshold is set to a nominal 3.6A peak current. The low-side FET also has a current limit that decides if the PWM Controller will operate in synchronous or non-synchronous mode. This threshold is set to 100mA and it turns off the low-side NMOS before the current reverses, prevent 0 Tset(the4id (4 0. 10 Tf 1000r7b0yTd (the)Tj0r7 0 Td5lh(sense)Tj23.4 0 Td4(current)e)Tj

Temperature Qualification

The bqSWITCHER continuously monitors battery temperature by measuring the voltage between the TS pin and VSS pin. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develop this voltage. The bqSWITCHER compares this voltage against its internal thresholds to determine if charging is allowed. To initiate a charge cycle, the battery temperature must be within the $V_{(LTF)}$-to-$V_{(HTF)}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER suspends charge and waits until the battery temperature is within the $V_{(LTF)}$-to-$V_{(HTF)}$ range. During the charge cycle (both precharge and fast charge), the battery temperature must be within the $V_{(LTF)}$-to-$V_{(TCO)}$ thresholds. If battery temperature is outside of this range, the bqSWITCHER battery



The magnitude of the precharge current, $I_{O(PRECHG)}$, is determined by the value of programming resistor, $R_{(ISET2)}$, connected to the ISET2 pin.

$$I_{O(PRECHG)} \quad \frac{K_{(ISET2)} \quad V_{(ISET2)}}{R_{(ISET2)} \quad R_{(SNS)}} \tag{2}$$

where

R_{SNS} is the external current-sense resistor
$V_{(ISET2)}$ is the output voltage of the ISET2 pin
$K_{(ISET2)}$ is the V/A gain factor
$V_{(ISET2)}$ and $K_{(ISET2)}$ are specified in the Electrical Characteristics table.

Battery Charge Current

The battery charge current, $I_{O(CHARGE)}$, is established by setting the external sense resistor, $R_{(SNS)}$, and the resistor, $R_{(ISET1)}$, connected to the ISET1 pin.

In order to set the current, first choose $R_{(SNS)}$ based on the regulation threshold V_{IREG} across this resistor. The best accuracy is achieved when the V_{IREG} is between 100 mV and 200 mV.

$$R_{(SNS)} = \frac{V_{IREG}}{I_{OCHARGE}} \tag{3}$$

If the results is not a standard sense resistor value, choose the next larger value. Using the selected standard value, solve for V_{IREG}. Once the sense resistor is selected, the ISET1 resistor can be calculated using the following equation:

$$R_{ISET1} = \frac{K_{ISET1} \times V_{ISET1}}{R_{SNS} \times I_{CHARGE}} \tag{4}$$

Battery Voltage Regulation

The voltage regulation feedback occurs through the BAT pin. This input is tied directly to the positive side of the battery pack. The bqSWITCHER monitors the battery-pack voltage between the BAT and VSS pins.

Output regulation voltage is specified as:

$$\Gamma = \frac{(\ 1+\ 2)}{2}\ T_{BA} \tag{5}$$

where R1 and R2 are resistor divider from BAT to FB and FB to VSS, respectively.

Recharge threshold voltage is specified as:

$$\Gamma = \frac{(\ 1+\ 2)}{2\ \ 50\ T} \tag{6}$$

Charge Termination and Recharge

The bqSWITCHER monitors the charging current during the voltage regulation phase. Once the termination threshold, I_{TERM}, is detected, the bqSWITCHER terminates charge. The termination current level is selected by the value of programming resistor, $R_{(ISET2)}$, connected to the ISET2 pin.

$$I_{TERM} \quad \genfrac{}{}{0pt}{}{K_{(ISET2)}}{R_{(ISET2)}} \quad \genfrac{}{}{0pt}{}{V_{TERM}}{R_{(SNS)}} \tag{7}$$

where

$R_{(SNS)}$ is the external current-sense resistor
V_{TERM} is the output of the ISET2 pin
$K_{(ISET2)}$ is the A/V gain factor
V_{TERM} and $K_{(ISET2)}$ are specified in the Electrical Characteristics table

As a safety backup, the bqSWITCHER also provides a programmable charge timer. The charge time is programmed by the value of a capacitor connected between the TTC pin and GND by the following formula:

$$t_{CHARGE} = C_{(TTC)} \times K_{(TTC)} \tag{8}$$

where

$C_{(TTC)}$ is the capacitor connected to the TTC pin
$K_{(TTC)}$ is the multiplier

A new charge cycle is initiated when one of the following conditions is detected:

- The battery voltage falls below the V_{RCH} threshold.
- Power-on reset (POR), if battery voltage is below the V_{RCH} threshold
- $\overline{CE}$ toggle
- TTC pin, described as follows.

In order to disable the charge termination and safety timer, the user can pull the TTC input below the V_{TTC_EN} threshold. Going above this threshold enables the termination and safety timer features and also resets the timer. Tying TTC high disables the safety timer only.

Sleep Mode

The bqSWITCHER enters the low-power sleep mode if the VCC pin is removed from the circuit. This feature prevents draining the battery during the absence of VCC.

Charge Status Outputs

The open-drain STAT1 and STAT2 outputs indicate various charger operations as shown in Table 1. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates that the open-drain transistor is turned off.

Table 1. Status Pins Summary

Charge State	STAT1	STAT2
Charge-in-progress	ON	OFF
Charge complete	OFF	ON
Charge suspend, timer fault, overvoltage, sleep mode, battery absent	OFF	OFF

Table 2. Status Pins Summary

Charge State	STAT1	STAT2
Battery absent	OFF	OFF
Charge-in-progress	ON	OFF
Charge complete	OFF	ON
Battery over discharge, $V_{I(BAT)} < V_{(SC)}$	ON/OFF (0.5 Hz)	OFF
Charge suspend (due to TS pin and internal thermal protection)	ON/OFF (0.5 Hz)	OFF
Precharge timer fault	ON/OFF (0.5 Hz)	OFF
Fast charge timer fault	ON/OFF (0.5 Hz)	OFF
Sleep mode	OFF	OFF

$\overline{\text{PG}}$ Output

The open-drain $\overline{\text{PG}}$ (power good) indicates when the AC-to-DC adapter (i.e., V_{CC}) is present. The output turns on when sleep-mode exit threshold, $V_{SLP\text{-}EXIT}$, is detected. This output is turned off in the sleep mode. The $\overline{\text{PG}}$ pin can be used to drive an LED or communicate to the host processor.

$\overline{\text{CE}}$ Input (Charge Enable)

The $\overline{\text{CE}}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level V_{CC} signal disables the charge. A high-to-low transition on this pin also resets all timers and fault conditions. Note that the $\overline{\text{CE}}$ pin cannot be pulled up to VTSB voltage. This may create power-up issues.

Timer Fault Recovery

As shown in Figure 6, bqSWITCHER provides a recovery method to deal with timer fault

$$f_0 = \frac{1}{2\pi \times \sqrt{L_{OUT} \times C_{OUT}}}$$

Battery Detection

For applications with removable battery packs, bqSWITCHER provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

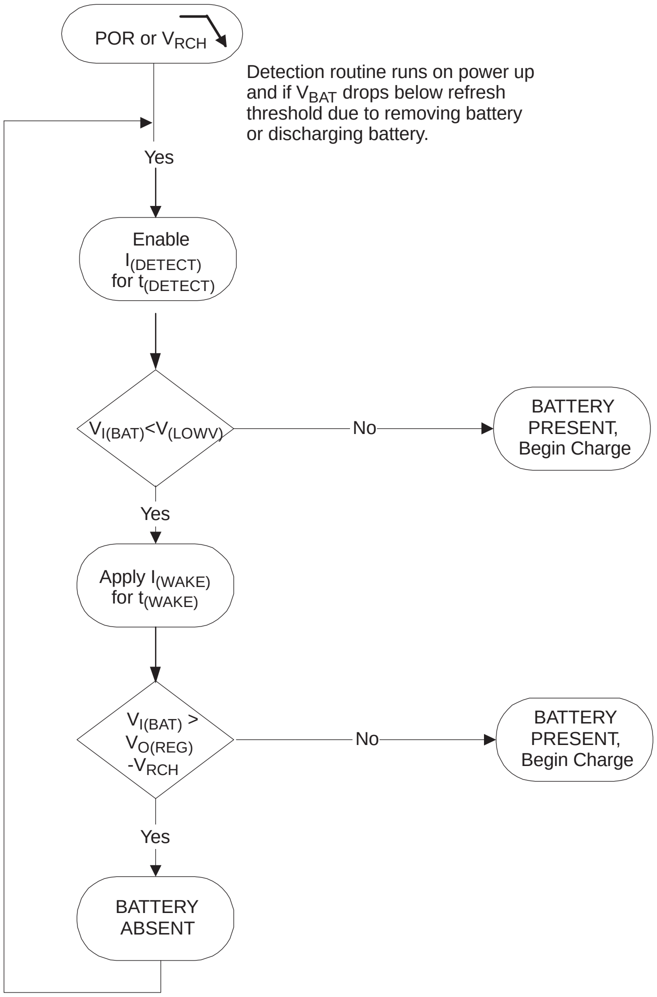


Figure 7. Battery Absent Detection

The voltage at the BAT pin is held above the battery recharge threshold, $V_{OREG} – V_{RCH}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqSWITCHER begins a battery absent detection test. This test involves enabling a detection current, $I_{DISCHARGE1}$, for a period of $t_{DISCHARGE1}$ and checking to see if the battery voltage is below the short circuit threshold, V_{SHORT}. Following this, the wake current, I_{WAKE} is applied for a period of t_{WAKE} and the battery voltage is checked again to ensure that it is above the recharge threshold. The purpose of this current is to attempt to *close* an open battery pack protector, if one is connected to the bqSWITCHER.

Passing both of the discharge and charge tests indicates a battery absent fault at the STAT pins. Failure of either test starts a new charge cycle. For the absent battery condition, typically the voltage on the BAT pin rises aiddeewthresh (a

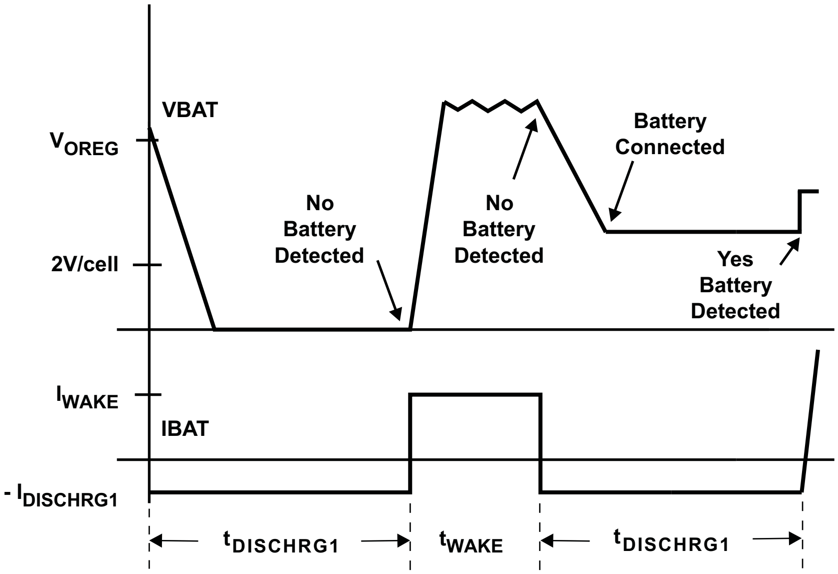


Figure 8. Battery Detect Timing Diagram

Battery Detection Example

In order to detect a *no battery* condition during the discharge and wake tests, the maximum output capacitance should not exceed the following:

a. Discharge ($I_{DISCHRG1}$ = 400 A, $t_{DISCHRG1}$ = 1s, V_{SHORT} = 2V)

$$C_{MAX\_DIS} = \frac{I_{DISCHRG1} \times t_{DISCHRG1}}{V_{OREG} - V_{SHORT}}$$

$$C_{MAX\_DIS} = \frac{400\ \mu A \times 1s}{4.2\ V - 2\ V}$$

$$C_{MAX\_DIS} = 182\ \mu F \tag{10}$$

b. Wake (I_{WAKE} = 2 mA, t_{WAKE} = 0.5 s, $V_{OREG} - V_{RCH}$ = 4.1V)

$$C_{MAX\_WAKE} = \frac{I_{WAKE} \times t_{WAKE}}{\left(V_{OREG} - V_{RCH}\right) - 0\ V}$$

$$C_{MAX\_WAKE} = \frac{2\ mA \times 0.5s}{(4.2\ V - 0.1\ V) - 0V}$$

$$C_{MAX\_WAKE} = 244\ \mu F \tag{11}$$

Based on these calculations the recommended maximum output capacitance to ensure proper operation of the battery detection scheme is 100 F which will allow for process and temperature variations.

Figure 9 shows the battery detection scheme when a battery is inserted. Channel 3 is the output signal and Channel 4 is the output current. The output signal switches between V_{OREG} and GND until a battery is inserted. Once the battery is detected, the output current increases from 0A to 1.3A, which is the programmed charge current for this application.

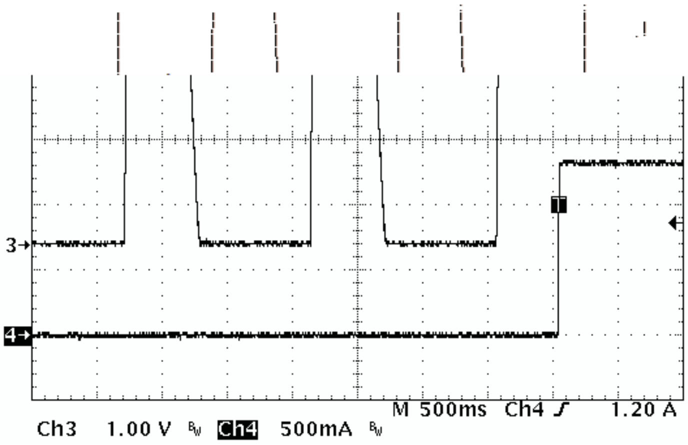


Figure 9. Battery Detection Waveform When a Battery is Inserted

Figure 10 shows the battery detection scheme when a battery is removed. Channel 3 is the output signal and Channel 4 is the output current. When the battery is removed, the output signal goes up due to the stored energy in the inductor and it crosses the $V_{OREG} – V_{RCH}$ threshold. At this point the output current goes to 0A and the IC terminates the charge process and turns on the $I_{DISCHG2}$ for $t_{DISCHG2}$. This causes the output voltage to fall down below the $V_{OREG} – V_{RCHG}$ threshold triggering a *Battery Absent* condition and starting the battery detection scheme.

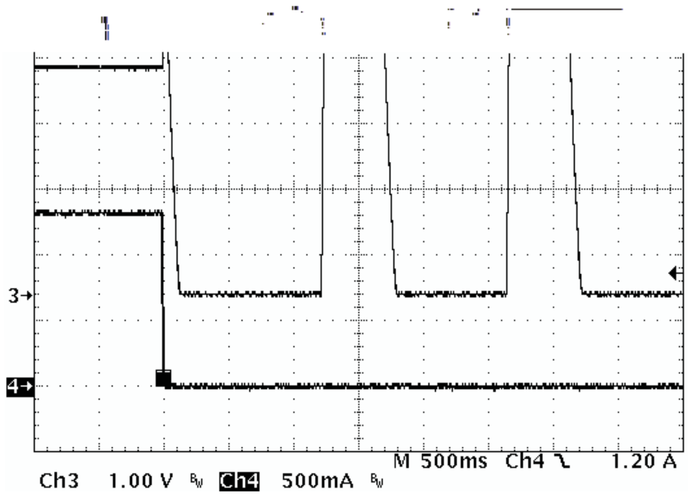


Figure 10. Battery Detection Waveform When a Battery is Removed

Current Sense Amplifier

A current sense amplifier feature that translates the charge current into a DC voltage is offered. Figure 11 is a block diagram of this feature.

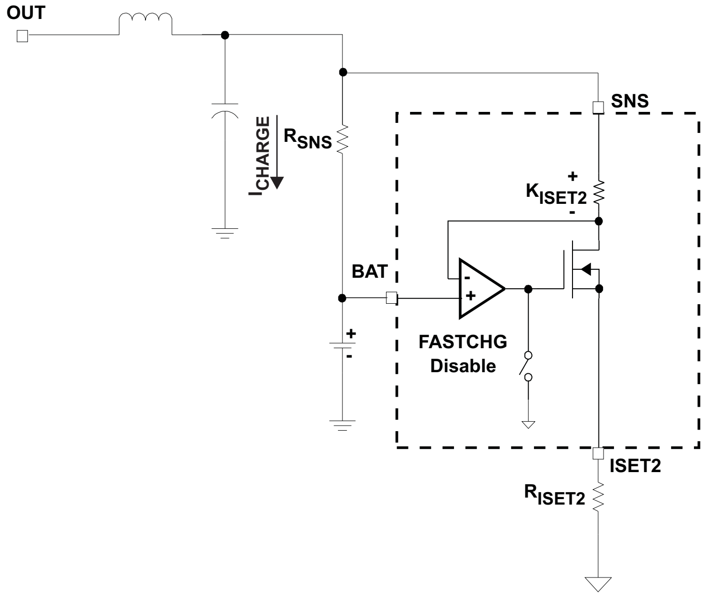


Figure 11. Current Sense Amplifier

The voltage on the ISET2 pin can be used to calculate the charge current. Equation 12 shows the relationship between the ISET2 voltage and the charge current:

$$I_{CHARGE} = \frac{V_{ISET2} \times K_{(ISET2)}}{R_{SNS} \times R_{ISET2}} \tag{12}$$

This feature can be used to monitor the charge current (Figure 12) during the current regulation phase (Fastcharge only) and the voltage regulation phase. The schematic for the application circuit for this waveform is shown in Figure 14

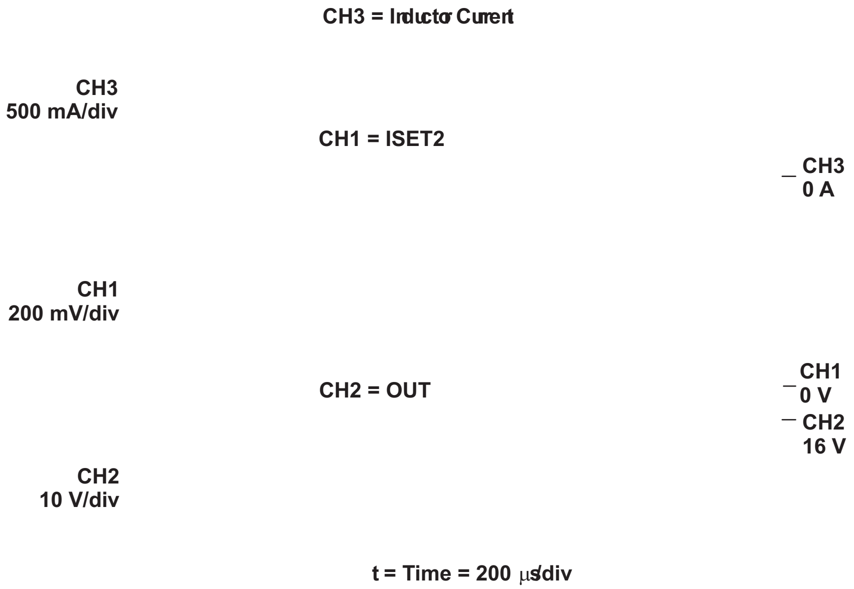


Figure 12. Current Sense Amplifier Charge Current Waveform

bqSWITCHER SYSTEM DESIGN EXAMPLE

The following section provides a detailed system design example for the bq24100.

System Design Specifications:

- V_{IN} = 16V
- V_{BAT} = 4.2V (1-Cell)
- I_{CHARGE} = 1.33 A
- $I_{PRECHARGE}$ = I_{TERM} = 133 mA
- Safety Timer = 5 hours
- Inductor Ripple Current = 30% of Fast Charge Current
- Initiate Charge Temperature = 0°C to 45°C

1. Determine the inductor value (L_{OUT}) for the specified charge current ripple:

$$\Delta I_L = I_{CHARGE} \times I_{CHARGE}\text{Ripple}$$

$$L_{OUT} = \frac{V_{BAT} \times \left(V_{INMAX} - V_{BAT}\right)}{V_{INMAX} \times f \times \Delta I_L}$$

$$L_{OUT} = \frac{4.2 \times (16 - 4.2)}{16 \times (1.1 \times 10^6) \times (1.33 \times 0.3)}$$

$$L_{OUT} = 7.06\ \mu\text{H} \tag{13}$$

Set the output inductor to standard 10 H. Calculate the total ripple current with using the 10 H inductor:

$$\Delta I_L = \frac{V_{BAT} \times \left(V_{INMAX} - V_{BAT}\right)}{V_{INMAX} \times f \times L_{OUT}}$$

$$\Delta I_L = \frac{4.2 \times (16 - 4.2)}{16 \times (1.1 \times 10^6) \times (10 \times 10^{-6})}$$

$$\Delta I_L = 0.282\ \text{A} \tag{14}$$

Calculate the maximum output current (peak current):

$$I_{LPK} = I_{OUT} + \frac{\Delta I_L}{2}$$

$$I_{LPK} = 1.33 + \frac{0.282}{2}$$

$$I_{LPK} = 1.471\ \text{A} \tag{15}$$

Use standard 10 H inductor with a saturation current higher than 1.471A. (i.e., Sumida CDRH74-100)

2. Determine the output capacitor value ($_{OUT}$) using 16 kHz as the resonant frequency:

$$f_0 = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times f_0{}^2 \times L_{OUT}}$$

$$C_{OUT} = \frac{1}{4\pi^2 \times (16 \times 10^3)^2 \times (10 \times 10^{-6})}$$

$$C_{OUT} = 9.89\ \mu F \tag{16}$$

Use standard value 10 F, 25V, X5R, ±20% ceramic capacitor (i.e., Panasonic 1206 ECJ-3YB1E106M

3. Determine the sense resistor using the following equation:

$$R_{SNS} = \frac{V_{RSNS}}{I_{CHARGE}} \tag{17}$$

In order to get better current regulation accuracy (±10%), let V_{RSNS} be between 100 mV and 200 mV. Use V_{RSNS} = 100 mV and calculate the value for the sense resistor.

$$R_{SNS} = \frac{100\ mV}{1.33\ A}$$

$$R_{SNS} = 0.075 \tag{18}$$

This value is not standard in resistors. If this happens, then choose the next larger value which in this case is 0.1 . Using the same equation (15) the actual V_{RSNS} will be 133mV. Calculate the power dissipation on the sense resistor:

$$P_{RSNS} = I_{CHARGE}{}^2 \times R_{SNS}$$

$$P_{RSNS} = 1.33^2 \times 0.1$$

$$P_{RSNS} = 176.9\ mW \tag{19}$$

Select standard value 100 m , 0.25W 0805, 1206 or 2010 size, high precision sensing resistor. (i.e., Vishay CRCW1210-0R10F)

4. Determine ISET 1 resistor using the following equation:

$$R_{ISET1} = \frac{K_{ISET1} \times V_{ISET1}}{R_{SNS} \times I_{CHARGE}}$$

$$R_{ISET1} = \frac{1000 \times 1.0}{0.1 \times 1.33}$$

$$R_{ISET1} = \tag{20}$$

Select standard value 7.5 k , 1/16W ±1% resistor (i.e., Vishay CRCWD0603-7501-F)

5. Determine ISET 2 resistor using the following equation:

$$R_{ISET2} = \frac{K_{ISET2} \times V_{ISET2}}{R_{SNS} \times I_{PRECHARGE}}$$

$$R_{ISET2} = \frac{1000 \times 0.1}{0.1 \times 0.133}$$

$$R_{ISET2} = 7.5\ k \tag{21}$$

Select standard value 7.5 k , 1/16W ±1% resistor (i.e., Vishay CRCWD0603-7501-F)

6. Determine TTC capacitor ($_{TTC}$) for the 5.0 hours safety timer using the following equation:

$$C_{TTC} = \frac{t_{CHARGE}}{K_{TTC}}$$

$$C_{TTC} = \frac{300\ m}{2.6\ m/nF}$$

$$C_{TTC} = 115.4\ nF \qquad (22)$$

   Select standard value 100 nF, 16V, X7R, ±10% ceramic capacitor (i.e., Panasonic ECJ-1VB1C104K). Using this capacitor the actual safety timer will be 4.3 hours.

7. Determine TS resistor network for an operating temperature range from 0°C to 45°C.

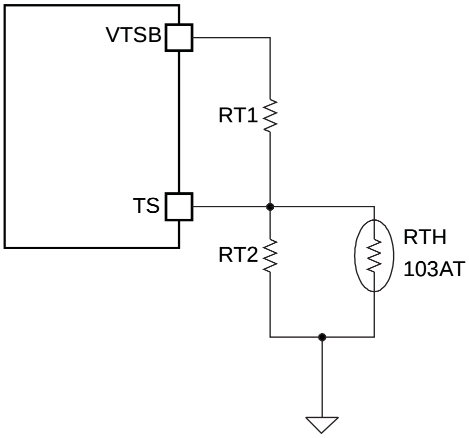


Figure 13. TS Resistor Network

   Assuming a 103AT NTC Thermistor on the battery pack, determine the values for RT1 and RT2 using the following equations:

(23)

$$RTH_{COLD} = 27.28\ k$$

$$RTH_{HOT} = 4.912\ k$$

$$RT1 = 9.31\ k$$

$$RT2 = 442\ k \qquad (24)$$

APPLICATION INFORMATION

Charging Battery and Powering System Without Affecting Battery Charge and Termination

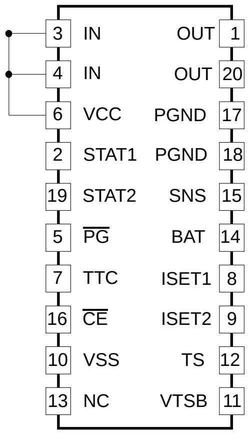


Figure 14. Application Circuit for Charging a Battery and Powering a System Without Affecting Termination

The bqSWITCHER was designed as a stand-alone battery charger but can be easily adapted to power a system load, while considering a few minor issues.

Advantages:

1. The charger controller is based only on what current goes through the current-sense resistor (so precharge, constant current, and termination all work well), and is not affected by the system load.
2. The input voltage has been converted to a usable system voltage with good efficiency from the input.
3. Extra external FETs are not needed to switch power source to the battery.
4. The TTC pin can be grounded to disable termination and keep the converter running and the battery fully charged, or let the switcher terminate when the battery is full and then run off of the battery via the sense resistor.

Other Issues:

1. If the system load current is large (1 A), the IR drop across the battery impedance causes the battery voltage to drop below the refresh threshold and start a new charge. The charger would then terminate due to low charge current. Therefore, the charger would cycle between charging and termination. If the load is smaller, the battery would have to discharge down to the refresh threshold resulting in a much slower cycling. Note that grounding the TTC pin keeps the converter on continuously.
2. If TTC is grounded, the battery is kept at 4.2 V (not much different than leaving a fully charged battery set unloaded).
3. Efficiency declines 2-3% hit when discharging through the sense resistor to the system.

Using bq24105 to Charge LiFePO$_4$ Battery

The LiFePO$_4$ battery has many unique features such as a high thermal runaway temperature, discharge current capability, and charge current. These special features make it attractive in many applications such as power tools. The recommended charge voltage is 3.6 V and termination current is 50 mA. Figure 15 shows an application circuit for charging one cell LiFePO4 using bq24105. The charge voltage is 3.6 V and recharge voltage is 3.516 V. The fast charging current is set to 1.33 A while the termination current is 50 mA. This circuit can be easily changed to support two or three cell applications. However, only 84 mV difference between regulation set point and rechargeable threshold makes it frequently enter into recharge mode when small load current is applied. This can be solved by lower down the recharge voltage threshold to 200 mV to discharge more energy from the battery before it enters recharge mode again. See the application report, *Using the bq24105/25 to Charge LiFePO$_4$ Battery* (SLUA443), for additional details. The recharge threshold should be selected according to real application conditions.

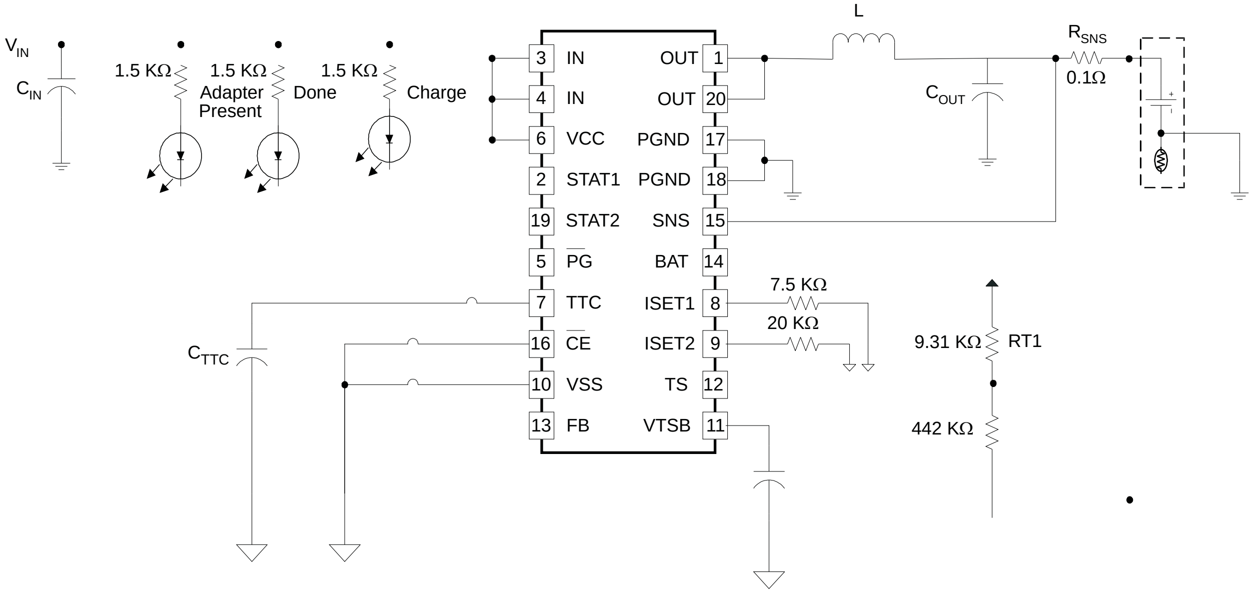


Figure 15. 1-Cell LiFePO4 Application

THERMAL CONSIDERATIONS

The SWITCHER is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the IC and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application report entitled: *QFN/SON PCB Attachment* (SLUA271).

The most common measure of package thermal performance is thermal impedance ($_{JA}$) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for $_{JA}$ is:

$$\theta_{(JA)} = \frac{T_J - T_A}{P} \tag{25}$$

Where:

T_J = chip junction temperature
T_A = ambient temperature
P = device power dissipation

Factors that can greatly influence the measurement and calculation of $_{JA}$ include:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

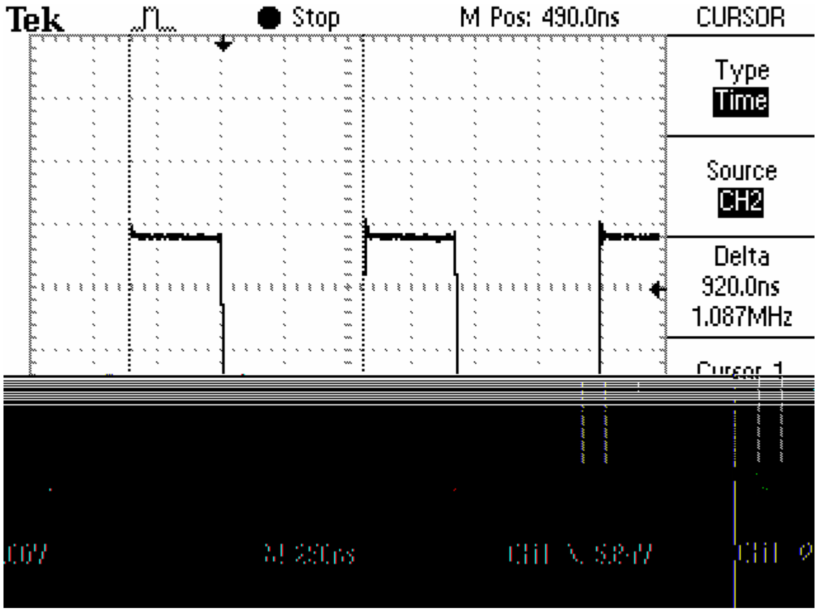
The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal power FET. It can be calculated from the following equation:

P = [Vin × Iin - Vbat × Ibat]

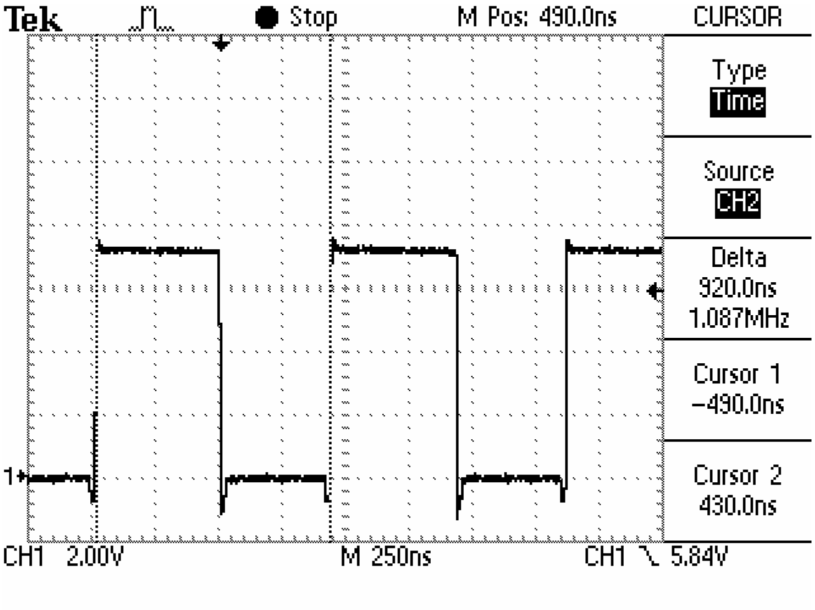
Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at its lowest. (See Figure 5.)

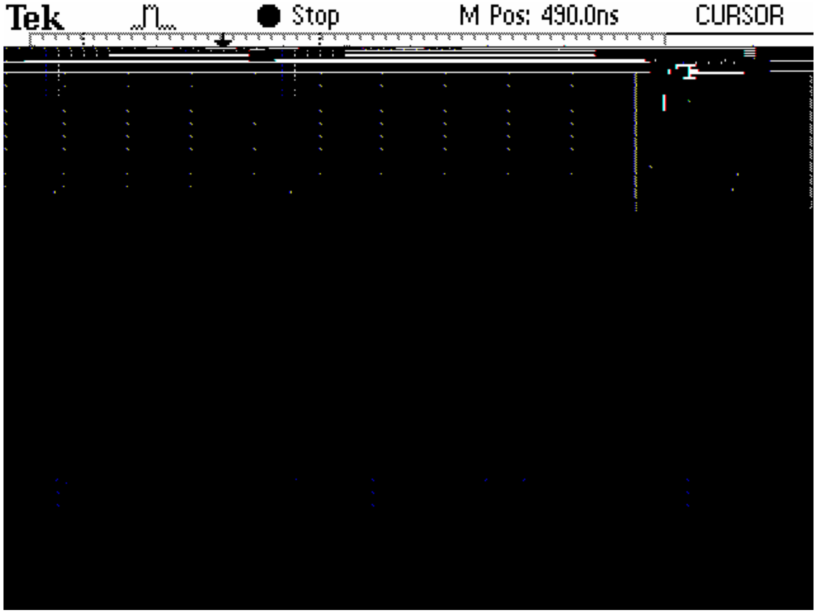
PCB LAYOUT CONSIDERATION

It is important to pay special attention to the PCB layout. The following



Precharge: The current is low in precharge; so, the bottom synchronous FET turns off after its minimum Precharge: Thesyn





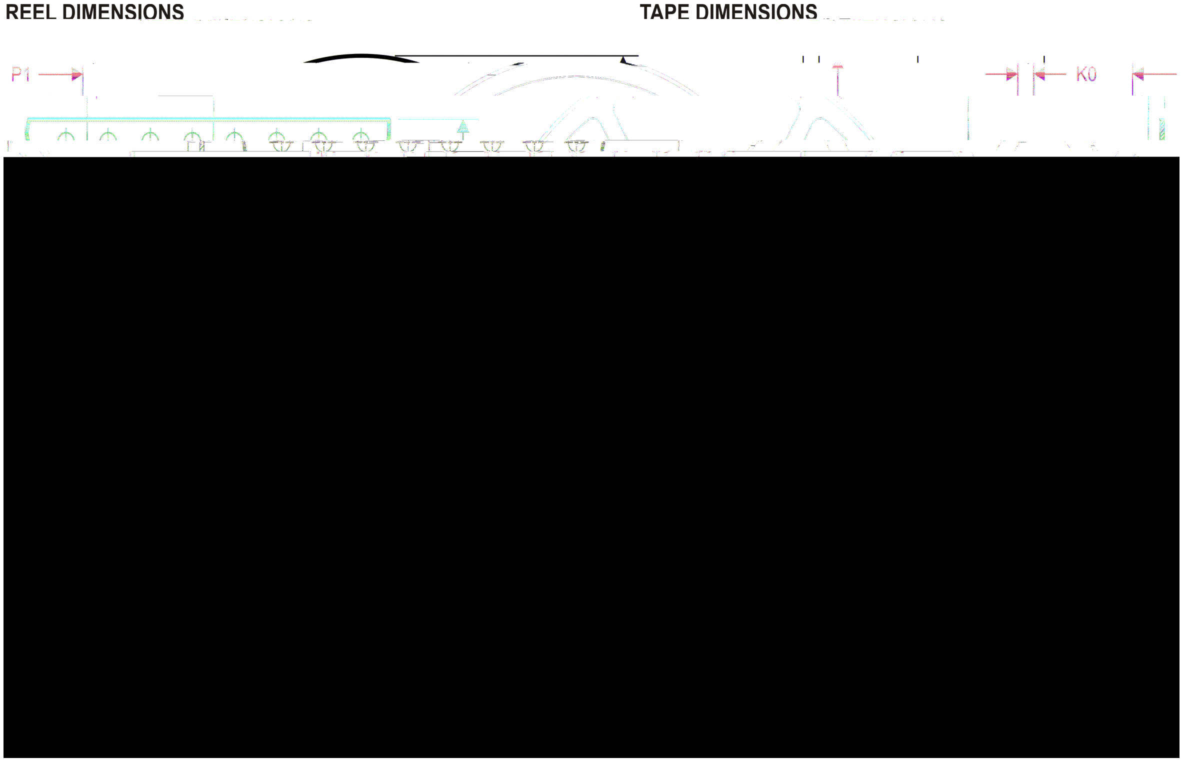
REVISION HISTORY

Changes from Original (August, 2009) to Revision A	Page
• Updated V_{OREG} formula to match the BQ24105 commercial datasheet.	13

PACKAGING INFORMATION

- Catalog - TI's standard catalog product

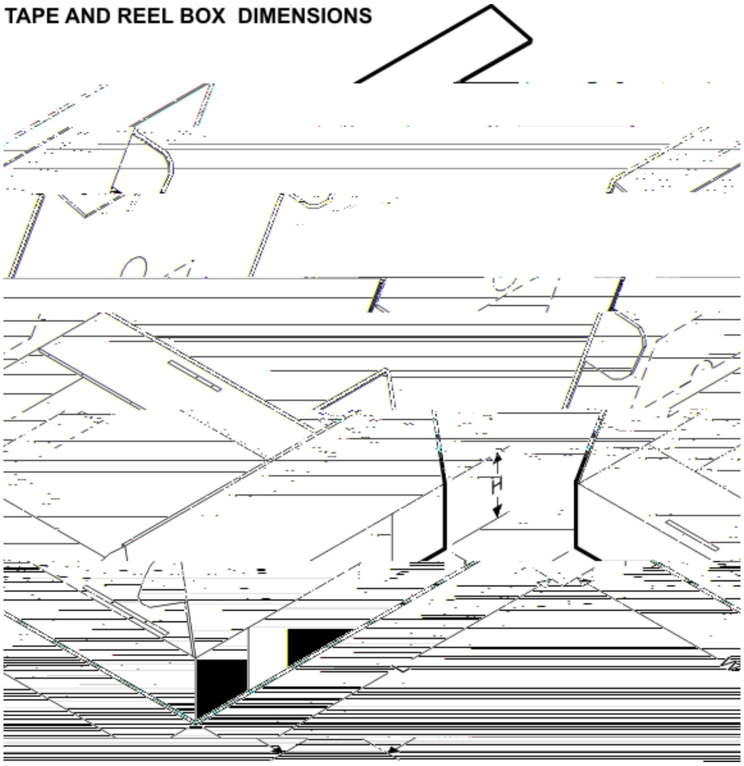
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24105IRHLRQ1	QFN	RHL	20	3000	330.0	12.4	3.8	4.8	1.6	8.0	12.0	Q1

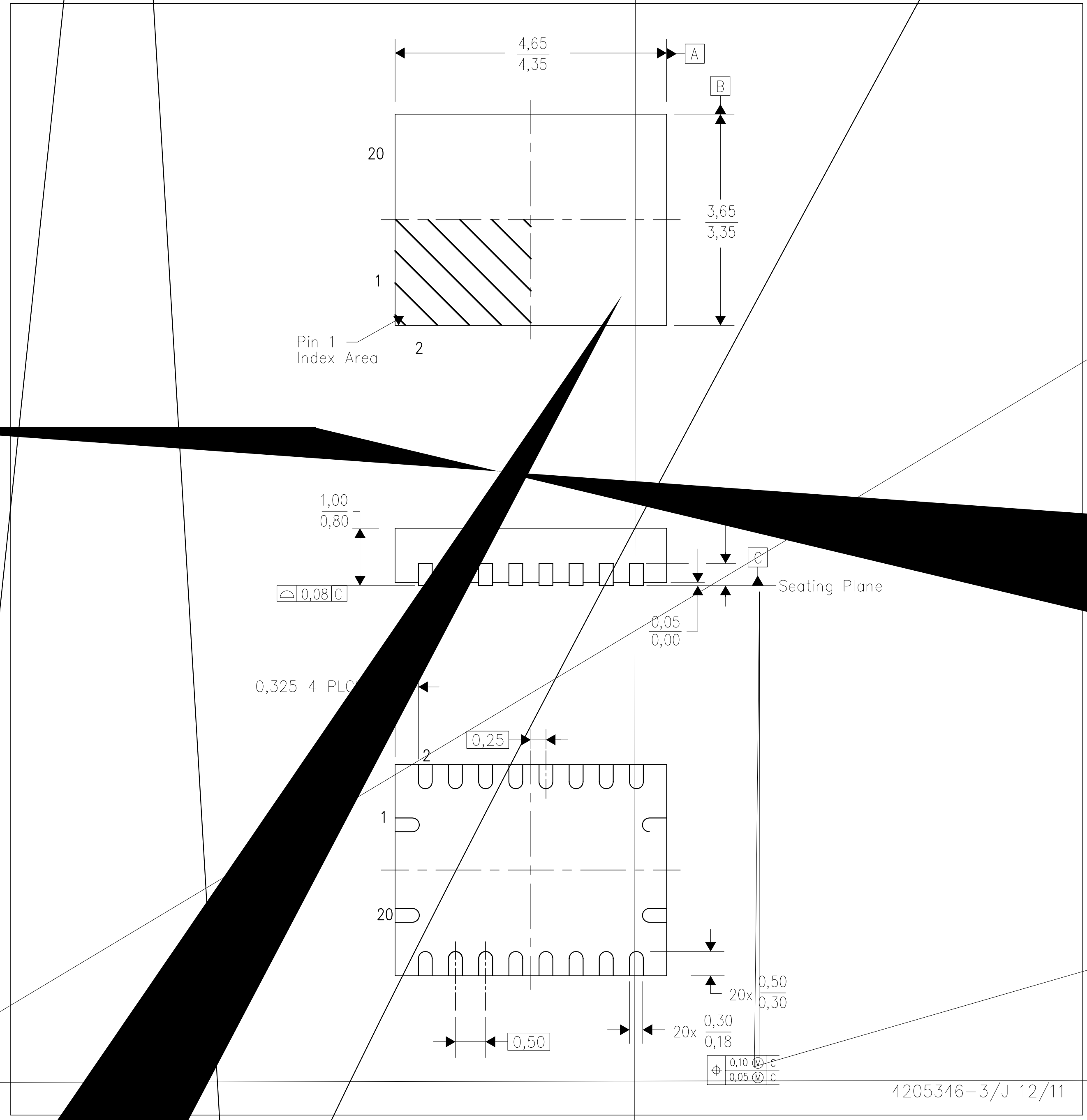
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24105IRHLRQ1	QFN	RHL	20	3000	367.0	367.0	35.0

RHL (R-PVQFN-N20) PLASTIC QUAD FLATPACK NO-LEAD



NOTES dimens and tolerancing per ASME Y14.5M-1994.

wing is subject to change without notice.

Quad Flatpack No-Lead) Package configuration.

package thermal pad must be soldered to the board for thermal and mechanical performance.

duct Data Sheet for details regarding the exposed thermal pad features and dimensions.

RHL (S-PVQFN-N20)

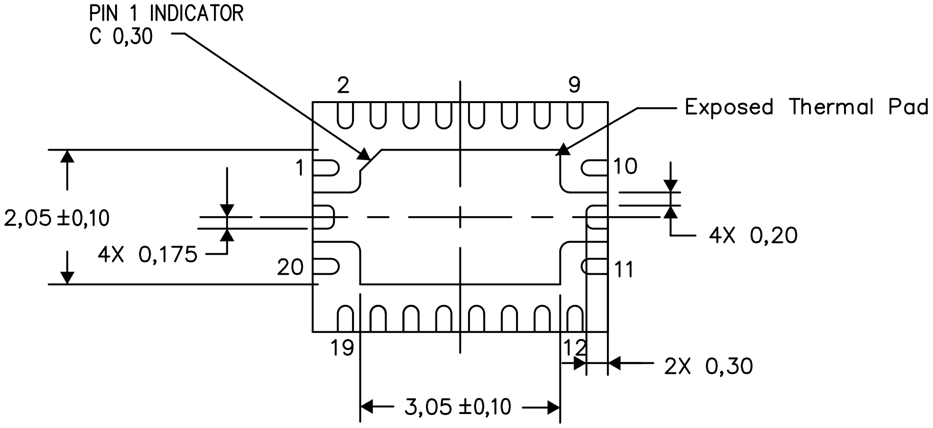
THERMAL INFORMATION

cttached directly to an external

integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



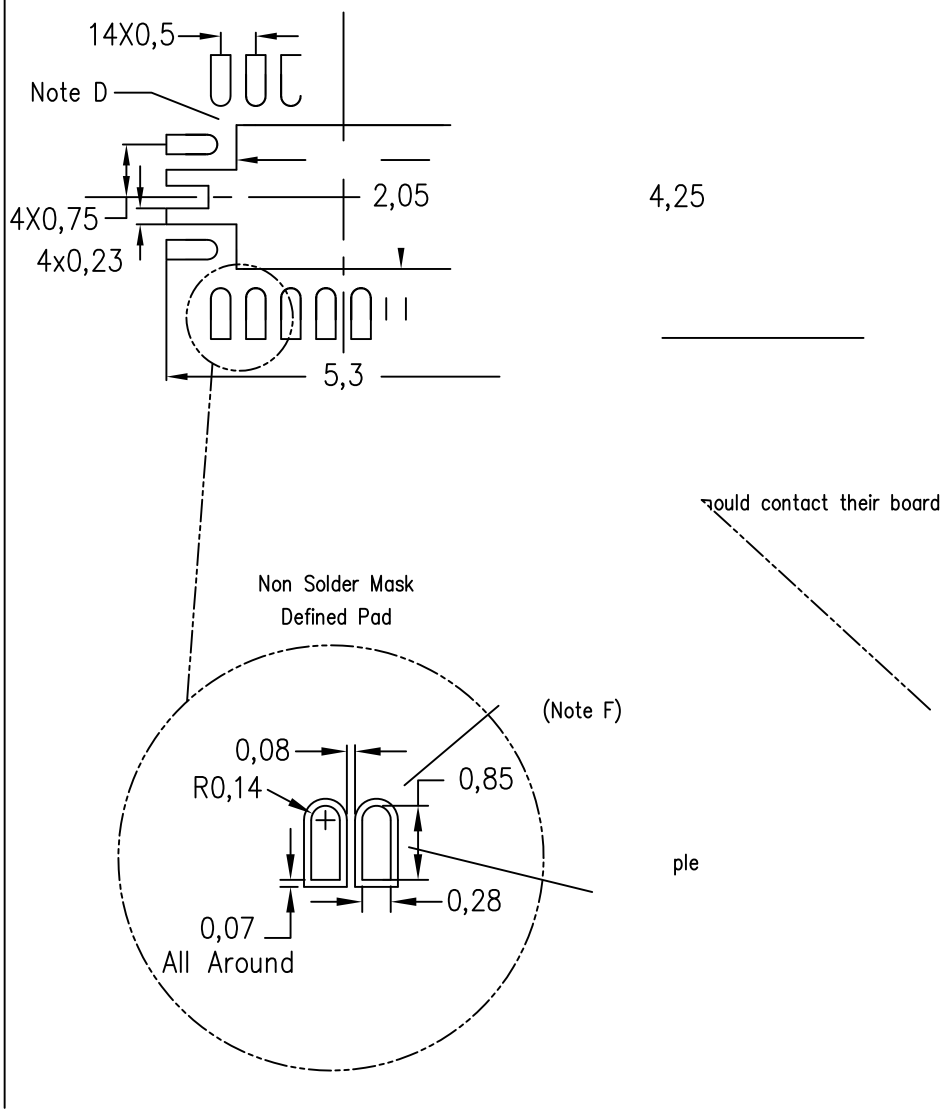
Bottom View

Exposed Thermal Pad Dimensions

4206363-3/M 08/12

kage incorporates an exposed thermal pad that is designed to be

RHL (R–PVQFN–N20)



ould contact their board fabrication site for minimum solder mask web tolerances b

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

E.

F.

IMPORTANT NOTICE

Texas Instruments