bq2014H

Low-Cost NiCd/NiMH Gas Gauge IC

Features

- Accurate measurement of available capacity in NiCd or NiMH batteries
- Low-cost battery management solution for pack integration
  - As little as ½ square inch of PCB for complete circuit
  - Low operating current (120µA typical)
  - Less than 100nA of data retention current
- High-speed (5kb/s) single-wire communication interface (HDQ bus) for critical battery parameters
- Communication with an external charge controller such as the bq2004
- Direct drive of remaining capacity LEDs
- Automatic rate and temperature compensation of measurements
- 16-pin narrow SOIC

General Description

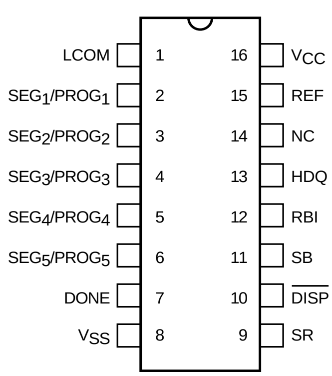
The bq2014H NiCd/NiMH Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of available battery capacity. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery. Compensations for battery temperature, self-discharge, and rate of discharge are applied to the charge counter to provide available capacity information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

Nominal available capacity may be directly indicated using a five-segment LED display. The bq2014H also supports a simple single-line bidirectional serial link to an external processor (common ground). The 5kb/s HDQ bus interface reduces communications overhead in the external microcontroller.

Internal registers include available capacity and energy, temperature, voltage and current, and battery status. The external processor may also overwrite some of the bq2014H gas gauge data registers.

The bq2014H can operate from the batteries in the pack. The REF output and an external transistor allow a simple, inexpensive voltage regulator to supply power to the circuit from the cells.

Pin Connections



16-Pin Narrow SOIC

PN20140H..eps

Pin Names

LCOM	LED common output	V_{SS}	System ground
$SEG_1/PROG_1$	LED segment 1/ program 1 input	SR	Sense resistor input
$SEG_2/PROG_2$	LED segment 2/ program 2 input	$\overline{DISP}$	Display control input
$SEG_3/PROG_3$	LED segment 3/ program 3 input	SB	Battery sense input
$SEG_4/PROG_4$	LED segment 4/ program 4 input	RBI	Register backup input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	HDQ	Serial communications input/output
DONE	Charge complete input	NC	No connect
		REF	Voltage reference output
		V_{CC}	Supply voltage

SLUS030A–JUNE 1999 - REVISED OCTOBER 2003

Pin Descriptions

Open-drain output that switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

1

Outputs that each may activate an LED to sink the current sourced from LCOM.

1

Three-level input pins that define the programmed full count (PFC) thresholds described in Table 2.

Three-level input pins that define the scale factor described in Table 2.

Three-level input pin that defines the self-discharge and battery-compensation factors as shown in Table 1.

Communicates the status of an external charge-controller such as the bq2004 Fast-Charge IC to the bq2014H. Note: This pin must be pulled down to V_{SS} using a 200kΩ resistor.

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2014H is $V_{SR} + V_{OS}$.

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during charge. $\overline{DISP}$ low activates the display. See Table 1.

Monitors the battery cell-voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds and for battery-removed detection.

Provides backup potential to the bq2014H registers while $V_{CC} \leq 3V$. A storage capacitor or a battery can be connected to RBI.

This is the open-drain bidirectional communications port.

REF provides a voltage reference output for an optional microregulator.

Functional Description

General Operation

The bq2014H determines battery capacity by monitoring the amount of current input to or removed from a rechargeable battery. The bq2014H measures discharge and charge currents, measures battery voltage, estimates self-discharge, monitors the battery for low battery-voltage thresholds, and compensates for temperature and charge/discharge rate. Current measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and

Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2014H monitors the battery potential through the SB pin for the end-of-discharge voltage (EDV) thresholds.

The EDV threshold levels are used to determine when the battery has reached an "empty" state.

The EDV thresholds for the bq2014H are programmable

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2014H. The bq2014H accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. The accumulated charge and discharge currents are adjusted for temperature and rate to provide the indication of compensated available capacity to the host system or user.

The main counter, Nominal Available Capacity (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2014H adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity equals the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. [illegible]

LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

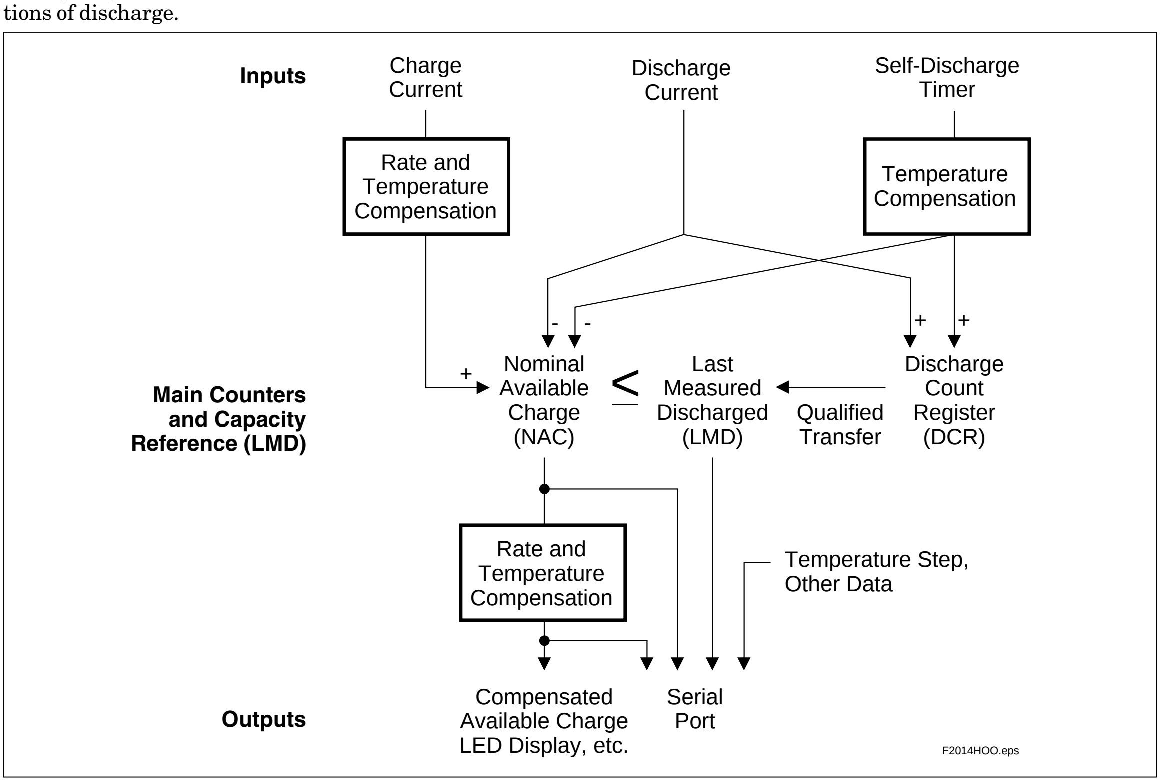


Figure 2. Operational Overview

[illegible]

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The bq2014H is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) ∗ sense resistor (Ω) =

PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference until the bq2014H "learns" a new capacity reference.

Example: Selecting a PFC Value

Given:

Sense resistor = 0.05Ω
Number of cells = 10
Capacity = 3500mAh, NiMH
Current range = 50mA to 1A
Relative display mode
Self-discharge = $^{NAC}/_{47}$ per day @ 25°C
Voltage drop over sense resistor = 2.5mV to 50mV
Nominal discharge voltage = 1.2V

Therefore:

3500mAh ∗ 0.05Ω = 175mVh

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z or H			
1	2		$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	$PROG_3$ = H	$PROG_3$ = Z	$PROG_3$ = L	Units
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh

Select:

PFC = 27648 counts or 173mVh
$PROG_1$ = low
$PROG_2$ = high
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = low

The initial full battery capacity is 173mVh (3460mAh) until the bq2014H "learns" a new capacity with a qualified discharge from full to EDV1.

- [illegible]

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV1. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD or 0.94 ∗ LMD if T < 0°C.

- [illegible]

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC ≥ 0.94 ∗ LMD and a discharge is detected. The DCR does not roll over but stops counting when it reaches FFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if all the following conditions are met:

- No valid charge initiations (charges greater than 2 NAC updates where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC ≥ 0.94 ∗ LMD and EDV1.
- The self-discharge is less than 6.25% of NAC.
- The temperature is ≥ 0°C when the EDV1 level is reached during discharge.
- The discharge begins when NAC ≥ 0.94 ∗ LMD.
- VDQ is set.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update. If the DCR update value is less than 0.94 ∗ LMD, LMD will only be modified by 0.94 ∗ LMD. This prevents invalid DCR values from corrupting LMD.

- [illegible]

SAE is useful in determining the available energy within the battery, and may provide a more useful capacity reference in battery chemistries with sloped voltage profiles during discharge. SAE may be converted to an mWh value using the following formula:

$$E(mWh) = (SAEH * 256 + SAEL) * \frac{1.2 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

where R_{B1}, R_{B2}, and R_S

Count Compensations

Charge Compensation

Two charge efficiency compensation factors are used for trickle and fast charge. Trickle charge is defined as a rate of charge < C/3. The compensation defaults to the fast-charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over two ranges between nominal and hot temperatures. The compensation factors are shown below.

Charge Temperature	Trickle-Charge Compensation	Fast-Charge Compensation
< 40°C	0.81	0.94
> 40°C	0.75	0.88

Compensated Available Capacity

NAC is adjusted for rate of discharge and temperature to derive the CACD and CACT values.

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the discharge rate. This com-

Table 6. bq2014H Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

Error Summary

Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated. (See the DCR description.) The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity.

A Capacity Inaccurate counter (CPI) is maintained and incremented each time a valid charge occurs (qualified by NAC; see the CPI register description). It is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

Current-Sensing Error

Table 6 shows the non-linearity and non-repeatability errors associated with the bq2014H current sensing.

Table 7 illustrates the current-sensing error as a function of V_{OS}. A digital filter prevents charge and discharge counts to the NAC register when V_{SRO} is between V_{SRQ} and V_{SRD}.

Table 7. V_{OS}-Related Current Sense Error (Current = 1A)

V_{OS} (µV)	Sense Resistor			
	20	50	100	mΩ
50	0.25	0.10	0.05	%
100	0.50	0.20	0.10	%
150	0.75	0.30	0.15	%
180	0.90	0.36	0.18	%

Done Input

A charge-control IC or a microcontroller uses the DONE input to communicate charge status to the bq2014H. When the DONE input is asserted high on charge completion, the bq2014H sets NAC = LMD and VDQ = 1. The DONE input should be maintained high as long as the charge controller or microcontroller keeps the batteries full; otherwise, the pin should be held low.

Communicating with the bq2014H

The bq2014H includes a simple single-pin (HDQ plus return) serial data interface. A host processor uses the interface to access various bq2014H registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain HDQ pin on the bq2014H should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, in which the host processor sends a command byte to the bq2014H. The command directs the bq2014H to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. (See Figure 4.)

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2014H may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs (e.g., t_{CYCB} > 250µs), the bq2014H should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time, t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2014H is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections:

1. The first section is used to start the transmission by either the host or the bq2014H taking the HDQ pin to a logic-low state for a period, $t_{STRH;B}$.
2. The next section is the actual data transmission, where the data should be valid by a period, $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period, $t_{DH;DV}$, to allow the host or bq2014H to sample the data bit.
3. The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period, $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should be until a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2014H is always performed with the bit transmitted first. Figure 5 shows an example of a communication sequence to read the bq2014H NACH register.

bq2014H Command Code and Registers

The bq2014H status registers are listed in Table 8 and described below. All registers are Read/Write in the bq2014H. [illegible] 01 [illegible]

Command Code

The bq2014H latches the command code when eight valid command bits have been received by the bq2014H. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code is used to select whether the received command is for a read or a write function:

The W/$\overline{R}$ values are

Command Code Bits							
7	6	5	4	3	2	1	0
W/$\overline{R}$	-	-	-	-	-	-	-

where W/$\overline{R}$ is

0 The bq2014H outputs the requested register contents specified by the address portion of command code.

1 The following eight bits should be written to the register specified by the address portion of command code.

The lower 7-bit field of the command code contains the address portion of the register to be accessed:

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Primary Status Flags Register (FLGS1)

The FLGS1 register (address = 01h) contains the primary bq2014H flags.

The ***charge status*** flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

where CHGS is

0 Either discharge activity detected or $V_{SRO} \leq V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The ***battery replaced*** flag (BRP) is asserted whenever the bq2014H is reset either by application of V_{CC} or by a serial port command. BRP is reset when either a valid charge action increments NAC to be equal to LMD, or a valid charge action is detected after the EDV1 flag is asserted. BRP = 1 signifies that the device has been reset.

The BRP values are

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

where BRP is

0 Battery is charged until NAC = LMD or discharged until the EDV1 flag is asserted

1 bq2014H is reset

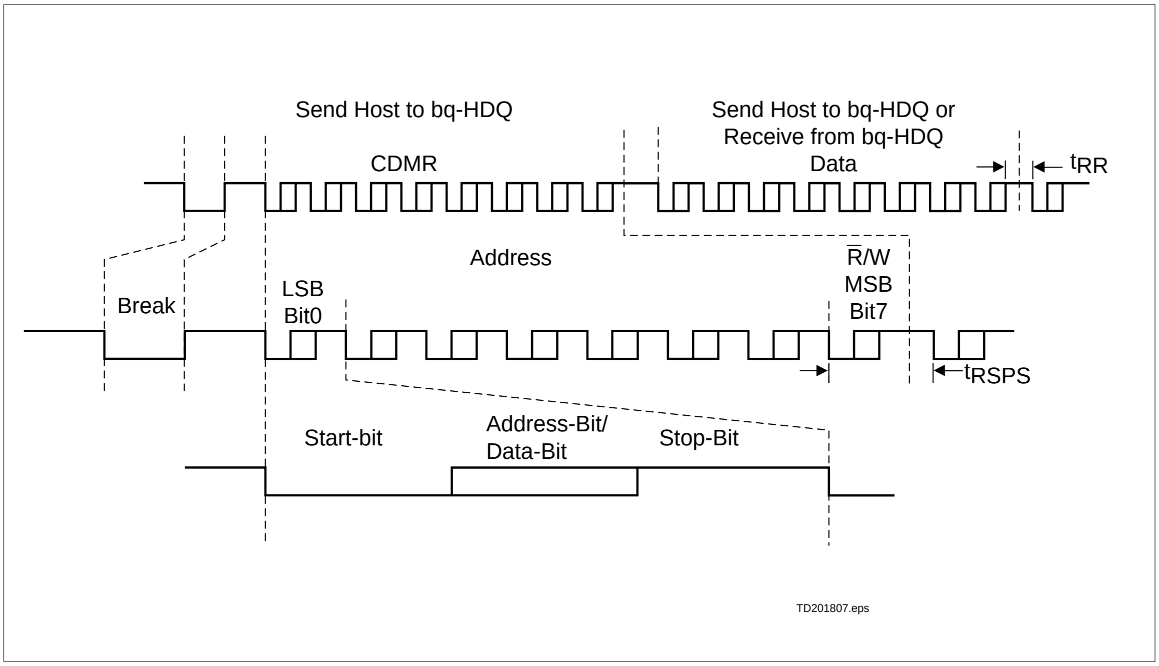


Figure 4. bq2014H Communication Example

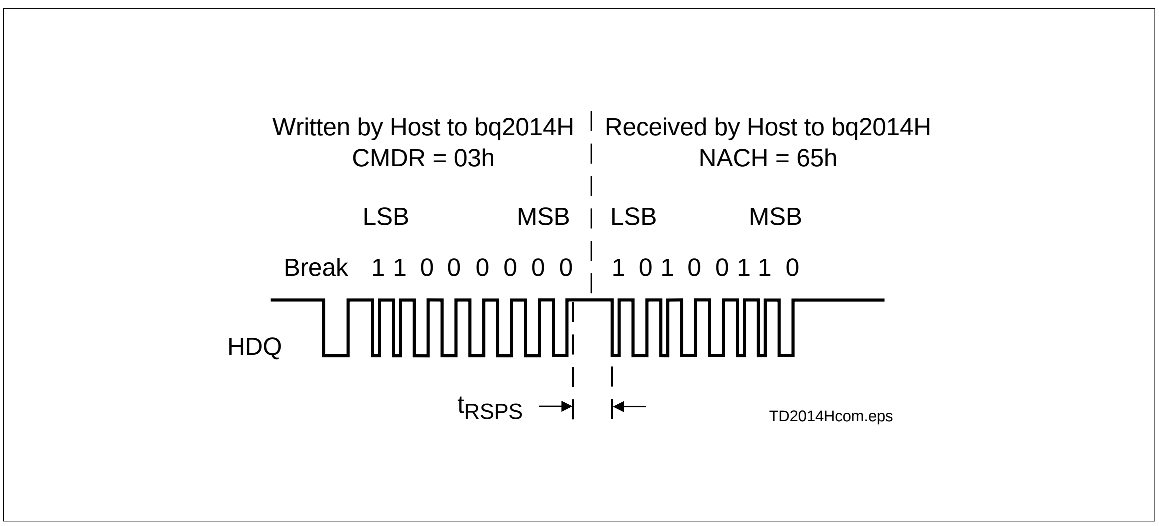


Figure 5. Typical Communication with the bq2014H

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field 7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	Primary status flags register	01h	R	CHGS	BRP	0	CI	VDQ	1	EDV1	EDVF
TMP	Temperature register	02h	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available capac-ity high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available capacity low byte register	17h	R/W	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	R	RSVD	DR2	DR1	DR0	ENINT	VQ	RSVD	OVLD
PPD	Program pin pull-down register	07h	R	RSVD	RSVD	RSVD	PPD5	PPD4	PPD3	PPD2	PPD180(BATID0) T -45.8981 -

RR

The ***capacity inaccurate*** flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2014H is reset. The flag is cleared after an LMD update.

The CI values are

FLGS1 Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	-	CI	-	-	-	-

where CI is

Nominal Available Capacity Registers (NACH/NACL)

The NACH high-byte register (address=03h) and the NACL low-byte register (address=17h) are the main gas gauging registers for the bq2014H. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. NACH and NACL are set to 0 during a bq2014H reset.

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

Program Pin Pull-Down Register (PPD)

The PPD register (address=07h) contains some of the programming pin information for the bq2014H. The segment drivers, SEG_{1-5}, have a corresponding PPD register location, PPD_{1-5}. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xxx01001.

Program Pin Pull-Up Register (PPU)

The PPU register (address=08h) contains the rest of the programming pin information for the bq2014H. The segment drivers, SEG_{1-5}, have a corresponding PPU register location, PPU_{1-5}. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_5 have pull-up resistors, the contents of PPU are xxx10100.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
RSVD	RSVD	RSVD	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Capacity Inaccurate Count Register (CPI)

The CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2014H adapts to the changing capacity over time. A complete discharge from full (NAC $\geq$ 0.94 $*$ LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and there has been no more than a 6% self-discharge reduction.

The CPI register is incremented every time a valid charge is detected. When NAC $\geq$ 0.94 $*$ LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 $*$ LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Battery Voltage Register (VSB)

The battery voltage register is used to read the single-cell battery voltage on the SB pin. The VSB register (address = 0Bh) is updated approximately once per second with the present value of the battery voltage.
V_{SB} = 1.2V $*$ (VSB/256).

VSB Register Bits							
7	6	5	4	3	2	1	0
VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0

Voltage Threshold Register (VTS)

The end-of-discharge threshold voltages (EDV1 and EDVF) can be set using the VTS register (address = 0Ch). The VTS register sets the EDV1 trip point. EDVF is set 25mV below EDV1. The default value in the VTS register is A2h, representing EDV1 = 0.76V and EDVF = 0.735V. EDV1 = 1.2V $*$ (VTS/256).

VTS Register Bits							
7	6	5	4	3	2	1	0
VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0

Compensated Available Charge Registers (CACT/CACD)

The CACD register (address = 0Eh) contains the NAC value compensated for discharge rate. This is a monotonicly decreasing value during discharge. If the discharge rate is > 2C then this value is lower than NAC. CACD is updated only when the discharge rate compensated NAC value is a lower value than CACD during discharge. During charge, CACD is continuously updated with the NAC value.

The CACT register (address = 0Dh) contains the CACD value compensated for temperature. CACT will contain a value lower than CACD when the battery temperature is below 10°C. The CACT value is also used in calculating the LED display pattern.

Scaled Available Energy Registers (SAEH/SAEL)

The SAEH high-byte register (address = 0Fh) and the SAEL low-byte register (address = 10h) are used to scale battery voltage and CACT to a value that can be translated to watt-hours remaining under the present conditions.

Relative CAC Register (RCAC)

The RCAC register (address = 11h) provides the relative battery state-of-charge by dividing CACT by LMD.

RCAC varies from 0 to 64h representing relative state-of-charge from 0 to 100%.

Current Scale Register (VSRH/VSRL)

The VSRH register (address = 12h) and the VSRL register (address = 13h) report the average signal across the SR and V_{SS} pins. The bq2050H updates this register pair every 22.5s. V_{SRH} (high-byte) and V_{SRL} (low-byte) form a 16-bit signed integer value representing the average current during this time. The battery pack current can be calculated from:

$$|I(mA)| = (V_{SRH} * 256 + V_{SRL})/(8 * R_S)$$

where:

R_S = sense resistor value in Ω.
V_{SRH} = high-byte value of battery current
V_{SRL} = low-byte value of battery current

The bq2014H indicates an average discharge current with a "1" in the MSB position of the VSRH register. To calculate discharge current, use the 2's complement if the concatenated register contents in the above equation.

Discharge Count Register (DCR)

The DCR register (address = 18h) stores the high-byte of the discharge count. DCR is reset to zero at the start of a valid discharge cycle and can count to a maximum of FFh. DCR will not increment if EDV1 = 1 and will not roll over from FFh.

Program Pin Full Count (PPFC)

The PPFC register contains information concerning the program pin configuration. This information is used to determine the data integrity of the bq2014H. [illegible]

The recommended reset method for the bq2014H is

- Write PPFC to zero
- Write LMD to zero

After these operations, a software reset will occur.

Resetting the bq2014H sets the following:

- LMD = PFC
- CPI, VDQ, RCAC, NACH/L, CACH/L, SAEH/L, NMCV = 0
- CI and BRP = 1

Voltage Offset (V_{OS}) Interrupt (INTSS)

The INTSS register (address = 38h) is useful during intial characterization of bq2014H designs. When the bq2014H counts a charge pulse, CHGI (bit 0) will be set to 1. When the bq2014H counts a discharge pulse, DCHGI (bit 3) will be set to 1. All other locations in the INTSS register are reserved.

Display

The bq2014H can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2014H displays the battery charge state in relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD.

The capacity display is also adjusted for the present battery temperature and discharge rate. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the CACT and CACD register descriptions.

When $\overline{DISP}$ is tied to V_{CC}, the SEG_{1-5} outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active whenever the bq2014H detects a charge in progress $V_{SRO} > V_{SRQ}$. When pulled low, the segment outputs become active for a period of four seconds, ± 0.5 seconds.

The segment outputs are modulated as two banks, with segments 1, 3, and 5 alternating with segments 2 and 4. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

A micropower source for the bq2014H can be inexpensively built using a FET and an external resistor. (See Figure 1.)

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	Relative to V_{SS}	-0.3	+7.0	V	
All other pins	Relative to V_{SS}	-0.3	+7.0	V	
REF	Relative to V_{SS}	-0.3	+8.5	V	Current limited by R1 (see Figure 1)
V_{SR}	Relative to V_{SS}	-0.3	Vcc+0.7	V	100kΩ series resistor should be used to protect SR in case of a shorted battery.
T_{OPR}	Operating temperature	0	+70	°C	Commercial

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDV1}	First empty warning	0.73	0.76	0.79	V	SB, default
V_{EDVF}	Final empty warning	V_{EDV1} - 0.035	V_{EDV1} - 0.025	V_{EDV1} - 0.015	V	SB, default
V_{SRO}	SR sense range	-300	-	+500	mV	SR, V_{SR} + V_{OS}
V_{SRQ}	Valid charge	250	-	-	µV	V_{SR} + V_{OS} (see note)
V_{SRD}	Valid discharge	-	-	-250	µV	V_{SR} + V_{OS} (see note)

Note: V_{OS} is affected by PC board layout. Proper layout guidelines should be followed for optimal performance. See “LayoutConsiderations.”

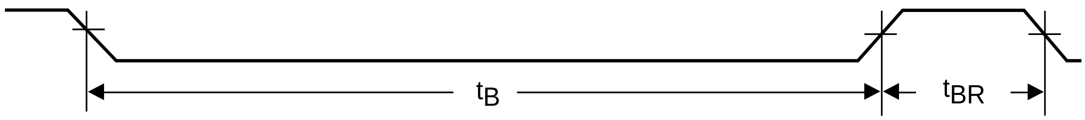
DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{OS}	Offset referred to V_{SR}	-	±50	±150	µV	$\overline{DISP}$ = VCC
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, HDQ = 0
		-	120	180	µA	V_{CC} = 4.25V, HDQ = 0
		-	170	250	µA	V_{CC} = 6.5V, HDQ = 0
V_{SB}	Battery input	0	-	V_{CC}	Vam	VSuBinput impedance

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

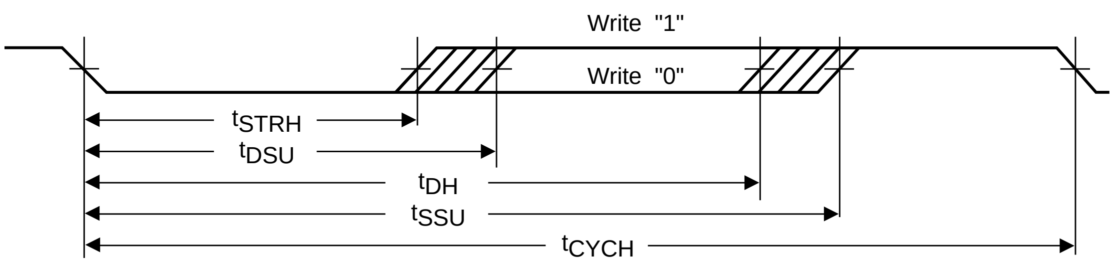
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes

Break Timing

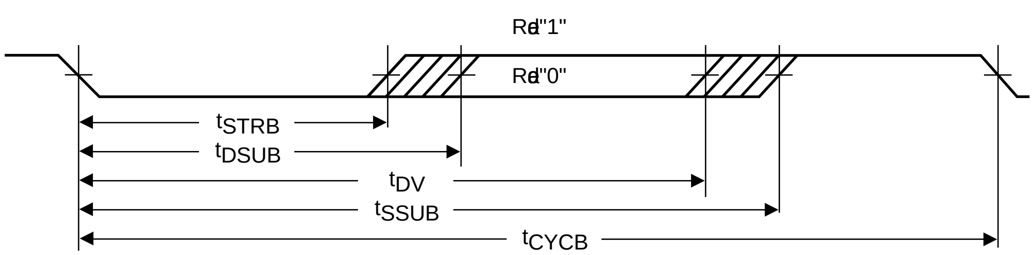


TD201803.eps

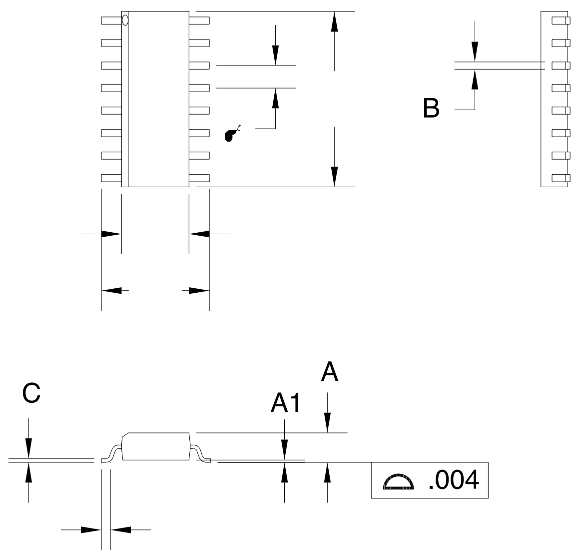
Host to bq2014H



bq2014H to Host



16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

Dimension	Inches Min.	Inches Max.	Millimeters Min.	Millimeters Max.
A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
e	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

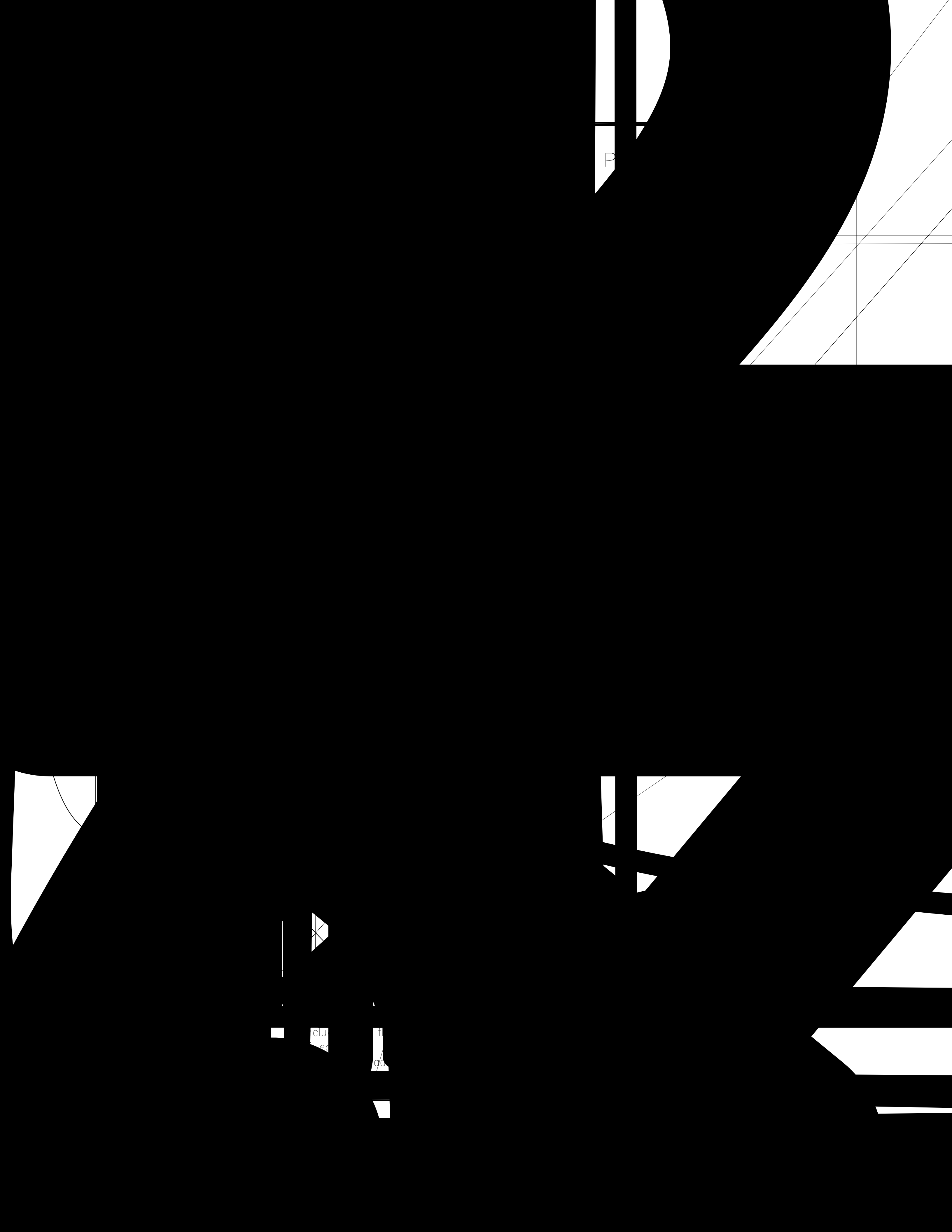
Ordering Information

bq2014H _ _

Temperature Range:
blank = Commercial (0 to +70°C)

Package Option:
SN = 16-pin narrow SOIC

Device:
bq2014H Gas-Gauge IC



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.

D. Laser cutting apertur
contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.

=. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All semiconductor products (also referred to herein as “components”) are sold subject to TI’s terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its components to the specifications applicable at the time of sale, in accordance with the warranty in TI’s terms and conditions of sale of semiconductor products. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by applicable law, testing of all parameters of each component is not necessarily performed.

TI assumes no liability for applications assistance or the design of Buyers’ products. Buyers are responsible for their products and applications using TI components. To minimize the risks associated with Buyers’ products and applications, Buyers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI components or services are used. Information published by TI regarding third-party products or services does not constitute a license to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of significant portions of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI components or services with statements different from or beyond the parameters stated by TI for that component or service voids all express and any implied warranties for the associated TI component or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyer acknowledges and agrees that it is solely responsible for compliance with all legal, regulatory and safety-related requirements concerning its products, and any use of TI components in its applications, notwithstanding any applications-related information or support that may be provided by TI. Buyer represents and agrees that it has all the necessary expertise to create and implement safeguards which anticipate dangerous consequences of failures, monitor failures and their consequences, lessen the likelihood of failures that might cause harm and take appropriate remedial actions. Buyer will fully indemnify TI and its representatives against any damages arising out of the use of any TI components in safety-critical applications.

In some cases, TI components may be promoted specifically to facilitate safety-related applications. With such components, TI’s goal is to help enable customers to design and create their own end-product solutions that meet applicable functional safety standards and requirements. Nonetheless, such components are subject to these terms.

No TI components are authorized for use in FDA Class III (or similar life-critical medical equipment) unless authorized officers of the parties have executed a special agreement specifically governing such use.

Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of