15V/±4A High-Efficiency PWM Power Driver

Check for Samples: DRV595

FEATURES

- **±4 A Output Current**
- **Wide Supply Voltage Range: 4.5 V – 26 V**
- **High Efficiency Generates Less Heat**
- **Multiple Switching Frequencies**
  - **Master/Slave Synchronization**
  - **Up to 1.2 MHz Switching Frequency**
- **Feedback Power Stage Architecture with High PSRR Reduces PSU Requirements**
- **Single Power Supply Reduces Component Count**
- **Integrated Self-Protection Circuits Including Over-Voltage, Under-Voltage, Over-Temperature, and Short Circuit with Error Reporting**
- **Thermally Enhanced Package**
  - **DAP (32-pin HTSSOP Pad-down)**
- **–40°C to 85°C Ambient Temperature Range**

APPLICATIONS

- **Power Line Communications (PLC) Driver**
- **Thermoelectric Cooler (TEC) Driver**
- **Laser Diode Biasing**
- **Motor Driver**
- **Servo Amplifier**

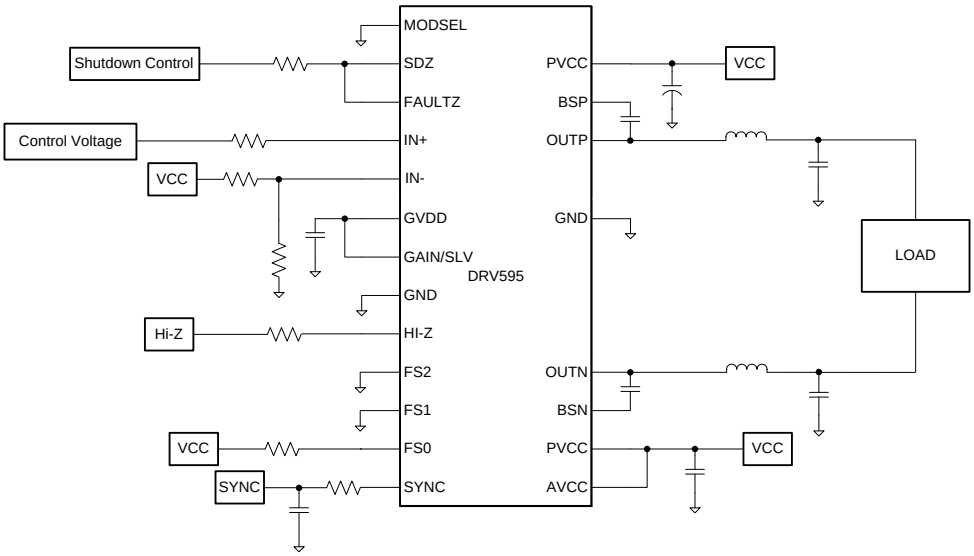
DESCRIPTION

The DRV595 is a high-efficiency, high-current power driver ideal for driving a wide variety of loads in systems powered from 4.5V to 26V. PWM operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV595 advanced oscillator/PLL circuit employs multiple switching frequency options; this is achieved together with a Master/Slave option, making it possible to synchronize multiple devices.

The DRV595 is fully protected against faults with short-circuit, thermal, over-voltage, and under-voltage protection. Faults are reported back to the processor to prevent devices from being damaged during overload conditions.

SIMPLIFIED APPLICATION CIRCUIT



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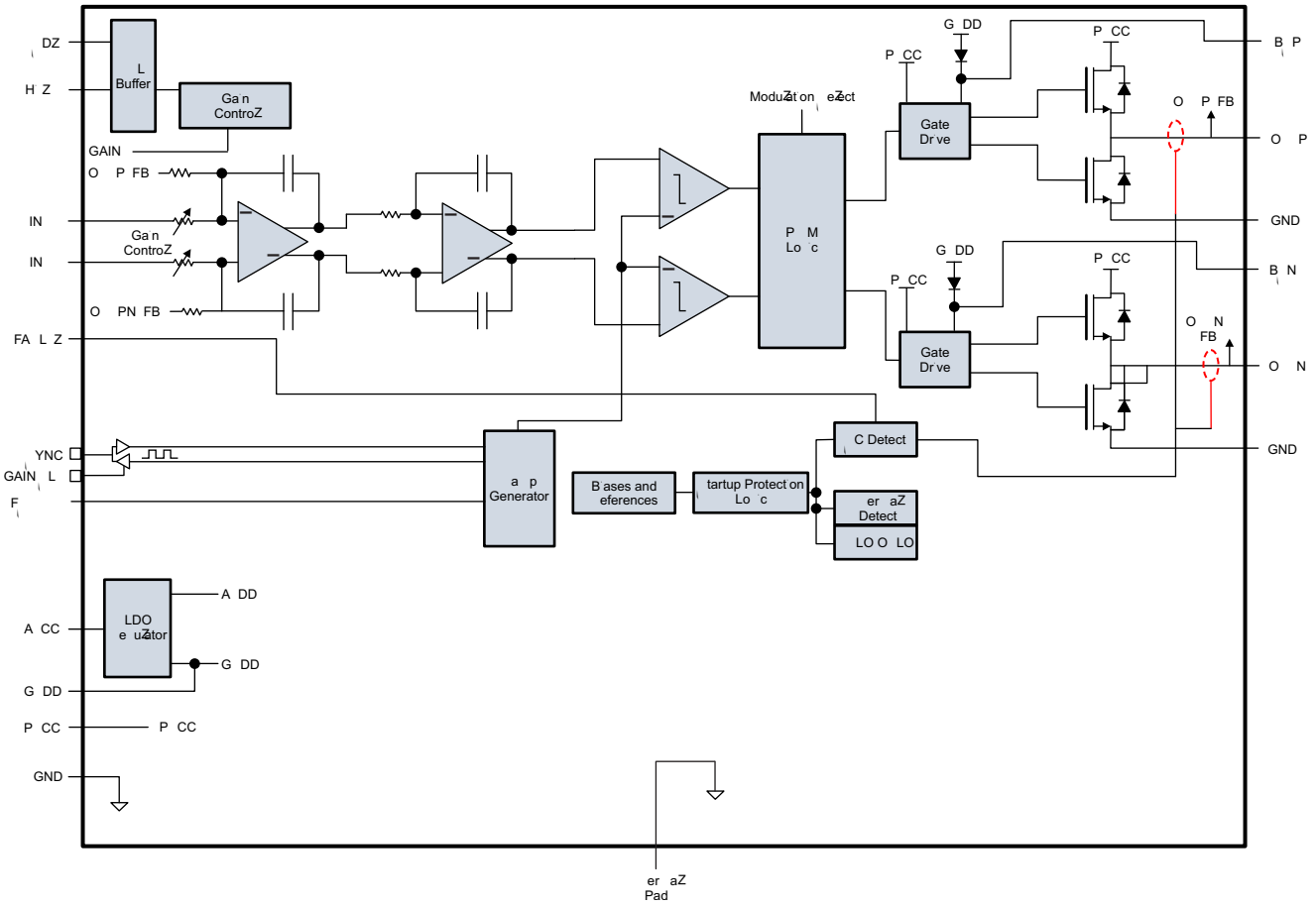
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SYSTEM BLOCK DIAGRAM



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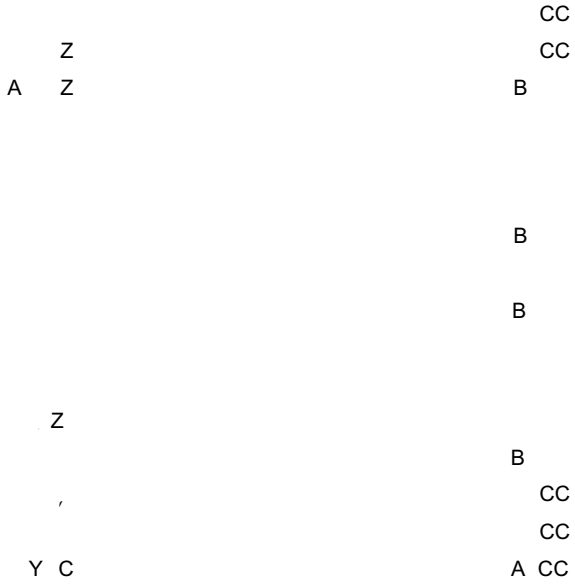
PINOUT CONFIGURATION

DRV595
32-PIN HTSSOP Package (DAP)
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	MODSEL	I	Mode selection logic input (LOW = BD mode, HIGH = 1SPW mode). TTL logic levels with compliance to AVCC.
2	SDZ	I	Shutdown logic input (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC.
3	FAULTZ	DO	General fault reporting. Open drain. See Table 3 FAULTZ = High, normal operation FAULTZ = Low, fault condition
4	IN+	I	Positive differential input. Biased at 3 V.
5	IN–	I	Negative differential input. Biased at 3 V.
6, 7	GVDD	PO	Internally generated gate voltage supply. Not to be used as a supply or connected to any component other than a 1 µF X7R ceramic decoupling capacitor and the GAIN/SLV resistor divider.
8	GAIN/SLV	I	Selects Gain and selects between Master and Slave mode depending on pin voltage divider.
9, 10, 11	GND	G	Ground
12	Hi-Z	I	Input for fast disable/enable of outputs (HIGH = outputs Hi-Z, LOW = outputs enabled). TTL logic levels with compliance to AVCC.
13	FS2	I	Frequency Selection input, used to select oscillator frequencies from 400kHz to 1200kHz.
14	FS1	I	Frequency Selection input, used to select oscillator frequencies from 400kHz to 1200kHz.
15	FS0	I	Frequency Selection input, used to select oscillator frequencies from 400kHz to 1200kHz.
16	SYNC	DIO	Clock input/output for synchronizing multiple devices. Direction determined by GAIN/SLV terminal.
17	AVCC	P	Analog Supply, can be connected to PVCC for single power supply operation.
18, 19	PVCC	P	Power supply
20, 24	BSN	BST	Boot strap for negative output, connect to 220 nF X5R, or better ceramic cap to OUTN
21	OUTN	PO	Negative output
22	GND	G	Ground
23	OUTN	PO	Negative output
25	GND	G	Ground
26, 30	BSP	BST	Boot strap for positive output, connect to 220 nF X5R, or better ceramic cap to OUTP

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TYPICAL CHARACTERISTICS

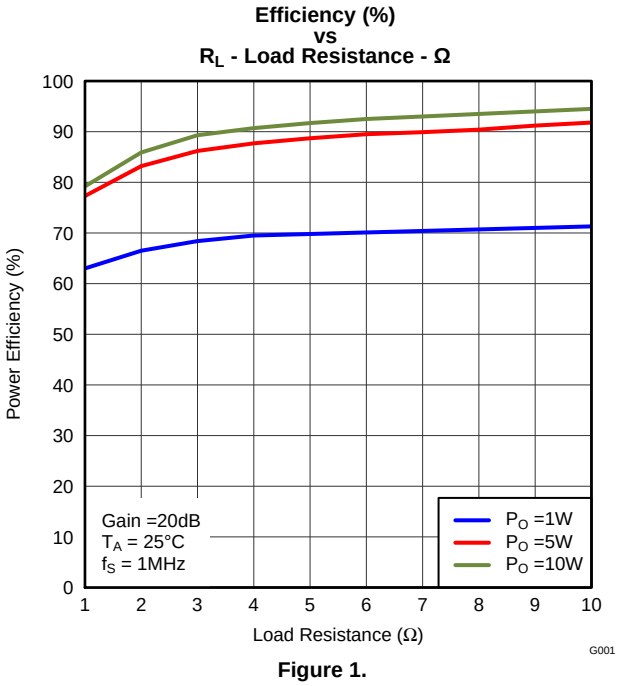

Figure 1.

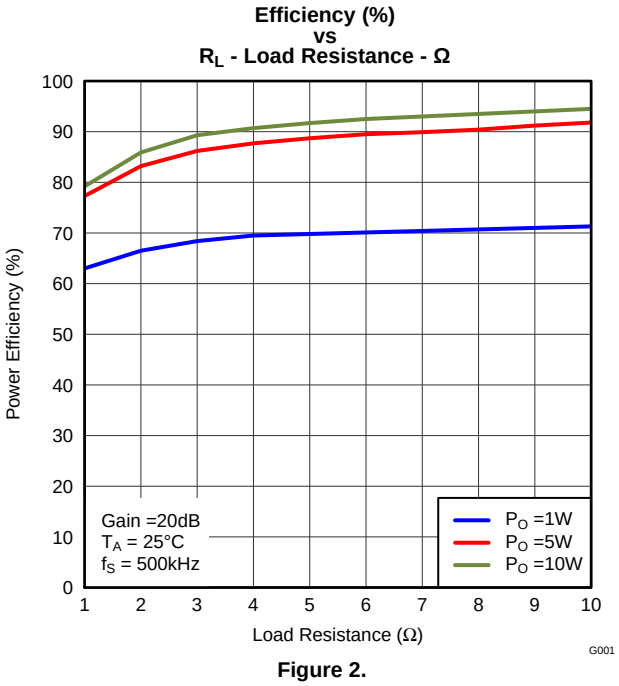

Figure 2.

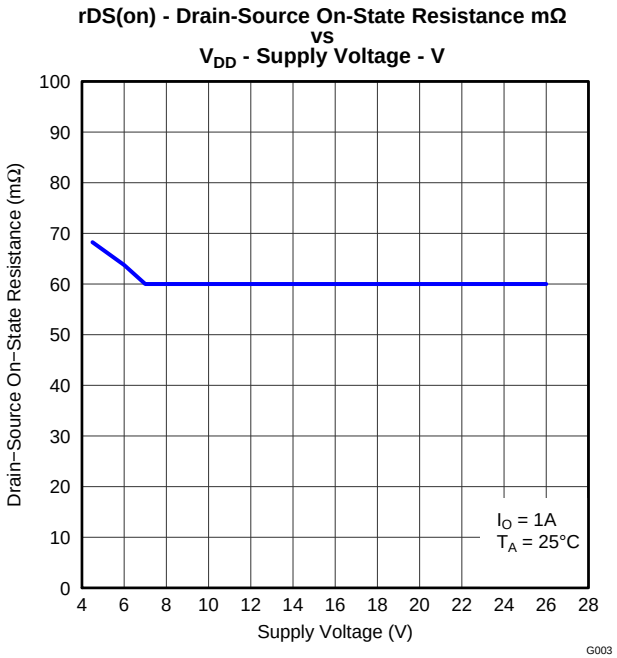

Figure 3.

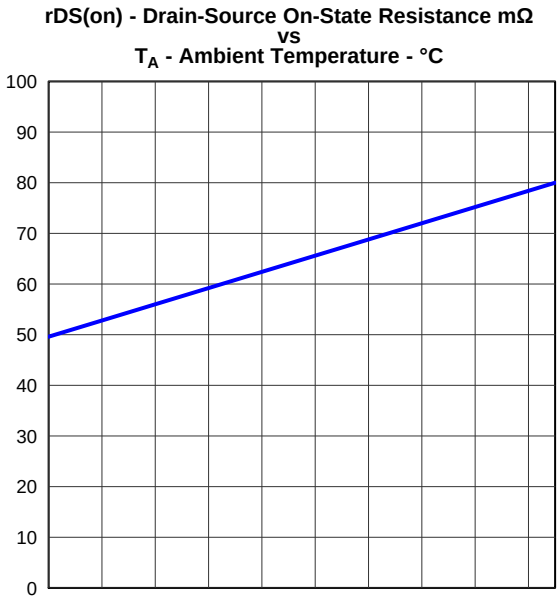

Figure 4.

TYPICAL CHARACTERISTICS (continued)

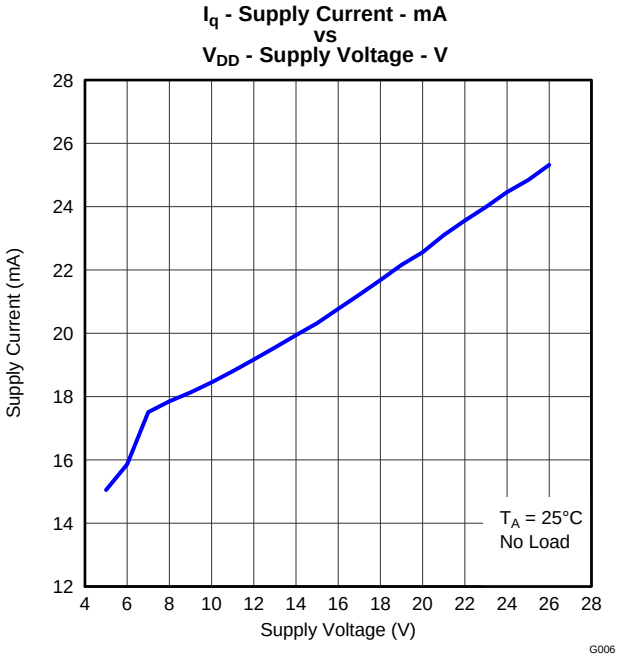

Figure 5.

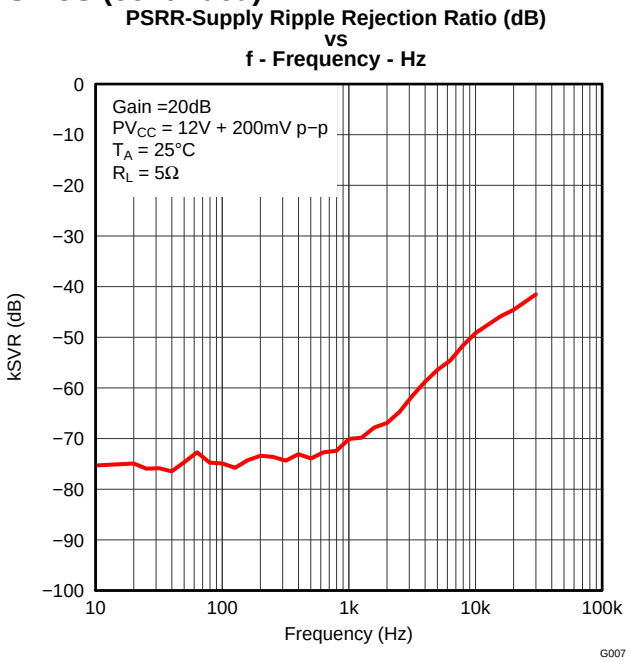

Figure 6.

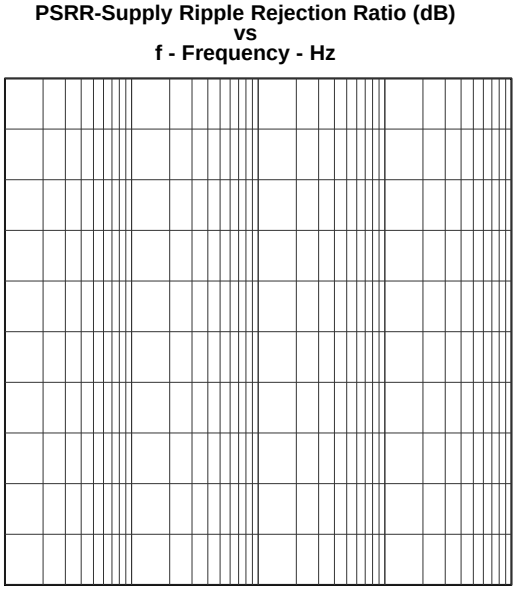

Figure 7.

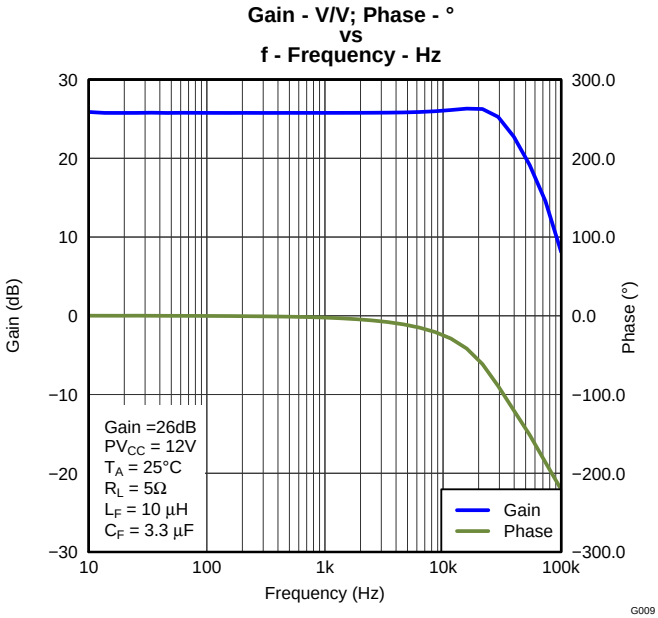

Figure 8.

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TYPICAL CHARACTERISTICS (continued)

Gain - V/V; Phase - °
vs
f - Frequency - Hz

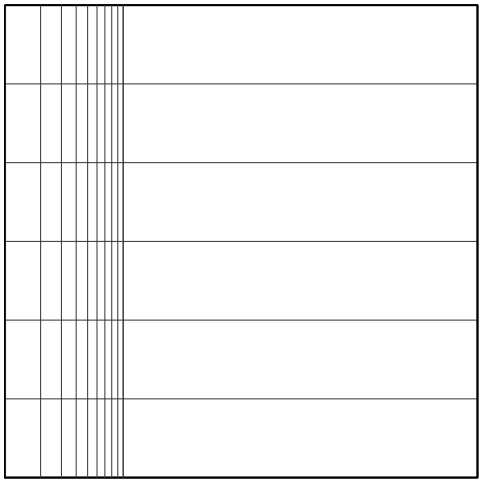

Figure 9.

V_{IO} - Input Offset Voltage - mV
vs
V_{IC} - Common-Mode Input Voltage - V

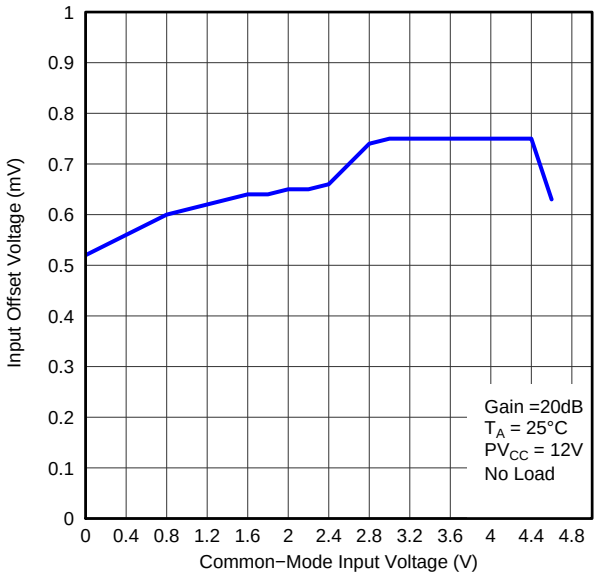

Figure 10.

V_{IO} - Input Offset Voltage - mV
vs
V_{IC} - Common-Mode Input Voltage - V

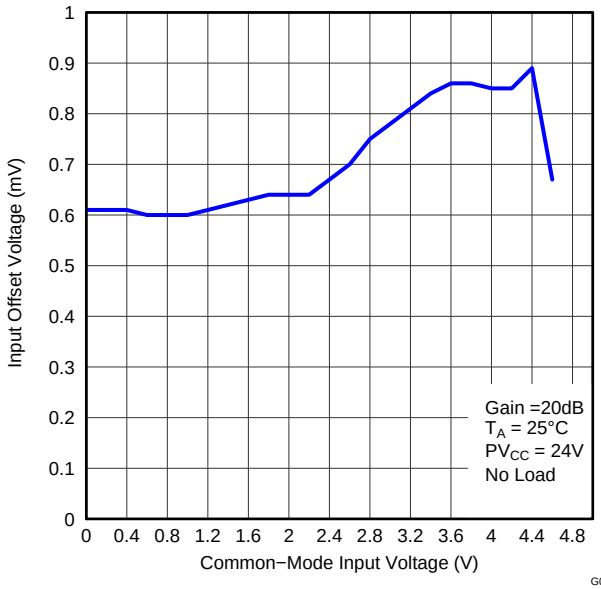

Figure 11.

APPLICATION INFORMATION

OUTPUT FILTER CONSIDERATIONS

The DRV595 can be used to drive a TEC element. The typical circuit used for this application is to have two feedback loops – one for constant current, and the second to monitor the temperature, and provide adjustments to keep a constant temperature on the laser diode. An error amplifier is used to combine the two feedback loops, along with a control signal from the system. The output of the error amplifier is then fed into the DRV595.

An output filter needs to be used to prevent excessive ripple from reaching the TEC element. Some TEC elements may be damaged by ripple; design the filter using the TEC specification to reduce the switching waveform enough to prevent TEC damage. This filter also reduces the amount of electrical noise coupled onto the TEC element.

For most applications, a second-order Butterworth low-pass filter with the cut-off frequency set to a few kilohertz should be sufficient. See Figure 12 for example filter designed with Equation 2, Equation 3, and Equation 4 .

Second-Order Butterworth LPF Transfer Function

$$H(s) = \frac{1}{s^2 + \sqrt{2}s + 1} \tag{1}$$

Using Half-Circuit Analysis

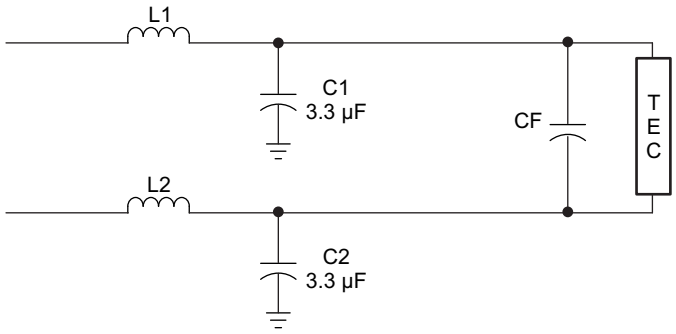

Figure 12. Second Order Butterworth Low-Pass Filter Configuration

$$L_x = \frac{\sqrt{2} \times R_L}{2\omega_o} \tag{2}$$

$$2 \quad C_F \quad \frac{\sqrt{2}}{2 \quad \frac{R_L}{2}} \quad 0 \tag{3}$$

$$\omega_0 = 2\pi \times f \tag{4}$$

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DEVICE INFORMATION

TYPICAL APPLICATION

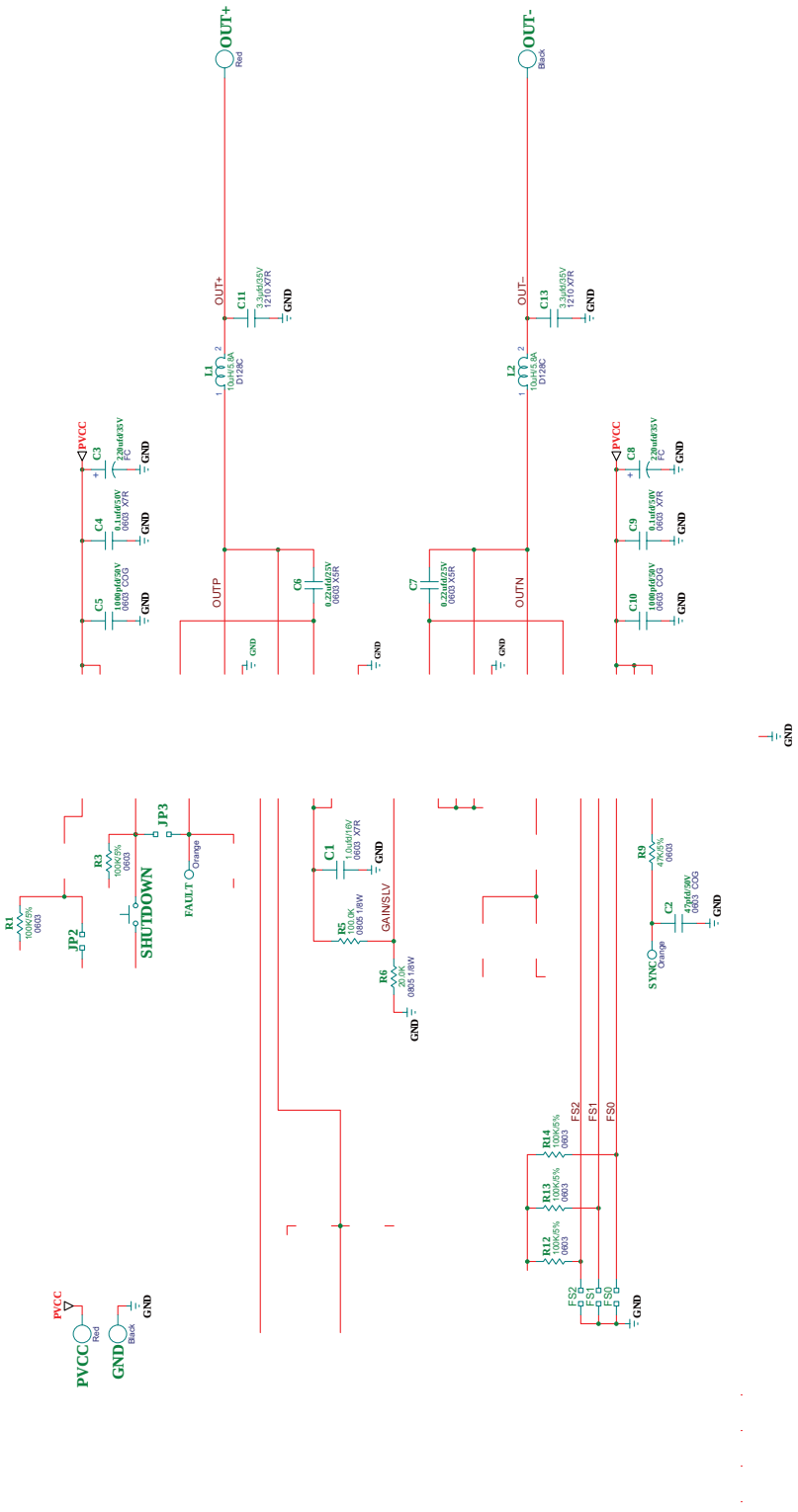

Figure 13. Schematic

START-UP SEQUENCING

To ensure proper operation on power up, wait 10ms after PV_{CC} and AV_{CC} are stable before using the analog inputs, IN– and IN+. Figure 14 illustrates this sequence.

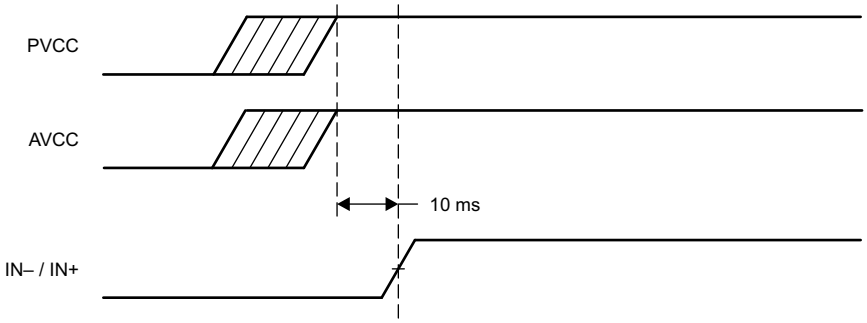

Figure 14. Start-Up Sequencing (1)

(1) NOTE: The timing relationship between PVCC assertion and AVCC assertion is not critical.

GAIN SETTING AND MASTER / SLAVE

The gain of the DRV595 is set by the voltage divider connected to the GAIN/SLV control pin. Master or slave mode is also controlled by the same pin. An internal ADC is used to detect the 4 input states. The first four states set the DRV595 in Master mode with gains of 20, 26, 32, 36 dB respectively, while the next four states set the DRV595 in Slave mode with gains of 20, 26, 32, 36 dB respectively. The gain setting is latched during power-up and cannot be changed while the device is powered. Table 1 shows the recommended resistor values for each mode and gain combination:

Table 1. GAIN and MASTER/SLAVE

MASTER / SLAVE MODE	GAIN	R1 (to GVDD)	R2 (to GND)	INPUT IMPEDANCE
Master	20 dB	OPEN	20 k	60 k
Master	26 dB	100 k	20 k	30 k
Master	32 dB	100 k	39 k	15 k
Master	36 dB	75 k	47 k	9 k
Slave	20 dB	51 k	51 k	60 k
Slave	26 dB	47 k	75 k	30 k
Slave	32 dB	39 k	100 k	15 k
Slave	36 dB	16 k	100 k	9 k

In Master mode, the SYNC terminal is an output, in Slave mode, the SYNC terminal is an input for a clock input. TTL logic levels with compliance to GVDD.

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INPUT IMPEDANCE

The DRV595 input stage is a fully differential input stage and the input impedance changes with the gain setting from 9 k at 36 dB gain to 60 k at 20 dB gain. Table 1 lists the values from min to max gain. The tolerance of the input resistor value is ±20% so the minimum value will be higher than 7.2 k .

Table 2. Recommended Input AC-Coupling Capacitors

GAIN	INPUT IMPEDANCE
20 dB	60 k
26 dB	30 k
32 dB	15 k
36 dB	9 k

START-UP/SHUTDOWN OPERATION

The DRV595 employs a shutdown mode of operation designed to reduce supply current (Icc) to the absolute minimum level during periods of non use for power conservation. The SDZ input terminal should be held high (see specification table for trip point) during normal operation when the amplifier is in use. Pulling SDZ low will put the outputs to Hi-Z and the amplifier to enter a low-current state. It is not recommended to leave SDZ unconnected, because amplifier operation would be unpredictable.

GVDD SUPPLY

The GVDD Supply is used to power the gates of the output full bridge transistors. It can also be used to supply the GAIN/SLV voltage divider. Decouple GVDD with a X5R ceramic 1 µF capacitor to GND. The GVDD supply is not intended to be used as an external supply. It is recommended to limit the current consumption by using resistor voltage dividers for GAIN/SLV of 100 k or more.

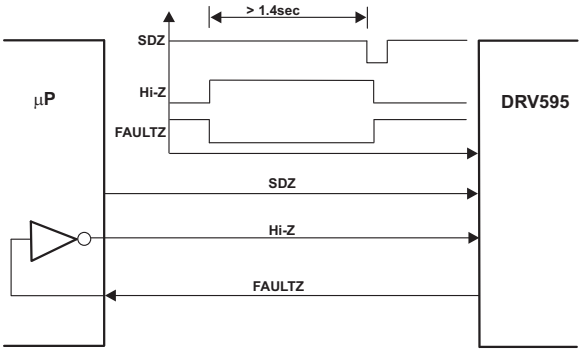
BSP AND BSN CAPACITORS

The fullNMOS

high side of each output to turn on correctly. A 220 nF ceramic capacitor of quality X5R or better, rated for at least 16 V, must be connected from each output to its corresponding bootstrap input. (See the application circuit diagram in Figure 13.)

DEVICE PROTECTION SYSTEM

The DRV595 contains a complete set of protection circuits carefully designed to make system design efficient as well as to protect the device against permanent failures due to short circuits, overload,



This is a modulation scheme that allows for smaller ripple current through the TEC load. Each output switches from 0 volts to the supply voltage. With no input, OUTP and OUTN are in phase with each other so that there is little or no current in the load. The duty cycle of OUTP is greater than 50% and OUTN is less than 50% for positive output voltages. The duty cycle of OUTP is less than 50% and OUTN is greater than 50% for negative output voltages. The voltage across the load sits at 0V throughout most of the switching period, reducing the switching current, which reduces any I^2R losses in the load.

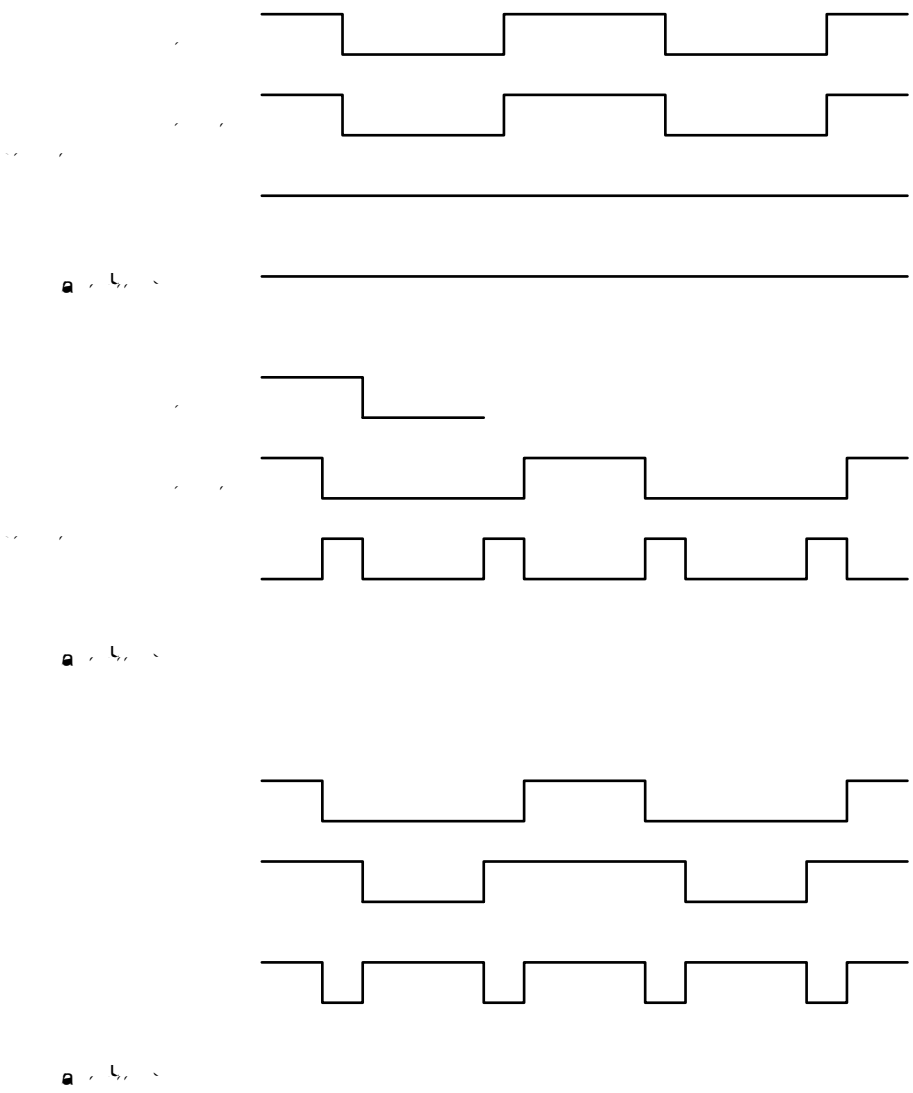


Figure 16. BD Mode Modulation

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POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURE

Though the DRV595 is much more efficient than traditional linear solutions, the power drop across the on-resistance of the output transistors does generate some heat in the package, which may be calculated as shown in Equation 5:

$$P_{DISS} = \left(I_{OUT}\right)^2 \times r_{DS(on),\ total} \quad \text{For example, at the maximum output current of 3 A through a total on-resistance of 60 m (at } T_J = 25°C\text{), the power dissipated in the package is 1.1 W.} \tag{5}$$

Calculate the maximum ambient temperature using Equation 6:

$$T_A = T_J - \left(\theta_{JA} \times P_{DISS}\right) \tag{6}$$

PRINTED-CIRCUIT BOARD (PCB LAYOUT)

It is necessary to take care when planning the layout of the printed circuit board. The following suggestions will help to meet EMC requirements.

- Decoupling capacitors — The high-frequency decoupling capacitors should be placed as close to the PVCC and AVCC terminals as possible. Large (100 F or greater) bulk power supply decoupling capacitors should be placed near the DRV595 on the PVCC supplies. Local, high-frequency bypass capacitors should be placed as close to the PVCC pins as possible. These caps can be connected to the IC GND pad directly for an excellent ground connection. Consider adding a small, good quality low ESR ceramic capacitor between 220 pF and 1 nF and a larger mid-frequency cap of value between 100 nF and 1 µF also of good quality to the PVCC connections at each end of the chip.
- Grounding — The PVCC decoupling capacitors should connect to GND. All ground should be connected at the IC GND, which should be used as a central ground connection or star ground for the DRV595.

For an example layout, see the DRV595 Evaluation Module (DRV595EVM) User Manual. Both the EVM user's manual and the thermal pad application report are available on the TI Web site at http://www.ti.com.

REVISION HISTORY

Changes from Original (December 2012) to Revision A — **Page**

- Changed Title From: 15V/±3A High-Efficiency PWM Power Driver To: 15V/±4A High-Efficiency PWM Power Driver 1
- Changed Feature From: ±3 A Output Current To: ±4 A Output Current 1
- Changed the Over current trip point TYP value From: 3 A To: 7.5 A 6

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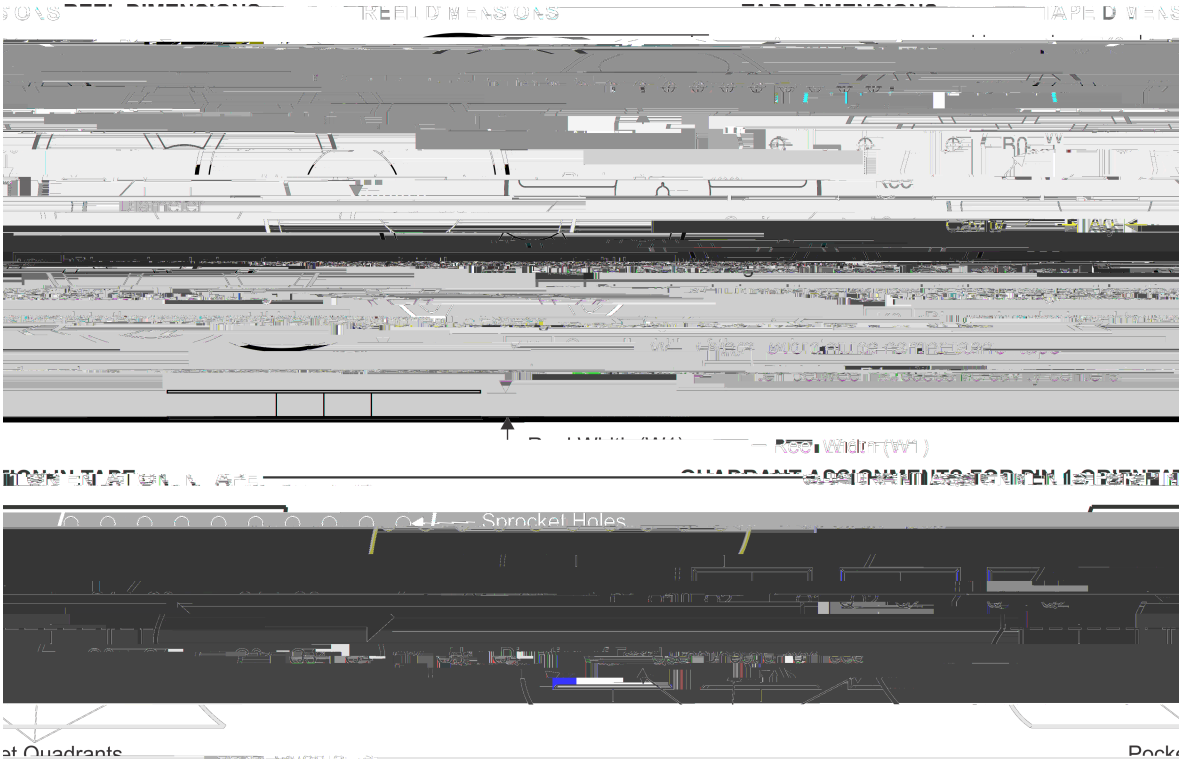
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV595DAP	ACTIVE	HTSSOP	DAP	32	46	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV595	Samples
DRV595DAPR	ACTIVE	HTSSOP	DAP	32	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DRV595	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

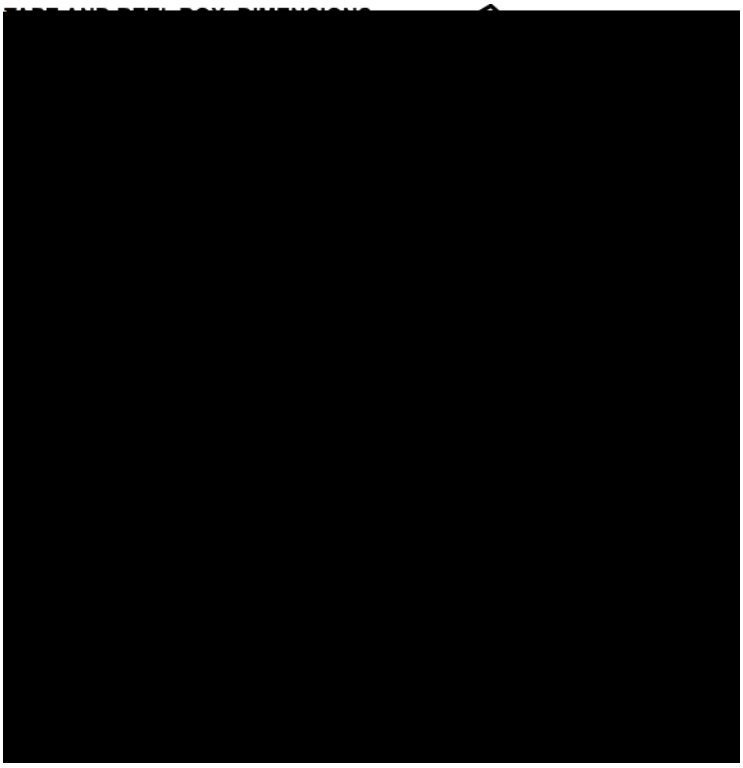
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): [illegible] re b-Free""Pb-Fr

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV595DAPR	HTSSOP	DAP	32	2000	330.0	24.4	8.6	11.5	1.6	12.0	24.0	Q1



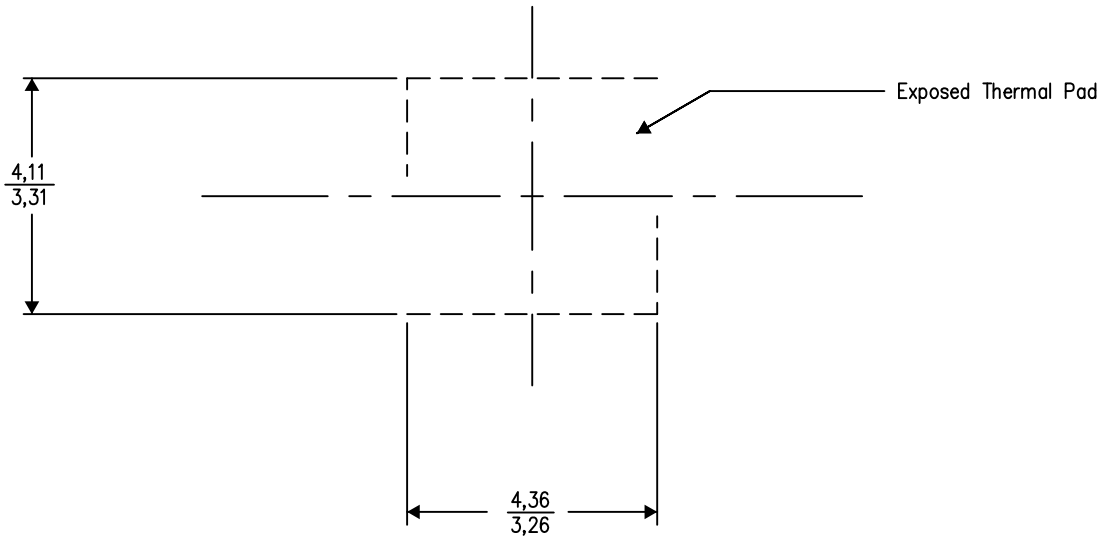
*All dimensions are nominal

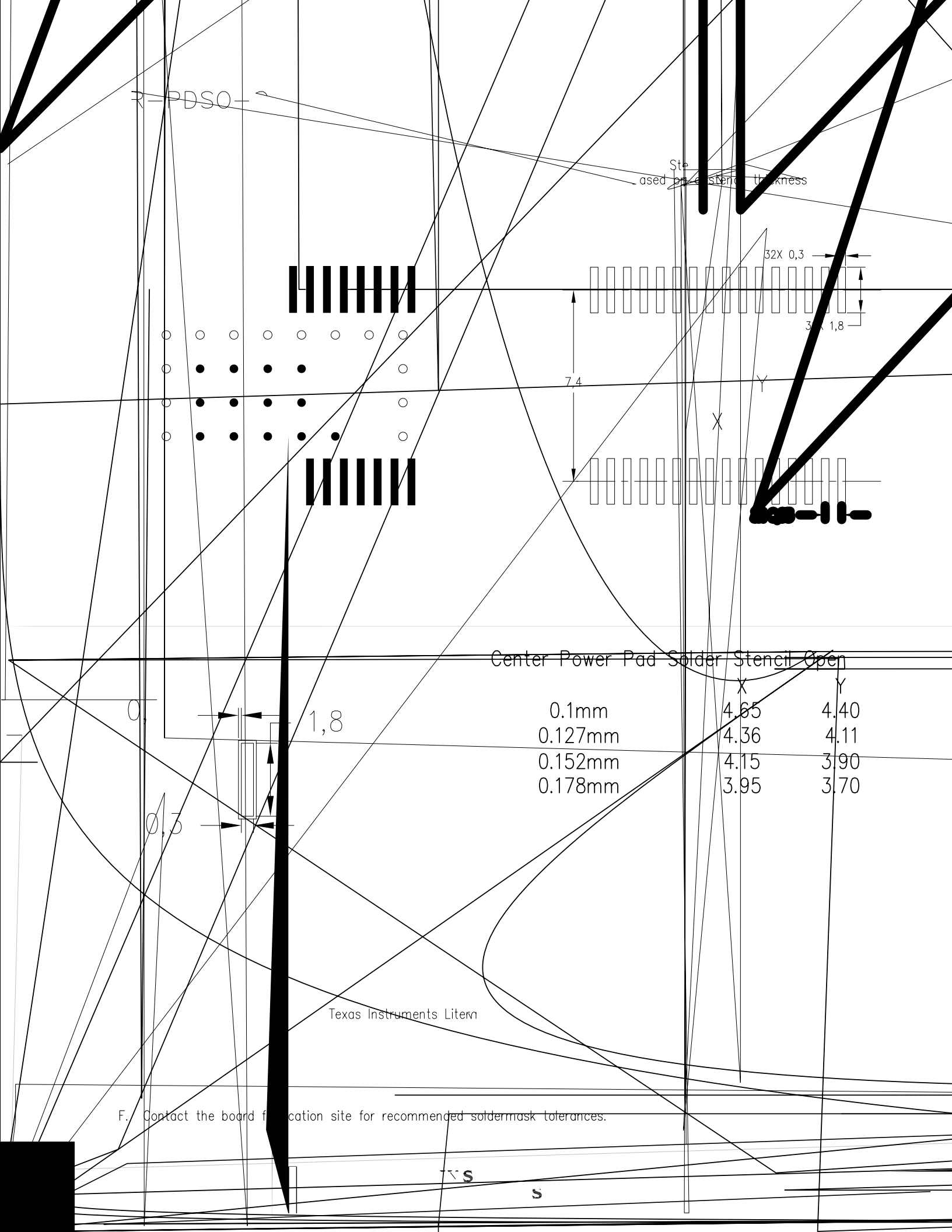
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV595DAPR	HTSSOP	DAP	32	2000	367.0	367.0	45.0

transfer from the integrated circuit (IC).

cdvantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both (

The exposed thermal pad dimensions for this package are shown in the following illustration.





Center Power Pad Solder Stencil Open

	X	Y
0.1mm	4.65	4.40
0.127mm	4.36	4.11
0.152mm	4.15	3.90
0.178mm	3.95	3.70

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F. Contact the board fabrication site for recommended soldermask tolerances.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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