UNITRODE

bq2010

Gas Gauge IC

Features

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for battery pack integration
  - 120µA typical standby current
  - Small size enables implementations in as little as ½ square inch of PCB
- Integrate within a system or as a stand-alone device
  - Display capacity via single-wire serial communication port or direct drive of LEDs
- Measurements compensated for current and temperature
- Self-discharge compensation using internal temperature sensor
- Accurate measurements across a wide range of current (> 500:1)
- 16-pin narrow SOIC

General Description

The bq2010 Gas Gauge IC is intended for battery-pack or in-system installation to maintain an accurate record of a battery's available charge. The IC monitors a voltage drop across a sense resistor connected in series between the negative battery terminal and ground to determine charge and discharge activity of the battery.

NiMH and NiCd battery self-discharge is estimated based on an internal timer and temperature sensor. Compensations for battery temperature and rate of charge or discharge are applied to the charge, discharge, and self-discharge calculations to provide available charge information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or "learned," in the course of a discharge cycle from full to empty.

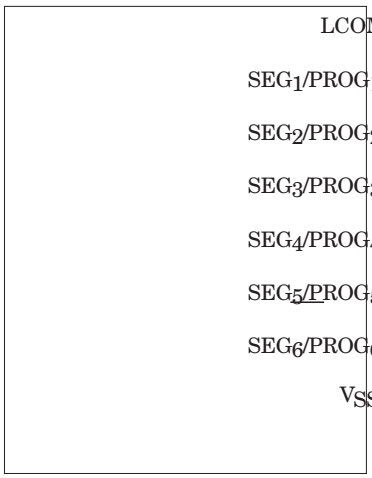
Nominal available charge may be directly indicated using a five- or six-segment LED display. These segments are used to indicate graphically the nominal available charge.

The bq2010 supports a simple single-line bidirectional serial link to an external processor (common ground). The bq2010 outputs battery information in response to external commands over the serial link.

The bq2010 may operate directly from 3 or 4 cells. With the REF output and an external transistor, a simple, inexpensive regulator can be built to provide V_{CC} across a greater number of cells.

Internal registers include available charge, temperature, capacity, battery ID, battery status, and programming pin settings. To support subassembly testing, the outputs may also be controlled. The external processor may also overwrite some of the bq2010 gas gauge data registers.

Pin Connections



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Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	NC	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	EMPTY	Empty battery indicator output
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$SEG_6/PROG_6$	LED segment 6/ program 6 input	SR	Sense resistor input
		V_{CC}	3.0–6.5V
		V_{SS}	System ground

Pin Descriptions

Open-drain output switches V_{CC} to source current for the LEDs. The switch is off during initialization to allow reading of the soft pull-up or pull-down program resistors. LCOM is also high impedance when the display is off.

Each output may activate an LED to sink the current sourced from LCOM.

These three-level input pins define the programmed full count (PFC) thresholds described in Table 2.

These three-level input pins define the scale factor described in Table 2.

This three-level input pin defines the selfdischarge compensation rate shown in Table 1.

This three-level pin defines the display operation shown in Table 1.

The voltage drop (V_{SR}) across the sense resistor R_S is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the high side of the sense resistor. $V_{SR} < V_{SS}$ indicates discharge, and $V_{SR} > V_{SS}$ indicates charge. The effective voltage drop, V_{SRO}, as seen by the bq2010 is $V_{SR} + V_{OS}$ (see Table 5).

$\overline{DISP}$ high disables the LED display. $\overline{DISP}$ tied to V_{CC} allows $PROG_X$ to connect directly to V_{CC} or V_{SS} instead of through a pull-up or pull-down resistor. $\overline{DISP}$ floating allows the LED display to be active during discharge or charge if the NAC registers update at a rate equivalent to $|V_{SRO}| \geq 4mV$. $\overline{DISP}$ low activates the display. See Table 1.

This input monitors the single-cell voltage potential through a high-impedance resistive divider network for end-of-discharge voltage (EDV) thresholds, maximum charge voltage (MCV), and battery removed.

This open-drain output becomes high-impedance on detection of a valid end-of-discharge voltage (V_{EDVF}) and is low following the next application of a valid charge.

This is an open-drain bidirectional pin.

REF provides a voltage reference output for an optional micro-regulator.

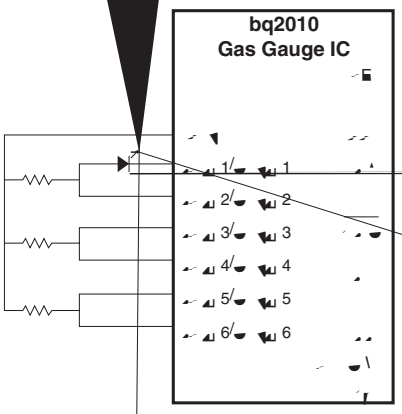
Function n

General Op

The bq2010 dete acity by monitoring the amount of ch removed from a rechargeable battery asures discharge and charge currents, e harge, monitors the battery for low-bat esholds, and compensates for temperatu discharge rates. The charge measurement monitoring the voltage across a small-value resistor between the negative battery term nd. The available battery charge is determi toring this voltage over time and correcting t ment for the environmental and operating co

Figure 1 shows a typical battery pack application of the bq2010 using the LED display capability as a charge-state indicator. The bq2010 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2010 monitors the charge and discharge currents as a voltage across a sense resistor (see R_S in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



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Voltage Thresholds

In conjunction with monitoring V_{SR} for charge/discharge currents, the bq2010 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor/divider network according to the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells, RB_1 is connected to the positive battery terminal, and RB_2 is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). EDV threshold levels are used to determine when the battery has reached an "empty" state, and the MCV threshold is used for fault detection during charging.

Two EDV thresholds for the bq2010 are fixed at:

V_{EDV1} (early warning) = 1.05V

V_{EDVF} (empty) = 0.95V

If V_{SB} is below either of the two EDV thresholds, the associated flag is latched and remains latched, independent of V_{SB}, until the next valid charge. EDV monitoring may be disabled under certain conditions as described in the next paragraph.

During discharge and charge, the bq2010 monitors V_{SR} for various thresholds. These thresholds are used to compensate the charge and discharge rates. Refer to the count compensation section for details. EDV monitoring is disabled if $V_{SR} \leq$ -250mV typical and resumes ½ second after $V_{SR} >$ -250mV.

EMPTY Output

The EMPTY output switches to high impedance when $V_{SB} < V_{EDVF}$ and remains latched until a valid charge occurs. The bq2010 also monitors V_{SB} relative to V_{MCV}, 2.25V. V_{SB} falling from above V_{MCV} resets the device.

Reset

The bq2010 recognizes a valid battery whenever V_{SB} is greater than 0.1V typical. V_{SB} rising from below 0.25V or falling from above 2.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

Temperature

The bq2010 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

Layout Considerations

The bq2010 measures the voltage differential between the SR and V_{SS} pins. V_{OS} (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and V_{CC}) should be placed as close as possible to the SB and V_{CC} pins, respectively, and their paths to V_{SS} should be as short as possible. A high-quality ceramic capacitor of 0.1µf is

Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2010. The bq2010 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2010 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Programmed Full Count (PFC) shown in Table 2. Until LMD is updated, NAC counts up to but not beyond this threshold during subsequent charges. This approach allows the gas gauge to be charger-independent and compatible with any type of charge regime.

1. [illegible]

LMD is the last measured discharge capacity of the battery. On initialization (application of V_{CC} or battery replacement), LMD = PFC. During subsequent discharges, the LMD is updated with the latest measured capacity in the Discharge Count Register (DCR) representing a discharge from full to below EDV1. A qualified discharge is necessary for a capacity transfer from the DCR to the LMD register. The LMD also serves as the 100% reference threshold used by the relative display mode.

2. [illegible]

The initial LMD and gas gauge rate values are programmed by using $PROG_1$–$PROG_4$. The PFC also provides the 100% reference for the absolute display mode. The bq2010 is configured for a given application by selecting a PFC value from Table 2. The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense resistor value:

Battery capacity (mAh) ∗ sense resistor (Ω) = PFC (mVh)

Selecting a PFC slightly less than the rated capacity for absolute mode provides capacity above the full reference for much of the battery's life.

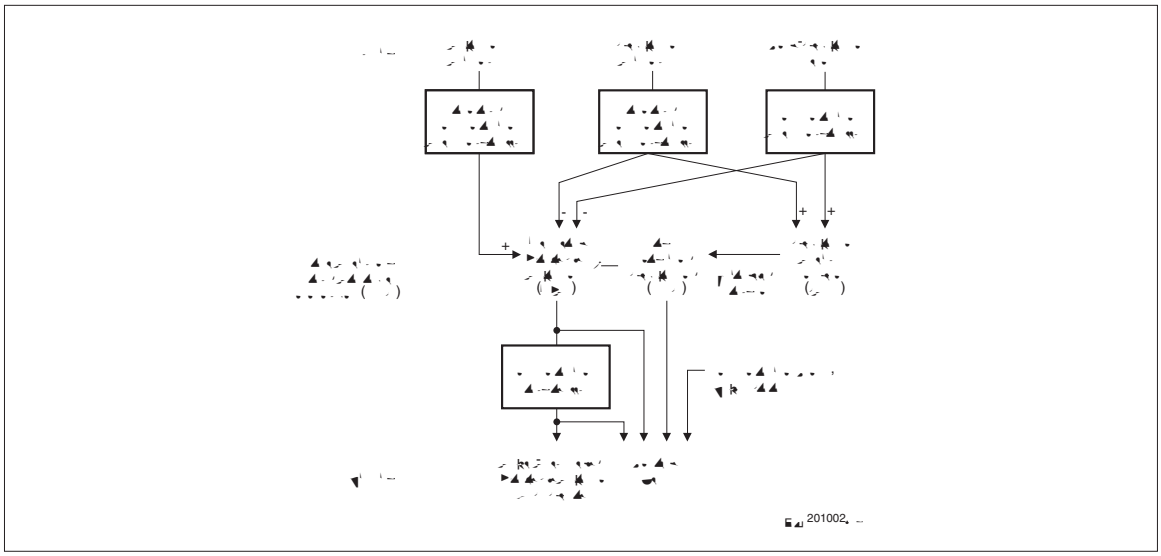


Figure 2. Operational Overview

E ... : S... PFC ...

Given:

Sense resistor = 0.1Ω
Number of cells = 6
Capacity = 2200mAh, NiCd battery
Current range = 50mA to 2A
Absolute display mode
Serial port only
Self-discharge = $\frac{1}{64}$
Voltage drop over sense resistor = 5mV to 200mV

Therefore:

2200mAh ∗ 0.1Ω = 220mVh

Select:

PFC = 33792 counts or 211mVh
$PROG_1$ = float
$PROG_2$ = float
$PROG_3$ = float
$PROG_4$ = low
$PROG_5$ = float
$PROG_6$ = float

The initial full battery capacity is 211mVh (2110mAh) until the bq2010 "learns" a new capacity with a qualified discharge from full to EDV1.

Table 1. bq2010 Programming

Pin Connection	$PROG_5$ Self-Discharge Rate	$PROG_6$ Display Mode	$\overline{DISP}$ Display State
H	Disabled	Absolute NAC = PFC on reset	LED disabled
Z	$\frac{NAC}{64}$	Absolute NAC = 0 on reset	LED-enabled on discharge or charge when equivalent $\lvert V_{SRO} \rvert \geq 4mV$
L	$\frac{NAC}{47}$	Relative NAC = 0 on reset	LED on

... $PROG_5$ and $PROG_6$ states are independent.

Table 2. bq2010 Programmed Full Count mVh Selections

$PROG_x$		Programmed Full Count (PFC)	$PROG_4$ = L			$PROG_4$ = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	Scale = 1/80	Scale = 1/160	Scale = 1/320	Scale = 1/640	Scale = 1/1280	Scale = 1/2560	mVh/ count
H	H	49152	614	307	154	76.8	38.4	19.2	mVh
H	Z	45056	563	282	141	70.4	35.2	17.6	mVh
H	L	40960	512	256	128	64.0	32.0	16.0	mVh
Z	H	36864	461	230	115	57.6	28.8	14.4	mVh
Z	Z	33792	422	211	106	53.0	26.4	13.2	mVh
Z	L	30720	384	192	96.0	48.0	24.0	12.0	mVh
L	H	27648	346	173	86.4	43.2	21.6	10.8	mVh
L	Z	25600	320	160	80.0	40.0	20.0	10.0	mVh
L	L	22528	282	141	70.4	35.2	17.6	8.8	mVh
VSR equivalent to 2 counts/sec. (nom.)			90	45	22.5	11.25	5.6	2.8	mV

3. [illegible]

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. NAC is reset to 0 on initialization ($PROG_6$ = Z or low) and on the first valid charge following discharge to EDV1. NAC is set to PFC on initialization if $PROG_6$ = high. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

4. [illegible]

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches ffffh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V_{EDV1} if:

No valid charge initiations (charges greater than 256 NAC counts, where $V_{SRO} > V_{SRQ}$) occurred during the period between NAC = LMD and EDV1 detected.

The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).

The temperature is ≥ 0°C when the EDV1 level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

Charge Counting

Charge activity is detected based on a positive voltage on the V_{SR} input. If charge activity is detected, the bq2010 increments NAC at a rate proportional to V_{SRO} and, if enabled, activates an LED display if the rate is equivalent to V_{SRO} > 4mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2010 determines charge activity sustained at a continuous rate equivalent to $V_{SRO} > V_{SRQ}$. A valid charge equates to sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V_{SRO} ($V_{SR} + V_{OS}$) falls below V_{SRQ}. V_{SRQ} is a programmable threshold as described in the Digital Magnitude Filter section. The default value for V_{SRQ} is 375µV.

Discharge Counting

The compensation factors during discharge are:

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.0 + (0.05 * N)$$

Where N = Number of 10°C steps below 10°C and $-150\text{mV} < V_{SR} < 0$.

For example:

T > 10°C : Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.0 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.0 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.0 becomes 1.15)

-20°C < T < -30°C: N = 4 (i.e., 1.0 becomes 1.20)

Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of $\frac{1}{64} * \text{NAC}$, $\frac{1}{47} * \text{NAC}$ per day, or disabled. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from

Table 5. bq2010 Current-Sensing Errors

Symbol	Parameter	Typical	Maximum	Units	Notes
V_{OS}	Offset referred to V_{SR}	± 50	± 150	µV	$\overline{DISP}$ = V_{CC}.
INL	Integrated non-linearity error	± 2	± 4	%	Add 0.1% per °C above or below 25°C and 1% per volt above or below 4.25V.
INR	Integrated non-repeatability error	± 1	± 2	%	Measurement repeatability given similar operating conditions.

the bq2010 should be pulled up by the host system or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2010. The command directs the bq2010 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2010 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2010. A BREAK is detected when the DQ pin is driven to a logic-low state for a time, t_B or greater. The DQ pin should then be returned to its normal ready-high logic state for a time, t_{BR}. The bq2010 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2010 taking the DQ pin to a logic-low state for a period, $t_{STRH,B}$. The next section is the actual data transmission, where the data should be valid by a period, t_{DSU}, after the negative edge used to start communication. The data should be held for a period, t_{DV}, to allow the host or bq2010 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period, t_{SSU}, after the negative edge used to start communication. The final logic-high state should be held until a period, t_{SV}, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2010 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2010 NAC register.

bq2010 Registers

The bq2010 command and status registers are listed in Table 6 and described below.

Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2010. The CMDR register contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command register is used to select whether the received command is for a read or a write function.

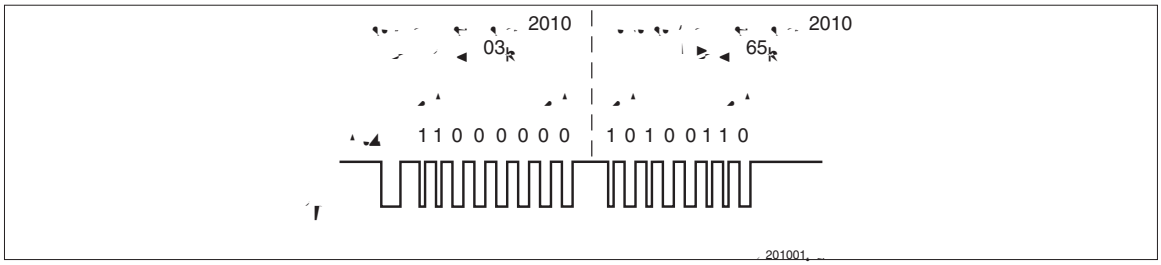


Figure 3. Typical Communication with the bq2010

Table 6. bq2010 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	Command register	00h	Write	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	Primary status flags register	01h	Read	CHGS	BRP	BRM	CI	VDQ	n/u	EDV1	EDVF
TMPGG	Temperature and gas gauge register	02h	Read	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	Nominal available charge high byte register	03h	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	Nominal available charge low byte register	17h	Read	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	Battery identification register	04h	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	Last measured discharge register	05h	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	Secondary status flags register	06h	Read	CR	DR2	DR1	DR0	n/u	n/u	n/u	OVLD
PPD	Program pin pull-down register	07h	Read	n/u	n/u	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	Program pin pull-up register	08h	Read	n/u	n/u	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	Capacity inaccurate count register	09h	Read	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
DMF	Digital magnitude filter register	0ah	R/W	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
RST	Reset register	39h	Write	RST	0	0	0	0	0	0	0

n/u = not used

The W/$\overline{R}$ values are:

Where W/$\overline{R}$ is:

0 The bq2010 outputs the requested register contents specified by the address portion of CMDR.

1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2010 flags.

The [illegible] flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when $V_{SRO} > V_{SRQ}$. A V_{SRO} of less than V_{SRQ} or discharge activity clears CHGS.

The CHGS values are:

Where CHGS is:

0 Either discharge activity detected or $V_{SRO} < V_{SRQ}$

1 $V_{SRO} > V_{SRQ}$

The [illegible] flag (BRP) is asserted whenever the potential on the SB pin (relative to V_{SS}), V_{SB}, falls from above the maximum cell voltage, MCV (2.25V), or rises above 0.1V. The BRP flag is also set when the bq2010 is reset (see the RST register description). BRP is reset when either a valid charge action increments NAC.3(flagrim2.6-97lag) (to)gAgtoThses BRPon inc

fro1bq2010bq2010aeite CHGS values

Where 72.1248 2.4(is:) T 1.3is

The [illegible] flag (VDQ) is asserted when the bq2010 is discharged from NAC=LMD. The flag remains set until either LMD is updated or one of three actions that can clear VDQ occurs:

- The self-discharge count register (SDCR) has exceeded the maximum acceptable value (4096 counts) for an LMD update.
- A valid charge action sustained at $V_{SRO} > V_{SRQ}$ for at least 256 NAC counts.
- The EDV1 flag was set at a temperature below 0°C

The VDQ values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

Where VDQ is:

0 SDCR ≥ 4096, subsequent valid charge action detected, or EDV1 is asserted with the temperature less than 0°C

1 On first discharge after NAC = LMD

The [illegible] flag (EDV1) warns the user that the battery is almost empty. The first segment pin, SEG_1, is modulated at a 4Hz rate if the display is enabled once EDV1 is asserted, which should warn the user that loss of battery power is imminent. The EDV1 flag is latched until a valid charge has been detected.

The EDV1 values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

Where EDV1 is:

0 Valid charge action detected, $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ providing that OVLD=0 (see FLGS2 register description)

The [illegible] flag (EDVF) is used to warn that battery power is at a failure condition. All segment drivers are turned off. The EDVF flag is latched until a valid charge has been detected. The EMPTY pin is also forced to a high-impedance state on assertion of EDVF. The host system may pull EMPTY high, which may be used to disable circuitry to prevent deep-discharge of the battery.

The EDVF values are:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	EDVF

Where EDVF is:

0 Valid charge action detected, $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ providing that OVLD=0 (see FLGS2 register description)

Temperature and Gas Gauge Register (TMPGG)

The read-only TMPGG register (address=02h) contains two data fields. The first field contains the battery temperature. The second field contains the available charge from the battery.

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

The bq2010 contains an internal temperature sensor. The temperature is used to set charge and discharge efficiency factors as well as to adjust the self-discharge coefficient.

The temperature register contents may be translated as shown below.

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30°C
0	0	0	1	-30°C < T < -20°C
0	0	1	0	-20°C < T < -10°C
0	0	1	1	-10°C < T < 0°C
0	1	0	0	0°C < T < 10°C
0	1	0	1	10°C < T < 20°C
0	1	1	0	20°C < T < 30°C
0	1	1	1	30°C < T < 40°C
1	0	0	0	40°C < T < 50°C
1	0	0	1	50°C < T < 60°C
1	0	1	0	60°C < T < 70°C
1	0	1	1	70°C < T < 80°C
1	1	0	0	T > 80°C

The bq2010 calculates the available charge as a function of NAC, temperature, and a full reference, either LMD or PFC. The results of the calculation are available via the display port or the gas gauge field of the TMPGG register. The register is used to give available capacity in $\frac{1}{16}$ increments from 0 to $\frac{15}{16}$.

The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

The adjustment between > 0°C and -20°C < T < 0°C has a 10°C hysteresis.

Nominal Available Charge Registers (NACH/NACL)

The read/write NACH high-byte register (address=03h) and the read-only NACL low-byte register (address=17h) are the main gas gauging register for the bq2010. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, if $PROG_6$ = Z or low, NACH and NACL are cleared to 0; if $PROG_6$ = high, NACH = PFC and NACL = 0. When the bq2010 detects a valid charge, NACL resets to 0. *Writing to the NAC registers affects the available charge counts and, therefore, affects the bq2010 gas gauge operation. Do not write the NAC registers to a value greater than LMD.*

Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V_{CC} is greater than 2V. The contents of BATID have no effect on the operation of the bq2010. There is no default setting for this register.

Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2010 uses as a measured full reference. The bq2010 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2010 updates the capacity of the battery. LMD is set to PFC during a bq2010 reset.

Secondary Status Flags Register (FLGS2)

The read-onlyrera4(thr)-2) thrhat tthr.

DR2–0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V_{SS}. The rate at which this measurement is made varies with device activity.

Program Pin Pull-Down Register (PPD)

The read-only PPD register (address=07h) contains some of the programming pin information for the bq2010. The segment drivers, $SEG_{1–6}$, have a corresponding PPD register location, $PPD_{1–6}$. A given location is set if a pull-down resistor has been detected on its corresponding segment driver. For example, if SEG_1 and SEG_4 have pull-down resistors, the contents of PPD are xx001001.

PPD/PPU Bits							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
-	-	PPU_6	PPU_5	PPU_4	PPU_3	PPU_2	PPU_1
-	-	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

The read-only PPU register (address=08h) contains the rest of the programming pin information for the bq2010. The segment drivers, $SEG_{1–6}$, have a corresponding PPU register location, $PPU_{1–6}$. A given location is set if a pull-up resistor has been detected on its corresponding segment driver. For example, if SEG_3 and SEG_6 have pull-up resistors, the contents of PPU are xx100100.

Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2010 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV1=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. When NAC > 0.94 * LMD, however, the CPI register increments on the first valid charge; CPI does not increment again for a valid charge until NAC < 0.94 * LMD. This prevents continuous trickle charging from incrementing CPI if self-discharge decrements NAC. The CPI register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. The CPI register is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

Digital Magnitude Filter (DMF)

The read-write DMF register (address = 0ah) provides the system with a means to change the default settings of the digital magnitude filter. By writing different values into this register, the limits of V_{SRD} and V_{SRQ} can be adjusted.

Care should be taken when writing to this register. A V_{SRD} and V_{SRQ} below the specified V_{OS} may adversely affect the accuracy of the bq2010. Refer to Table 4 for recommended settings for the DMF register.

Reset Register (RST)

The reset register (address=39h) provides the means to perform a software-controlled reset of the device. By writing the RST register contents from 00h to 80h, a bq2010 reset is performed. *Setting any bit other than the most-significant bit of the RST register is [illegible] and results in improper operation of the bq2010.*

Resetting the bq2010 sets the following:

- LMD = PFC
- CPI, VDQ, NACH, and NACL = 0
- CI and BRP = 1

NACH = PFC when $PROG_6$ = H. Self-discharge is disabled when $PROG_5$ = H

Display

The bq2010 can directly display capacity information using low-power LEDs. If LEDs are used, the program pins should be resistively tied to V_{CC} or V_{SS} for a program high or program low, respectively.

The bq2010 displays the battery charge state in either absolute or relative mode. In relative mode, the battery charge is represented as a percentage of the LMD. Each LED segment represents 20% of the LMD. The sixth segment, SEG_6, is not used.

In absolute mode, each segment represents a fixed amount of charge, based on the initial PFC. In absolute mode, each segment represents 20% of the PFC, with SEG_6 representing "overfull" (charge above the PFC). As the battery wears out over time, it is possible for the LMD to be below the initial PFC. In this case, all of the LEDs may not turn on in absolute mode, representing the reduction in the actual battery capacity.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. The temperature adjustments are detailed in the TMPGG register description.

When $\overline{DISP}$ is tied to V_{CC}, the $SEG_{1–6}$ outputs are inactive. When $\overline{DISP}$ is left floating, the display becomes active

whenever the NAC registers are counting at a rate equivalent to $|V_{SRO}| \geq 4mV$. When pulled low, the segment outputs become active immediately. A capacitor tied to $\overline{DISP}$ allows the display to remain active for a short period of time after activation by a push-button switch.

The segment outputs are modulated as two banks of three, with segments 1, 3, and 5 alternating with segments 2, 4, and 6. The segment outputs are modulated at approximately 100Hz with each segment bank active for 30% of the period.

SEG_1 blinks at a 4Hz rate whenever V_{SB} has been detected to be below V_{EDV1} (EDV1 = 1), indicating a low-battery condition. V_{SB} below V_{EDVF} (EDVF = 1) disables the display output.

Microregulator

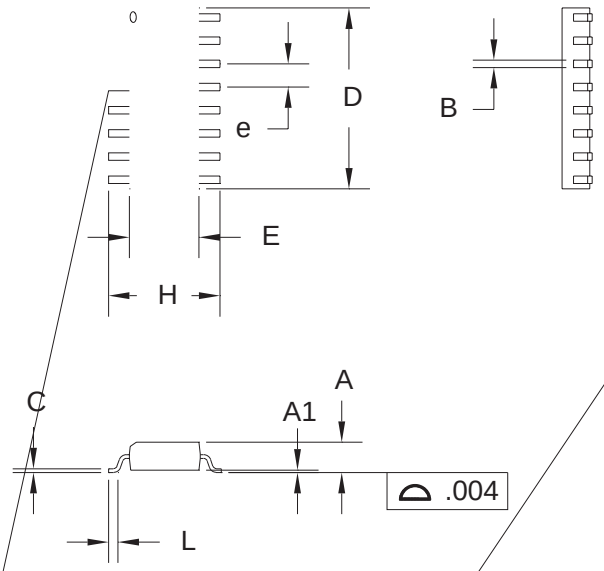
The bq2010 can operate directly from 3 or 4 cells. To fa-

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	3.0	4.25	6.5	V	V_{CC} excursion from < 2.0V to ≥ 3.0V initializes the unit.
V_{REF}	Reference at 25°C	5.7	6.0	6.3	V	I_{REF} = 5µA
	Reference at -40°C to +85°C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	Reference input impedance	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	Normal operation	-	90	135	µA	V_{CC} = 3.0V, DQ = 0
		-	120	180	µA	V_{CC} = 4.25V, DQ = 0
		-	170	250	µA	V_{CC} = 6.5V, DQ = 0
V_{SB}	Battery input	0	-	V_{CC}	V	
R_{SBmax}	SB input impedance	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$ input leakage	-	-	5	µA	V_{DISP} = V_{SS}
I_{LCOM}	LCOM input leakage	-0.2	-	0.2	µA	$\overline{DISP}$ = V_{CC}
R_{DQ}	Internal pulldown	500	-	-	KΩ	
V_{SR}	Sense resistor input	-0.3	-	2.0	V	V_{SR} < V_{SS} = discharge; V_{SR} > V_{SS} = charge
R_{SR}	SR input impedance	10	-	-	MΩ	-200mV < V_{SR} < V_{CC}
V_{IH}	Logic input high	V_{CC} - 0.2	-	-	V	$PROG_1$–$PROG_6$
V_{IL}	Logic input low	-	-	V_{SS} + 0.2	V	$PROG_1$–$PROG_6$
V_{IZ}	Logic input Z	float	-	float	V	$PROG_1$–$PROG_6$
V_{OLSL}	SEG_X output low, low V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75mA SEG_1–SEG_6
V_{OLSH}	SEG_X output low, high V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0mA SEG_1–SEG_6
V_{OHLCL}	LCOM output high, low V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25mA
V_{OHLCH}	LCOM output high, high V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0mA
I_{IH}	$PROG_{1-6}$ input high current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{IL}	$PROG_{1-6}$ input low current	-	1.2	-	µA	V_{PROG} = V_{CC}/2
I_{OHLCOM}	LCOM source current	-33	-	-	mA	At V_{OHLCH} = V_{CC} - 0.6V
I_{OLS}	SEG_X sink current	-	-	11.0	mA	At V_{OLSH} = 0.4V
I_{OL}	Open-drain sink current	-	-	5.0	mA	At V_{OL} = V_{SS} + 0.3V DQ, EMPTY
V_{OL}	Open-drain output low	-	-	0.5	V	I_{OL} ≤ 5mA, DQ, EMPTY
V_{IHDQ}	DQ input high	2.5	-	-	V	DQ
V_{ILDQ}	DQ input low	-	-	0.8	V	DQ
R_{PROG}	Soft pull-up or pull-down resistor value (for programming)	-	-	200	KΩ	$PROG_1$–$PROG_6$
R_{FLOAT}	Float state external impedance	Kva9875 TD()Tj (tor)M2 1 Tf2.1728 0.943 TD(PRO4)Tj6 0 0 6 429.2966 0895 TD63Tm(1)Tj7.5				

Serial Communication Timing Specification ($T_A = T_{OPR}$)

16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

Dimension	Minimum	Maximum
=	0.060	0.0 0
= 1	0.004	0.010
	0.013	0.020
	0.00	0.010
	0.3 5	0.400
	0.150	0.160
	0.045	0.055
	0.225	0.245
	0.015	0.035

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	4		≤ -150 ≤ -250
3	6	1, 5	5 5
3	,		5
3	11		64 2010
3	13		
3	13		-150 -250

Notes: 1 2 *1995 Data Book*.
3 1 5 1 4 .

Ordering Information

bq2010

Temperature Range:
(0 + 0)

Package Option:
16-

Device:
2010

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ2010SN-D107								

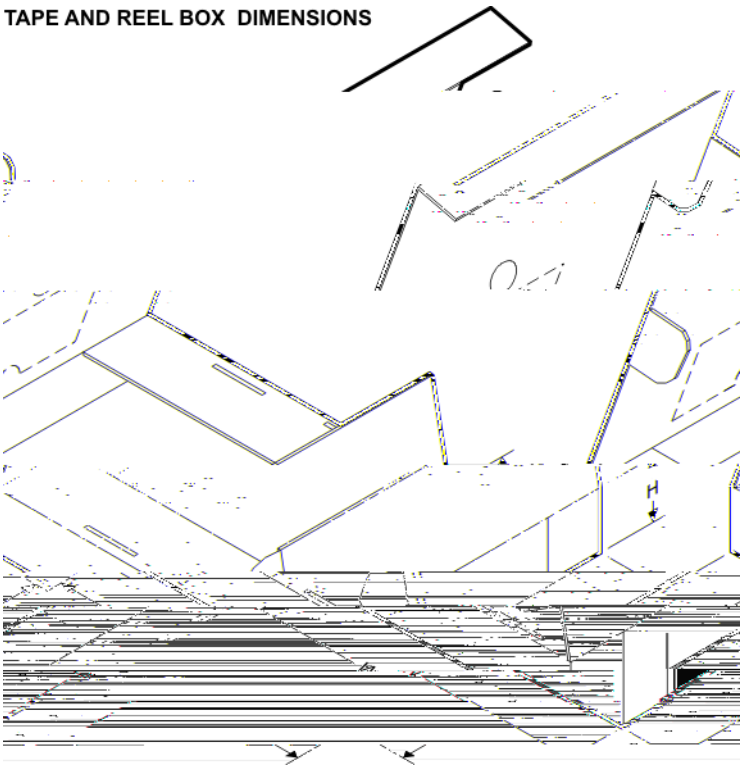
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2010SN-D107TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

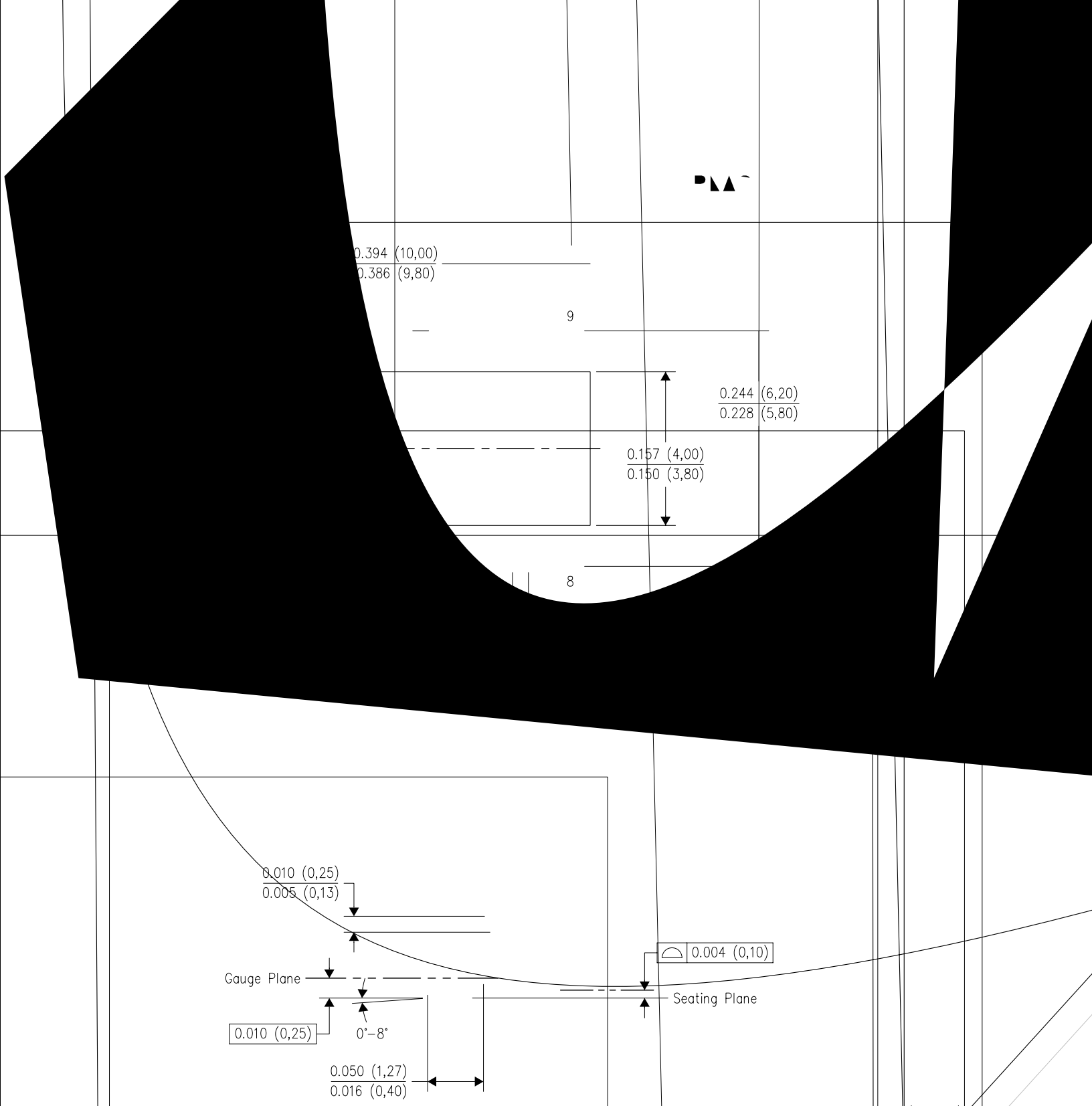
PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2010SN-D107TR	SOIC	D	16	2500	367.0	367.0	38.0



4040047-6/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate bur
ce interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

C. Publication IPC–735

D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.

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