UNITROD

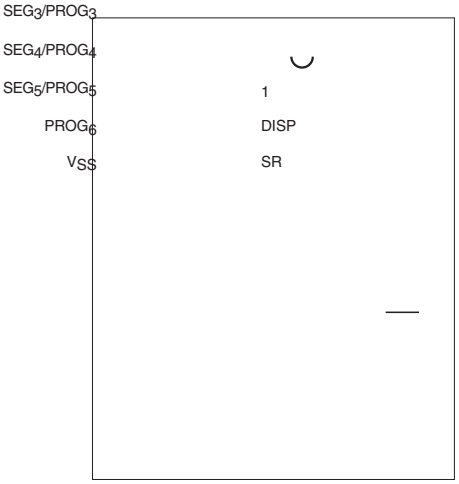
Features

- C
  - L L
- D
  - 120µA
  - S ½ PCB
- I
  - D LED
- M
- S
- 16- SOIC

General Description

T 2050 L I P G IC . T IC . C . B N LED . T 2050 . T ( ). T 2050 T 2050 (V_{BAT} > 3V). W REF . I ID, . T . T 2050 .

Pin Connections



Pin Names

LCOM	LED common output	REF	Voltage reference output
$SEG_1/PROG_1$	LED segment 1/ program 1 input	N/C	No connect
$SEG_2/PROG_2$	LED segment 2/ program 2 input	DQ	Serial communications input/output
$SEG_3/PROG_3$	LED segment 3/ program 3 input	RBI	Register backup input
$SEG_4/PROG_4$	LED segment 4/ program 4 input	SB	Battery sense input
$SEG_5/PROG_5$	LED segment 5/ program 5 input	$\overline{DISP}$	Display control input
$PROG_6$	Program 6 input	SR	Sense resistor input
		V_{CC}	3.0–6.5V
		V_{SS}	System ground

Pin Descriptions

LCOM **LED**

O - V_{CC} LED . T - LCOM -

EG1 **LED** (-
EG5 P OG1P OG 6)

E LED LCOM.

P OG1 **P** (- **EG1 EG 2)**
P OG2

T (PFC) - T 2.

P OG3 **P** (-
P OG4 **EG3 EG 4)**

T - T 2.

P OG5 - (- **EG5)**

T - T 1.

P OG6 **C/**

T - T 1.

N/C **N**

(-

T (V_{SR}) - R_S - . T SR - . V_{SR} < V_{SS} , V_{SR} > V_{SS} . T , V_{SRO}, 2050 V_{SR} + V_{OS} .

DI P **D**

DISP LED . DISP V_{CC} PROG_X - V_{CC} - V_{SS} . DISP LED DISP . S T 1.

B

T (EDV) , -

BI

T 2050 V_{CC} ≤ 3V. A RBI.

DQ **I/O**

T .

EF

REF -

CC

G

Functional Description

General Operation

T 2050 . T 2050 / . T . T . T

F 1

Voltage Thresholds

I [illegible] V_{SR} [illegible] /
[illegible] 2050 [illegible]
[illegible] SB [illegible] . T [illegible]
[illegible] :

$$\frac{RB1}{RB2} = 2N - 1$$

Gas Gauge Operation

T F 2 2050. T 2050 C

T , N A C (NAC), B NAC NAC DCR (D C R).

T D C R (DCR) I M D (LMD) T 2050

T P F C (PFC) T 2. U LMD , NAC . T

1. L M D (LMD) :

LMD . O V , LMD = PFC. D LMD D C R (DCR) EDV1. A DCR LMD . T LMD 100%

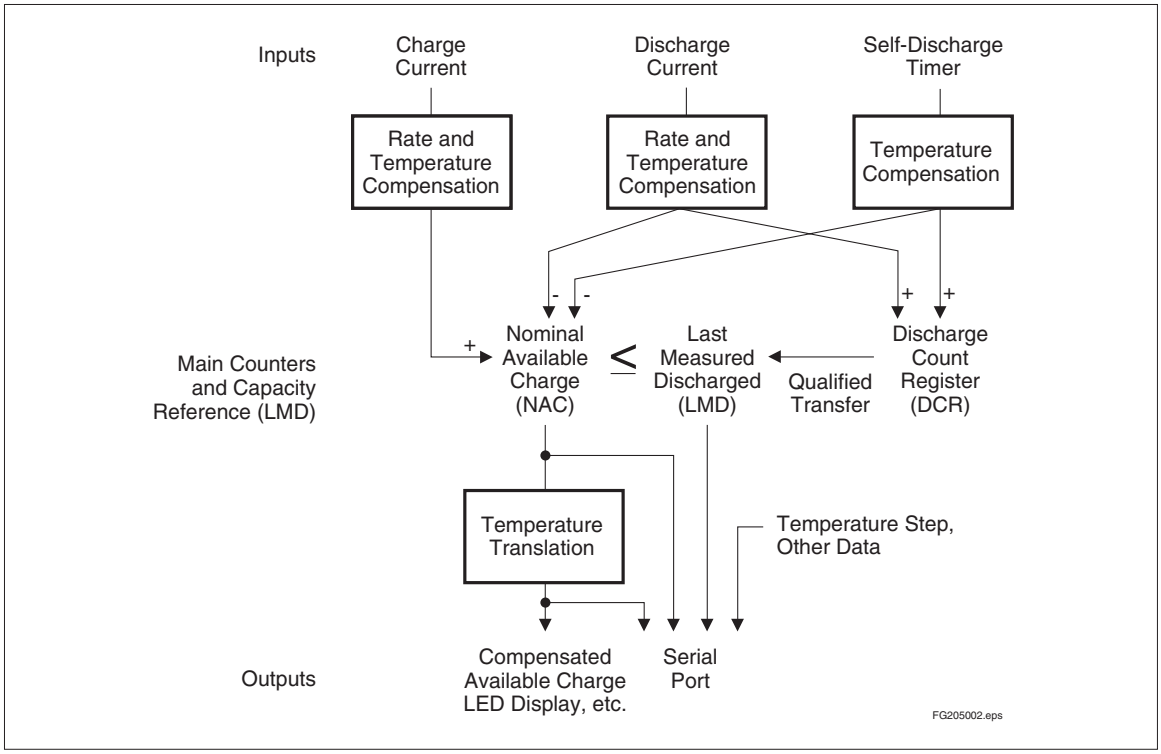


Figure 2. Operational Overview

2. P E C (PFC) :

T LMD PROG1 PROG4. T 2050
PFC T 2. T PFC
A :

H (A) * (Ω) =
PFC (V)

S PFC
2050 .

Example: Selecting a PFC Value

G :

S = 0.05Ω
N = 2
C = 1000 A , L -L
C = 50 A 1A
R
S
S = NAC/512 @ 25 C
V = 2.5 V 50 V
N = 3.6V

T :

1000 A * 0.05Ω = 50 V

Table 1. bq2050 Programming

Pin Connection	PROG5 Compensation/ Self-Discharge	PROG6 NAC on Reset	$\overline{\text{DISP}}$ Display State
H	T 4/D	PFC	LED
	T 4/ NAC/512	0	LED
L	T 3/ NAC/512	0	LED 4

N : PROG5 PROG6

Table 2. bq2050 Programmed Full Count mVh Selections

PROGx		Pro-grammed Full Count (PFC)	PROG4 = L			PROG4 = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	SCALE = 1/80	SCALE = 1/160	SCALE = 1/320	SCALE = 1/640	SCALE = 1/1280	SCALE = 1/2560	V /
H	H	49152	614	307	154	76.8	38.4	19.2	V
H		45056	563	282	141	70.4	35.2	17.6	V
H	L	40960	512	256	128	64.0	32.0	16.0	V
	H	36864	461	230	115	57.6	28.8	14.4	V
		33792	422	211	106	53.0	26.4	13.2	V
	L	30720	384	192	96.0	48.0	24.0	12.0	V
L	H	27648	346	173	86.4	43.2	21.6	10.8	V
L		25600	320	160	80.0	40.0	20.0	10.0	V
L	L	22528	282	141	70.4	35.2	17.6	8.8	V
VSR 2 / ( )			90	45	22.5	11.25	5.6	2.8	V

S :

PFC = 30720 48 V
$PROG_1$ =
$PROG_2$ =
$PROG_3$ =
$PROG_4$ =
$PROG_5$ =
$PROG_6$ =

T 48 V (960 A) 2050 – EDV1.

3. **N A C/ (NAC):**

NAC LMD 0. NAC 0 EDV1. T , NAC NAC = LMD.

4. **D C (DC):**

T DCR NAC NAC 0. P NAC = 0 ( ), DCR. A NAC = 0, DCR. T DCR 0 NAC = LMD. T DCR FFFF .

T DCR LMD V_{EDV1} :

N (256 NAC , $V_{SRO} > V_{SRQ}$) NAC = LMD EDV1 .

T 4096 (8% 18% PFC, PFC).

T ≥ 0 C EDV1 .

T (VDQ) LMD .

5. **A E (AE):**

SAE . SAE W :

$$E(W) = (SAEH * 256 + SAEL) * \frac{2.4 * SCALE * (R_{B1} + R_{B2})}{R_S * R_{B2}}$$

R_{B1}, R_{B2} R_S SCALE T 2. SAEH SAEL DQ.

6. **C / A C/ (CAC)**

CAC NAC,

Charge Counting

C V_{SR} I 2050 NAC V_{SR} , LED . C NAC.

T 2050 $V_{SRO} > V_{SRQ}$. A 256 NAC . O V_{SRO} (V

Table 3A. Graphite Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
< 0.5C	1.00	100%
≥ 0.5C	1.05	95%

Table 3B. Graphite Anode

Temperature	Temperature Compensation Factor	Efficiency
≥ 10° C	1.00	100%
0° C – 10° C	1.10	90%
-10° C – 0° C	1.35	74%
≤ -10° C	2.50	40%

Table 4A. Coke Anode

Approximate Discharge Rate	Discharge Compensation Factor	Efficiency
<0.5C	1.00	100%
≥ 0.5C	1.15	86%

Table 4B. Coke Anode

Temperature	Temperature Compensation Factor	Efficiency
≥ 10° C	1.00	100%
0° C – 10° C	1.25	80%
-10° C – 0° C	2.00	50%
≤ -10° C	8.00	12%

Charge Compensation

T 2050 NAC :

Temperature	Temperature Compensation Factor	Efficiency
< 10° C	0.95	95%
≥ 10° C	1.00	100%

T L-I

Self-Discharge Compensation

T ⅟512 * NAC . T 20° C 30° C . T 8 < 10° C > 70° C, 10° C). S T 5 :

Table 5. Self-Discharge Compensation

Temperature Range	Typical Rate PROG5 = Z or L
< 10° C	NAC/2048
10° 20° C	NAC/1024
20° 30° C	NAC/512
30° 40° C	NAC/256
40° 50° C	NAC/128
50° 60° C	NAC/64
60° 70° C	NAC/32
> 70° C	NAC/16

S PROG5 = H.

Digital Magnitude Filter

T 2050 . T 2050 200µV VSRD 210µV VSRQ.

Error Summary

Capacity Inaccurate

T LMD . O LMD . T LMD (DCR 7). T LMD . A .

A C I (CPI) (NAC; CPI) LMD DCR. T 255. T (CI) LMD 64 .

Current-Sensing Error

T 5 V_{SRO}. A NAC V_{SRO} V_{SRQ} V_{SRD}.

Communicating With the bq2050

T 2050 (DQ) . A 2050 . B . T DQ 2050 .

T 2050. T 2050 .

T . C 333 / . T . T . D 2050 .

I C_{CB} > 6 2050 BREAK . A BREAK DQ .

bq2050 Registers

T 2050
T 7

Command Register (CMDR)

Table 7. bq2050 Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	C	00	W	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	P	01	R	CHGS	BRP	/,	CI	VDQ	/,	EDV1	EDVF
TMP	T	02	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	N	03	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	N	17	R	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	B	04	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	L	05	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	S	06	R	/,	DR2	DR1	DR0	/,	/,	/,	OVLD
PPD	P	07	R	/,	/,	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	P	08	R	/,	/,	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	C	09	R	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
VSB	B	0B	R	VSB7	VSB6	VSB5	VSB4	VSB3	VSB2	VSB1	VSB0
VTS	E	0C	R/W	VTS7	VTS6	VTS5	VTS4	VTS3	VTS2	VTS1	VTS0
CACH	C	0D	R	CACH7	CACH6	CACH5	CACH4	CACH3	CACH2	CACH1	CACH0
CACL	C	0E	R	CACL7	CACL6	CACL5	CACL4	CACL3	CACL2	CACL1	CACL0
SAEH	S	0F	R	SAEH7	SAEH6	SAEH5	SAEH4	SAEH3	SAEH2	SAEH1	SAEH0
SAEL	S	10	R	SAEL7	SAEL6	SAEL5	SAEL4	SAEL3	SAEL2	SAEL1	SAEL0
RST	R	39	W	RST	0	0	0	0	0	0	0

N e : /, =

T ***capacity inaccurate*** (CI)
LMD . T CI
64 LMD
2050 . T
LMD .

T CI :

W CI :

0 W LMD -

1 A 64 -
LMD 2050

T ***valid discharge*** (VDQ)

Table 7. Temperature Register

TMP3	TMP2	TMP1	TMP0	Temperature
0	0	0	0	T < -30 C
0	0	0	1	-30 C < T < -20 C
0	0	1	0	-20 C < T < -10 C
0	0	1	1	-10 C < T < 0 C
0	1	0	0	0 C < T < 10 C
0	1	0	1	10 C < T < 20 C
0	1	1	0	20 C < T < 30 C
0	1	1	1	30 C < T < 40 C
1	0	0	0	40 C < T < 50 C
1	0	0	1	50 C < T < 60 C
1	0	1	0	60 C < T < 70 C
1	0	1	1	70 C < T < 80 C
1	1	0	0	T > 80 C

TMPGG Gas Gauge Bits							
7	6	5	4	3	2	1	0
-	-	-	-	GG3	GG2	GG1	GG0

Nominal Available Charge Registers (NACH/NACL)

T / NACH - (=03)
NACL - (=17)
2050. T NAC
. T
/
NAC. NACH NACL 0 -
2050 .

W *NAC a, c a a ab c a c a , a, c b 2050 a a a- . D NAC a a a a LMD.*

Battery Identification Register (BATID)

T / BATID (=04) -
. T BATID
V_{CC} 2V. T BATID
2050. T
.

Last Measured Discharge Register (LMD)

LMD / (=05)
2050 . T 2050
LMD
. I 2050
. LMD PFC
2050 .

Secondary Status Flags Register (FLGS2)

T - FLGS2 (=06)
2050 .

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	DR2	DR1	DR0	-	-	-	

T ***discharge rate*** , DR2 0, 6 4.

DR2	DR1	DR0	Discharge Rate
0	0	0	DRATE < 0.5C
0	0	1	0.5C ≤ DRATE < 2C
0	1	0	DRATE ≥ 2C (OVLD = 1)

T :

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	OVLD

T ***overload*** (OVLD)
2C . OVLD
0.5
2C. T -
.

Program Pin Pull-Down Register (PPD)

T - PPD (=07) -
2050. T
, $SEG_{1\ 6}$, PPD -
, $PPD_{1\ 6}$. A
. F SEG_1 SEG_4
PPD 001001.

Program Pin Pull-Up Register (PPU)

T - PPU (=08) -
2050. T
, $SEG_{1\ 6}$, PPU -
, $PPU_{1\ 6}$. A

. F SEG3 SEG6
PPU 100100.

Capacity Inaccurate Count Register (CPI)

T CPI =09)
LMD . B
2050
A (NAC=LMD)
(EDV1=1) LMD
0 C,
4096 .

T CPI
. W NAC > 0.94 ∗ LMD,
CPI ;
CPI
NAC < 0.94 ∗ LMC. T
CPI
NAC. T CPI 255
. W CPI
64, , CI,
FLGS1 . T CPI
LMD
CI .

Battery Voltage Register (VSB)

T
SB . T VSB
= 0B)
. V_{SB} =
2.4V ∗ (VSB/256).

Voltage Threshold Register (VTS)

T (EDV1
EDVF)
VTS =
0C). T / VTS EDV1
. EDVF 50 V EDV1. T
VTS A2 EDV1 =
1.52V EDVF = 1.47V. EDV1 = 2.4V ∗ (VTS/256).

Compensated Available Charge Registers (CACH/CACL)

T CACH = 0D)
CACL =
0E)
. CACH CACL
T 3A, 3B, 4A,
4B,
. T NAC
LMD
.

Scaled Available Energy Registers (SAEH/SAEL)

T SAEH = 0F)
SAEL =
10)
CAC

NAC . T CACH CACL .

W DISP V$_{CC}$, SEG1 5 . W DISP 2050 V$_{SRO}$ > V$_{SRQ}$. W ,± 0.5 .

T 1, 3, 5 2 4. T 100H 30% .

SEG$_1$ 4H V$_{SB}$ V$_{EDV1}$ (EDV1 = 1), . V$_{SB}$ V$_{EDVF}$ (EDVF = 1) .

Microregulator

T 2050 . A 2050 FET ; F 1.

DC Voltage Thresholds ($T_A = T_{OPR}$; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{EDVF}	F[illegible]	1.44	1.47	1.50	V	SB
V_{EDV1}	F[illegible]	1.49	1.52	1.55	V	SB
V_{SRO}	SR[illegible]	-300	-	2000	V	SR, $V_{SR} + V_{OS}$
V_{SRQ}	V[illegible]	210	-	-	µV	$V_{SR} + V_{OS}$ ([illegible])
V_{SRD}	V[illegible]	-	-	-200	µV	$V_{SR} + V_{OS}$ ([illegible])
V_{MCV}	M[illegible]	2.20	2.25	2.30	V	SB

DC Electrical Characteristics ($T_A = T_{OPR}$)

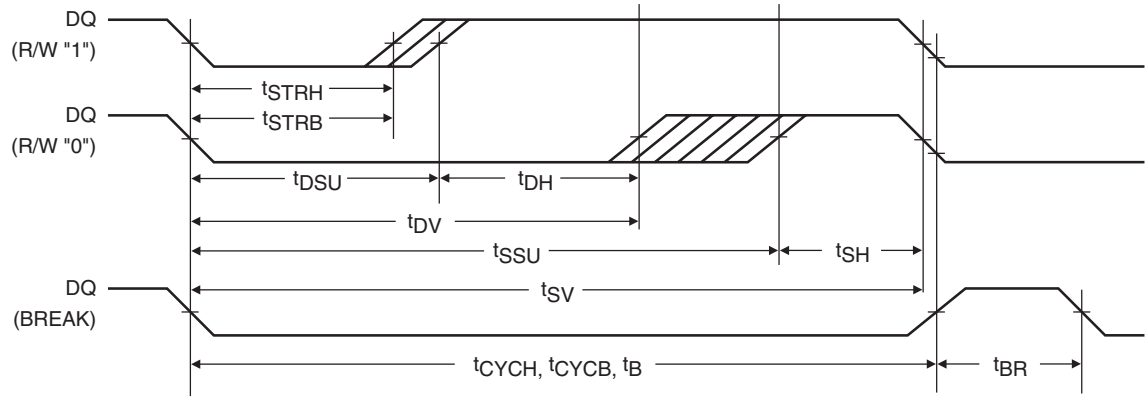
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	S[illegible]	3.0	4.25	6.5	V	V_{CC} [illegible] < 2.0V [illegible] ≥ 3.0V [illegible]
V_{OS}	O[illegible] V_{SR}	-	±50	±150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	R[illegible] 25 C	5.7	6.0	6.3	V	$I_{REF} = 5\mu A$

Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
tCYCH	C ... 2050	3	-	-		S...
tCYCB	C ... 2050 ...	3	-	6		
tSTRH	S... ... 2050	5	-	-		
tSTRB	S... ... 2050 ...	500	-	-	µ	
tDSU	D...	-	-	750	µ	
tDH	D...	750	-	-	µ	
tDV	D...	1.50	-	-		
tSSU	S...	-	-	2.25		
tSH	S...	700	-	-	µ	
tSV	S...	2.95	-	-		
tB	B...	3	-	-		
tBR	B...	1	-	-		

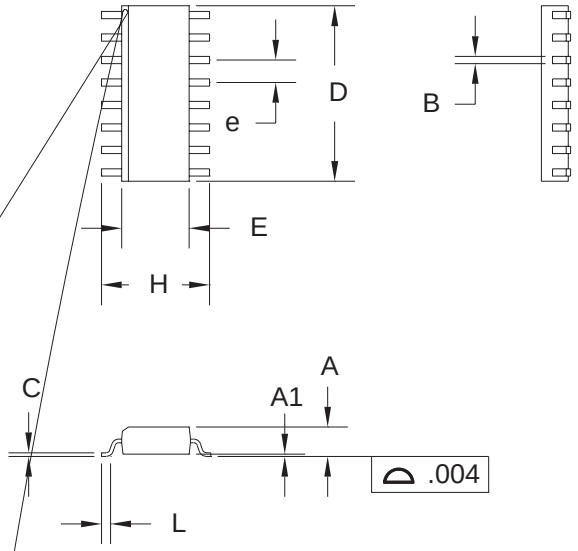
Note: T... DQ... V_{CC}... DQ...
DQ...

Serial Communication Timing



TD201002.eps

1 : ( )



1 : (0.150")

A	0.060	0.070	1.52	1.78
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.18	0.25
D	0.385	0.400	9.78	10.16
E	0.150	0.160	3.81	4.06
	0.045	0.055	1.14	1.40
H	0.225	0.245	5.72	6.22
L	0.015	0.035	0.38	0.89

1	4	C a , c +	W a : R b + , c a a I : R b , & C a , + , , RBI 15 .
1	11, 14	D -	
2	16	C a , a +	V EDVF: M , . a 1.45; M a . a 1.49 M , . , 1.44; M a . , 1.50 V EDV1: M , . a 1.50; M , . , 1.49
2	17	C a , a +	V CC: M , . a 2.5; M , . , 3.0
2	4, 11, 13, 14	R , ,	
2	9	M a , + V OS:	M a . a 150 M a . , 180

N e : C a , 1 = J , 1995 B c a , D c. 1994.
C a , 2 = S . 1996 C c a , J , 1995 B.

2050

Te e a e Ra e:
b a = C c a (-20 +70C)

Pac a e O :
SN = 16- a SOIC

De ce:
b 2040 Ga Ga I C W SMBI ac

7 9 19
7 5252
(97 2) 43 9 19
(97 2) 43 9 19 5

C 1996, U C a A . N a aa a b +c a
a , + U . U a c a , - +c + c .

U a + b - a +c c c b . N c - + - c+a (a , c ,) b U a a - .

U a + c a - + a + a + c a ca + + . I U c a + - + , + a + a - b - a U a ab - aa .

B c a a , a a U C a . P US.A.