Features

- C
- C
- D
  - 120µA
    (
  - S
    ½
    PCB
- I
  - D
    LED
- M
- S
-
- 16-
  SOIC

General Description

T 2012 G G IC

T IC

S N MH N C

C

B

T 2012

N

LED T)

T 2012

(

). T 2012

I

ID,

Pin Descriptions

LCOM **LED common output**

O - V$_{CC}$ LED . T

LCOM

SEG$_1$–SEG$_6$ **LED display segment outputs (dual function with PROG$_1$–PROG$_6$)**

E LED .
LCOM.

PROG$_1$–PROG$_2$ **Programmed full count selection inputs (dual function with SEG$_1$–SEG$_2$)**

T
(PFC)
T 2.

PROG$_3$ PROG$_4$ **Gas gauge rate selection inputs (dual function with SEG$_3$–SEG$_4$)**

T
T 2.

PROG$_5$ **Self-discharge rate selection (dual function with SEG$_5$)**

T
T 1.

PROG$_6$ **Display mode selection (dual function with SEG$_6$)**

T
T 1.

$\overline{CHG}$ **Charge control output**

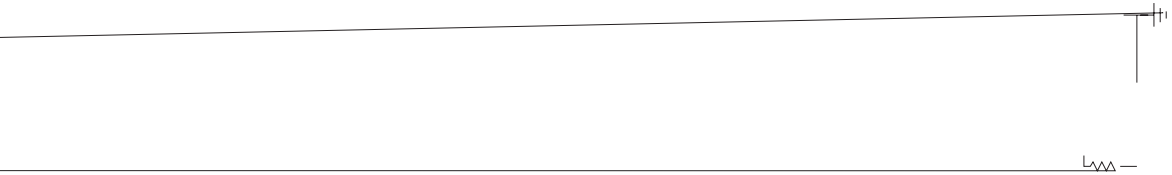
T W
C C

SR **Sense resistor input**

T (V$_{SR}$)
R$_S$
. T SR
. V$_{SR}$ < V$_{SS}$
V$_{SR}$ > V$_{SS}$. T
(V$_{SRO}$)
2012 V$_{SR}$ + V$_{OS}$ (T 5).

$\overline{DISP}$ **Display control input**

$\overline{DISP}$ LED . $\overline{DISP}$
V$_{CC}$ PROG$_X$



Voltage Thresholds

I V_SR /
2012
SB . T
/
:

$$\frac{RB_1}{RB_2} = N - 1$$

N , RB_1
, RB_2
. T (EDV)
(MCV). EDV
– MCV
.

T EDV 2012 :

EDV1 ( ) = 1.05V

EDVF ( ) = 0.95V

I V_{SB} EDV
V_{SB},

D 2012 V_{SR}
T
. R
EDV
$V_{SR} \leq -250$ V ½
$V_{SR} > -250$ V.

EMPTY Output

T EMPT
$V_{SB} < V_{EDF}$
. T 2012 V_{SB} V_{MCV},
2.25V. V_{SB} V_{MCV}

Reset

T 2012 V_{SB}
0.1V . V_{SB} 0.25V
2.25V . R
R R .

Temperature

T 2012
10 C -35 C +85 C. T -
T

10 C
:

Layout Considerations

T 2012
SR V_{SS} .

Gas Gauge Operation

T F 2 2012. T 2012 C , .

T , N A C (NAC), . B NAC , NAC DCR (D C R).

T D C R (DCR) I M D (LMD) T , 2012 .

T , (PFC) T 2. U LMD , NAC . T .

1. **Last Measured Discharge (LMD) or learned battery capacity:**

LMD . O (V_{CC}), LMD = PFC. D LMD D C R (DCR) EDV1. A DCR LMD . T LMD 100% .

2. **Programmed Full Count (PFC) or initial battery capacity:**

T LMD PROG$_1$ PROG$_4$. T PFC 100% . T 2012 PFC T 2. T PFC A :

B (A) *

Example: Selecting a PFC Value

G :

S = 0.1Ω
N = 6
O = 2200 A , N C
C = 50 A 2A
A
S
S = %64
V = 5 V 200 V

T :

2200 A ∗ 0.1Ω = 220 V

S :

PFC = 33792 211 V
PROG1 =
PROG2 =
PROG3 =
PROG4 =
PROG5 =
PROG6 =

T 211 V
(2110 A) 2012 – EDV1.

PROGx		Programmed Full Count (PFC)	PROG4 = L			PROG4 = Z			Units
1	2		PROG3 = H	PROG3 = Z	PROG3 = L	PROG3 = H	PROG3 = Z	PROG3 = L	
-	-	-	S = 1/80	S = 1/160	S = 1/320	S = 1/640	S = 1/1280	S = 1/2560	V /
H	H	49152	614	307	154	76.8	38.4	19.2	V
H		45056	563	282	141	70.4	35.2	17.6	V
H	L	40960	512	256	128	64.0	32.0	16.0	V
	H	36864	461	230	115	57.6	28.8	14.4	V
		33792	422	211	106	53.0	26.4	13.2	V
	L	30720	384	192	96.0	48.0	24.0	12.0	V
L	H	27648	346	173	86.4	43.2	21.6	10.8	V
L		25600	320	160	80.0	40.0	20.0	10.0	V
L	L	22528	282	141	70.4	35.2	17.6	8.8	V
V_{SR} 2 / ( )			90	45	22.5	11.25	5.56	2.8	V

3. Nominal Available Charge (NAC):

NAC
LMD
0. NAC 0
(PROG$_6$ =)
EDV1. NAC
PFC
PROG$_6$ = . T
, NAC NAC =
LMD.

4. Discharge Count Register (DCR):

T DCR
NAC
NAC
0. DCR
EDV1 . P NAC = 0 ( ),
DCR. A NAC = 0,
DCR. T DCR 0 NAC = LMD. T
DCR
FFFF .

T DCR LMD
V_{EDV1} :

N ( )
256 NAC ; $V_{SRO} > V_{SRQ}$)
NAC = LMD EDV1
.

T 4096
(8% 18% PFC,
PFC).

T ≥ 0 C EDV1
.

T (VDQ)
LMD .

Charge Counting

C
V_{SR} I ,
2012 NAC V_{SRO}
(V_{SR} + V_{OS}) , , LED
V_{SRO} > 4 V. C
NAC
.

T 2012
V_{SRO} > V_{SRQ}. A
256 NAC . O
V_{SRO} V_{SRQ}. V_{SRQ}
D
M F . T V_{SRQ}
375µV.

Charge Control

C $\overline{CHG}$ T
:

NAC < 0.94 * LMD
0.95V < V_{SB} < 2.25V
0 C < T < 50 C
BRM = 0

T ⅟16 (0.5
7.5)
:

NAC < LMD
0.95V < V_{SB} < 2.25V
T < 50 C
BRM = 0

T ⅟16 (0.5
7.5) 2- :

NAC = LMD
T < 50 C
0.95V < V_{SB} < 2.25V
BRM = 0

T :

NAC = LMD (2-)
T > 50 C
V_{SB} < 0.95V
V_{SB} > 2.25V
BRM = 1

T - (2) - -
0.8 * LMD (PROG$_6$ = L) 0.8 * PFC (PROG$_6$ = H).

Caution: The charge control output ($\overline{CHG}$) should be used with other forms of charge termination such as ΔT/forfor

Self-Discharge Estimation

T 2012 NAC
DCR
T
¼64 * NAC ¼47 * NAC
PROG5. T
20 30 C. T NAC
0.

Count Compensations

T 2012 NAC
≥2 / C
/
NAC / DCR. S
NAC DCR.

Charge Compensation

T P
≥ 2 NAC / (≥ 0.15C
0.32C PFC ; T 2). T
.

T
T

Discharge Compensation

C T
VSR. T
:

T
A
0.05 10 C 10 C.
C = 1.0 + (0.05 * N)

W N = N, 10 C 10 C
-150 V < VSR < 0.

F :
)
T > 10 C : N , N = 0
0 C < T < 10 C: N = 1 (., 1.0 1.05)
-10 C < T < 0 C: N = 2 (., 1.0 1.10)
-20 C < T < -10 C: N = 3 (., 1.0 1.15)
-20 C < T < -30 C: N = 4 (., 1.0 1.20)

Self-Discharge Compensation

T
¼64 * NAC ¼47 * NAC . T

Error Summary

Capacity Inaccurate

T LMD O LMD . T LMD (DCR). T LMD A .

A C I (CPI) (NAC; CPI) LMD DCR. T 255. T (CI) LMD 64 .

Current-Sensing Error

T 5 V_{SR}. A NAC V_{SRO} (V_{SR} + V_{OS}) V_{SRQ} V_{SRD}.

Communicating With the bq2012

T 2012 (DQ) A 2012 B . T DQ 2012 .

T , 2012.

T 2012)

T C 333

/ T)

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field 7(MSB)	6	5	4	3	2	1	0(LSB)
CMDR	C	00	W	W/$\overline{R}$	AD6	AD5	AD4	AD3	AD2	AD1	AD0
FLGS1	P	01	R	CHGS	BRP	BRM	CI	VDQ	$\overline{CHG}$	EDV1	EDVF
TMPGG	T	02	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	N	03	R/W	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	N	17	R	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	B	04	R/W	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	D	05	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	S	06	R	CR	DR2	DR1	DR0	/	/	/	OVLD
PPD	P	07	R	/	/	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PPU	P	08	R	/	/	PPU6	PPU5	PPU4	PPU3	PPU2	PPU1
CPI	C	09	R	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0

T ***battery removed*** (BRM) SB (V_{SS}) MCV 0.1V. T BRM BRM.

T BRM :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	BRM	-	-	-	-	-

W BRM :

0 $0.1V < V_{SB} < 2.25V$

1 $0.1 V > V_{SB}$ $V_{SB} > 2.25V$

T ***capacity inaccurate*** (CI) LMD . T CI 64 LMD 2012 . T LMD.

T CI :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	CI	-	-	-	-

W CI :

0 W LMD

1 A 64 LMD

T ***valid discharge*** (VDQ) 2012 NAC = LMD. T LMD VDQ :

- T (SDCR) (4096) LMD .
- A $V_{SRO} > V_{SRQ}$ 256 NAC .
- T EDV1 0 C

T VDQ :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	VDQ	-	-	-

W VDQ :

0 SDCR ≥ 4096, EDV1 0 C

1 O NAC = LMD

T ***charge control*** , $\overline{CHG}$, $\overline{CHG}$ (7 $\overline{CHG}$).

T $\overline{CHG}$:

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	$\overline{CHG}$	-	-

W $\overline{CHG}$:

0 W $\overline{CHG}$ 2012

1 W $\overline{CHG}$

T ***first end-of-discharge warning*** (EDV1) T , SEG_1, 4H EDV1 , T EDV1 .

T EDV1 :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	EDV1	-

W EDV1 :

0 V , $V_{SB} \geq 1.05V$

1 $V_{SB} < 1.05V$ OVLD=0 (FLGS2)

T ***final end-of-discharge warning*** (EDVF) A . T EDVF . T EMPT EDV1. T EMPT .

T EDVF :

W EDVF :

0 V , $V_{SB} \geq 0.95V$

1 $V_{SB} < 0.95V$ OVLD=0 (FLGS2)

Temperature and Gas Gauge Register (TMPGG)

T TMPGG (=02) T T

T 2012 T

T T 7.

T 2012 NAC, LMD PFC. T TMPGG T 1/16, 0 15/16.

T TMPGG A :

T > 0 C -20 C < T < 0 C 10 C

Nominal Available Charge Registers (NACH/NACL)

T / NACH (=03) NACL (=17) 2012. T NAC

T / NAC.

Digital Magnitude Filter (DMF)

T - DMF (= 0)
. B -
V_{SRD} V_{SRQ}

Note: C
. A V_{SRD} V_{SRQ} V_{OS} -
2012. R T
4 DMF .

Reset Register (RST)

T (=39) .
. B
RST 00 80 ,
2012 . *Setting any bit other than the most-significant bit of the RST register is* ***not allowed****, and results in improper operation of the bq2012.*

R 2012 :

- LMD = PFC
- CPI, VDQ, NACH, NACL = 0
- CI BRP = 1

Note: NACH = PFC $PROG_6$ = H.

Display

T 2012 LED . I LED
V_{CC} V_{SS} -
.

T 2012 .
I
LMD. B
LED 20% LMD. T
) .

I , PFC. I)
, 20% PFC,
–(-
PFC). A -
LMD PFC. I
LED .

T -
T
NAC . T -
TMPGG .

W DISP

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	R. ▼ ... V_{SS}	-0.3	7.0	V	
A ...	R. ▼ ... V_{SS}	-0.3	7.0	V	
REF	R. ▼ ... V_{SS}	-0.3	8.5	V	C. ... R1 (... F, ... 1) M, ... 100Ω ...
V_{SR}	R. ▼ ... V_{SS}	-0.3	7.0	V	SR, ▼ ... ▼ (... 2012▼ ... - ▼ ... ▼ ...).
T_{OPR}	O ... ▼ ... ▼ ... ▼ - ...	0	70	... C	C. ... ▼

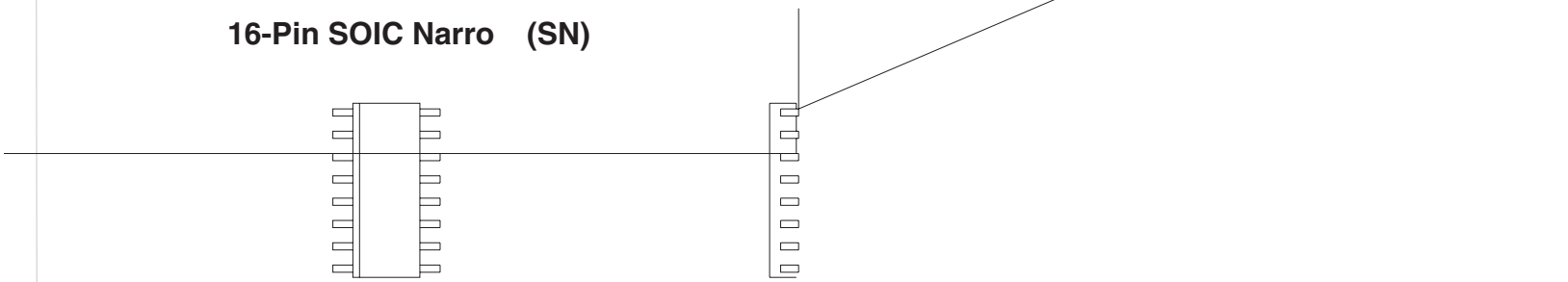
DC Electrical Characteristics ($T_A = T_{OPR}$)

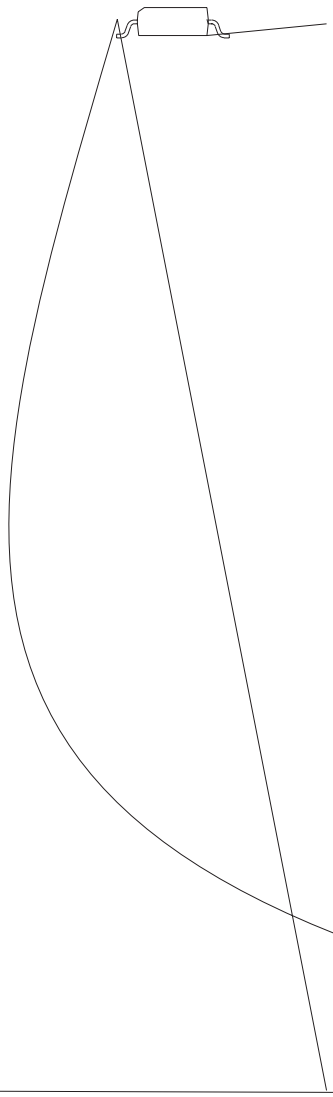
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	S	3.0	4.25	6.5	V	V_{CC} < 2.0V ≥ 3.0V
V_{OS}	O V_{SR}	-	±50	150	µV	$\overline{DISP} = V_{CC}$
V_{REF}	R 25 C	5.7	6.0	6.3	V	I_{REF} = 5µA
	R -40 C +85 C	4.5	-	7.5	V	I_{REF} = 5µA
R_{REF}	R	2.0	5.0	-	MΩ	V_{REF} = 3V
I_{CC}	N	-	90	135	µA	V_{CC} = 3.0V
		-	120	180	µA	V_{CC} = 4.25V
		-	170	250	µA	V_{CC} = 6.5V
V_{SB}	B	-	-	2.4	V	
R_{SB}	SB	10	-	-	MΩ	0 < V_{SB} < V_{CC}
I_{DISP}	$\overline{DISP}$	-	-	5	µA	$V_{DISP} = V_{SS}$
I_{LCOM}	LCOM	-0.2	-	0.2	µA	$\overline{DISP} = V_{CC}$
R_{DQ}	I	500	-	-	KΩ	
V_{SR}	S	-0.3	-	2.0	V	$V_{SR} < V_{SS}$ = ; $V_{SR} > V_{SS}$ =
R_{SR}	SR	10	-	-	MΩ	-200 V < V_{SR} < V_{CC}
V_{IH}	L	V_{CC} - 0.2	-	-	V	$PROG_1$ $PROG_6$
V_{IL}	L	-	-	V_{SS} + 0.2	V	$PROG_1$ $PROG_6$
V_I	L		-		V	$PROG_1$ $PROG_6$
V_{OLSL}	SEG V_{CC}	-	0.1	-	V	V_{CC} = 3V, I_{OLS} ≤ 1.75 A SEG_1 SEG_6
V_{OLSH}	SEG V_{CC}	-	0.4	-	V	V_{CC} = 6.5V, I_{OLS} ≤ 11.0 A SEG_1 SEG_6
V_{OHLCL}	LCOM V_{CC}	V_{CC} - 0.3	-	-	V	V_{CC} = 3V, I_{OHLCOM} = -5.25 A
V_{OHLCH}	LCOM V_{CC}	V_{CC} - 0.6	-	-	V	V_{CC} = 6.5V, I_{OHLCOM} = -33.0 A
I_{IH}	$PROG_{1-6}$	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{IL}	$PROG_{1-6}$	-	1.2	-	µA	$V_{PROG} = V_{CC}/2$
I_{OHLCOM}	LCOM	-33	-	-	A	A $V_{OHLCH} = V_{CC}$ - 0.6V
I_{OLS}	SEG	-	-	11.0	A	A V_{OLSH} = 0.4V
I_{OL}	O	-	-	5.0	A	A $V_{OL} = V_{SS}$ + 0.3V DQ, EMPT , $\overline{CHG}$
V_{OL}	O	-	-	0.5	V	I_{OL} ≤ 5 A, DQ, EMPT
V_{IHDQ}	DQ	2.5	-	-	V	DQ
V_{ILDQ}	DQ	-	-	0.8	V	DQ
R_{PROG}	S ( )	-	-	200	KΩ	$PROG_1$ $PROG_6$
R_{FLOAT}	F)	-	5	-	MΩ	$PROG_1$ $PROG_6$

Serial Communication Timing Specification

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
C CH	C 2012	3	-	-		S
C CB	C 2012	3	-	6		
STRH	S 2012	5	-	-		
STRB	S 2012	500	-	-	µ	
DSU	D	-	-	750	µ	
DH	D	750	-	-	µ	
DV						

16-Pin SOIC Narro (SN)





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ2012SN-D107	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ2012SN-D107G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ2012SN-D107TR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ2012SND107TRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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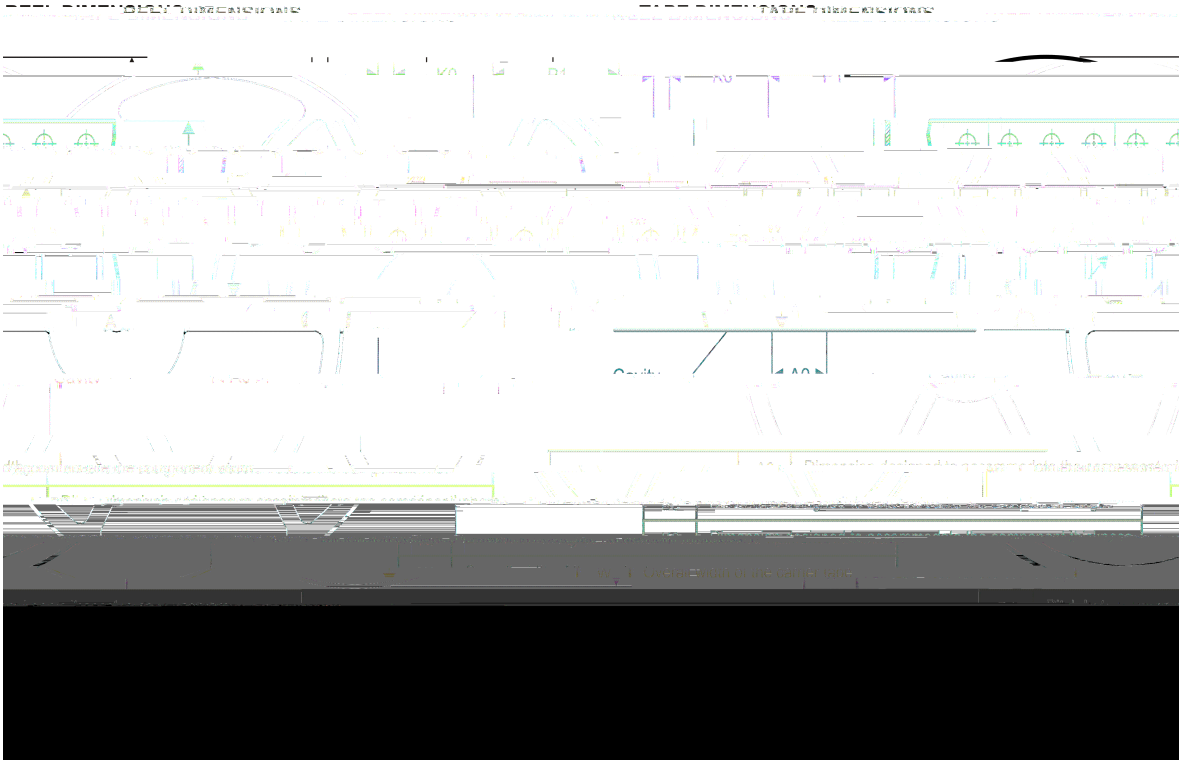
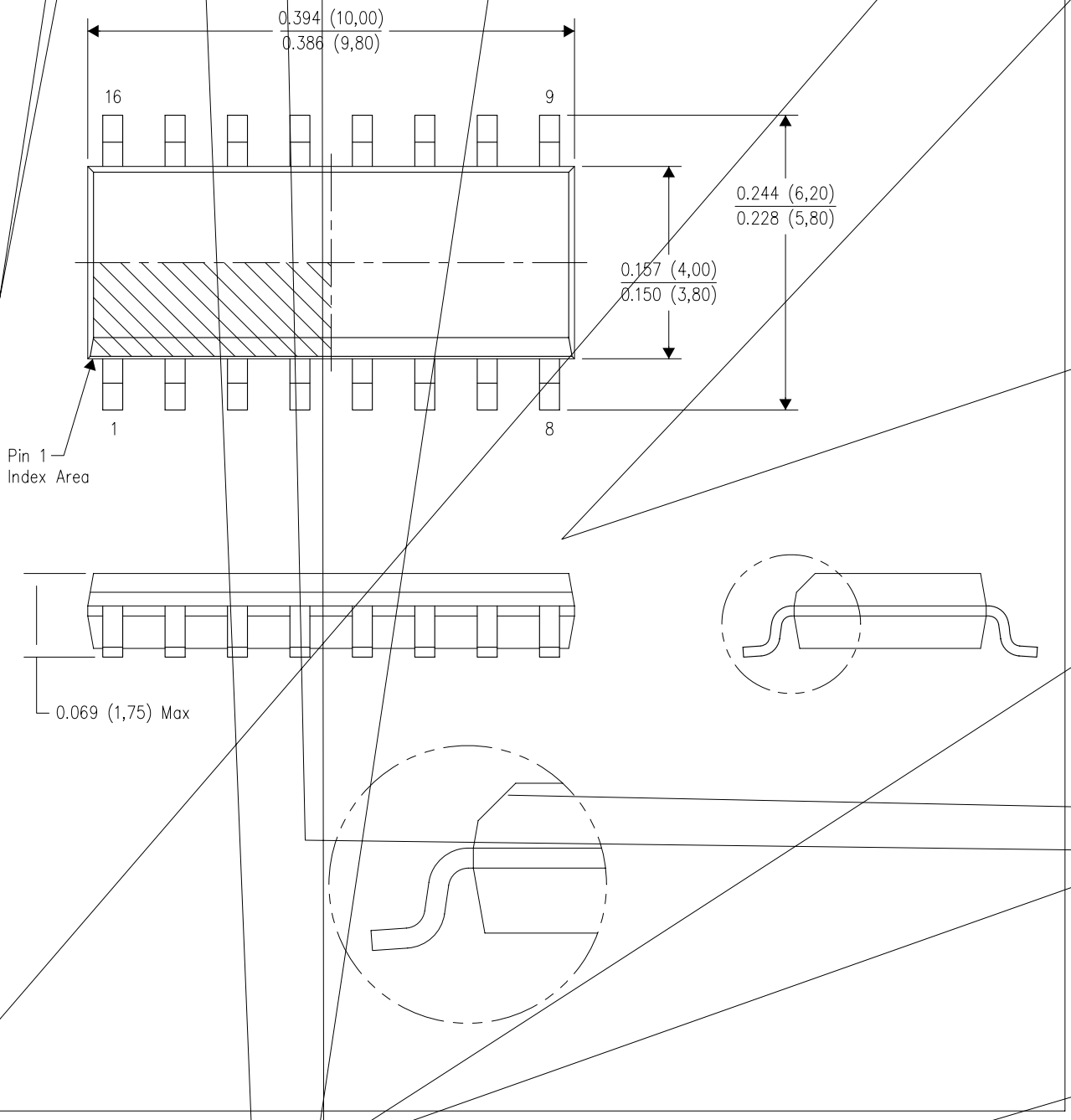
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2012SN-D107TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. rat include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall
D. ce interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 var

contact their board assembly site for stencil design recommendations. Re

=. Customers should contact their board fabrication site for solder mask tolerances between and around sign

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