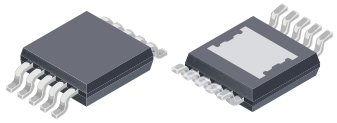
Full-Bridge DMOS PWM Motor Drivers

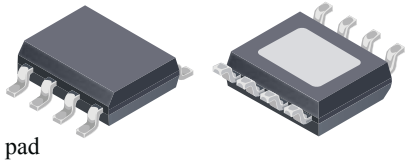
Features and Benefits

- Low $R_{DS(on)}$ outputs
- Overcurrent protection (OCP)
  - Motor short protection
  - Motor lead short to ground protection
  - Motor lead short to battery protection
- Low Power Standby mode
- Adjustable PWM current limit
- Synchronous rectification
- Internal undervoltage lockout (UVLO)
- Crossover-current protection
- Fault output (A4952 only)
- Selectable retry (A4952 only)

Packages:



10-pin MSOP
with exposed thermal pad
(LY package)



8-pin SOICN
with exposed thermal pad
(LJ package)

Not to scale

Description

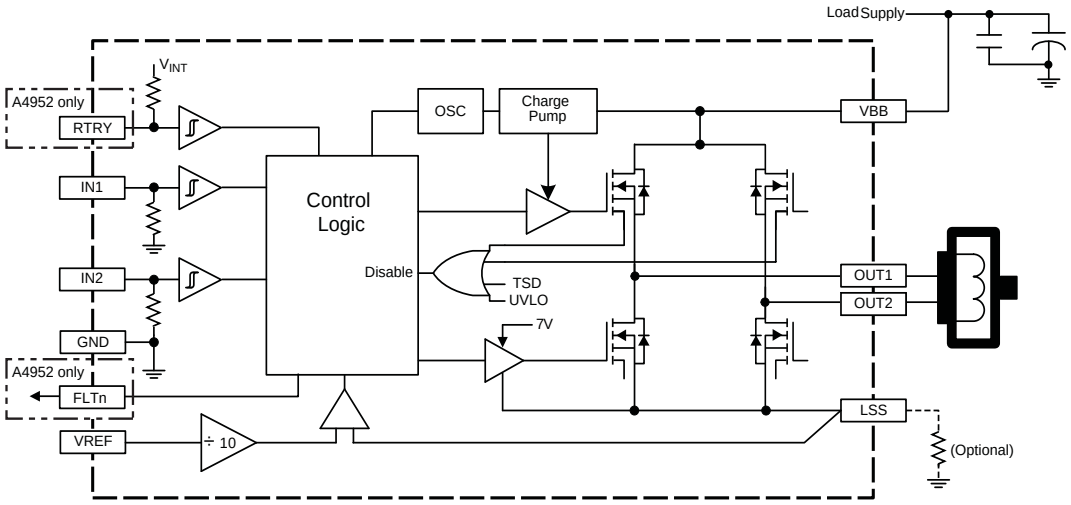
Designed for pulse width modulated (PWM) control of DC motors, the A4952 and A4953 are capable of peak output currents to ±2 A and operating voltages to 40 V.

Input terminals are provided for use in controlling the speed and direction of a DC motor with externally applied PWM control signals. Internal synchronous rectification control circuitry is provided to lower power dissipation during PWM operation.

Internal circuit protection includes overcurrent protection, motor lead short to ground or supply, thermal shutdown with hysteresis, undervoltage monitoring of V_{BB}, and crossover-current protection.

The A4952 is provided in a low-profile 10-pin MSOP package (suffix LY) and the A4953 is provided in a low-profile 8-pin SOICN package. Both packages have an exposed thermal pad, and are lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram



Selection Guide

Part Number	Packing
A4952ELYTR-T	4000 pieces per 13-in. reel
A4953ELJTR-T	3000 pieces per 13-in. reel

Absolute Maximum Ratings

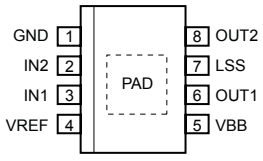
Characteristic	Symbol	Notes	Rating	Unit
Load Supply Voltage	V_{BB}		40	V
Logic I/O Voltage Range	V_{IN}		–0.3 to 6	V
FLTn Sink Current	I_{FLTN}		10	mA
V_{REF} Input Voltage Range	V_{REF}		–0.3 to 6	V
Sense Voltage (LSS pin)	V_S		–0.5 to 0.5	V
Motor Outputs Voltage	V_{OUT}		–2 to 42	V
Output Current	I_{OUT}	Duty cycle = 100%	2	A
Transient Output Current	i_{OUT}	T_W < 500 ns	6	A
Operating Temperature Range	T_A	Temperature Range E	–40 to 85	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature Range	T_{stg}		–55 to 150	°C

Thermal Characteristics may require derating at maximum conditions, see application information

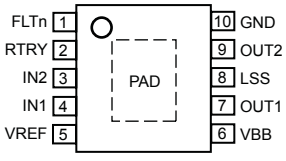
Characteristic	Symbol	Test Conditions*	Value	Unit
Package Thermal Resistance	$R_{\theta JA}$	LJ package, on 4-layer PCB based on JEDEC standard	35	°C/W
		LJ package, on 2-layer PCB with 0.8 in² 2-oz. copper each side	62	°C/W
		LY package, on 4-layer PCB based on JEDEC standard	48	°C/W
		LY package, (estimate) on 2-layer PCB with 1 in² 2-oz. copper each side	60	°C/W

*Additional thermal information available on the Allegro website.

Pin-out Diagrams



LJ Package (A4953)



LY Package (A4952)

Terminal List Table

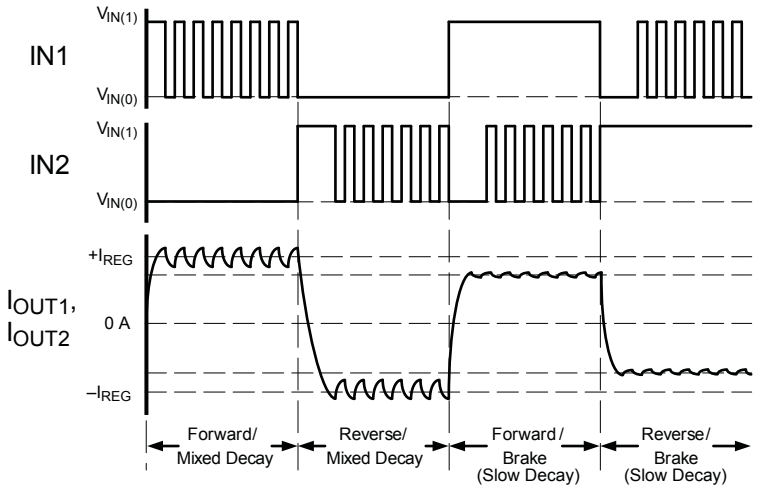
Name	Number		Function
	A4952	A4953	
FLTn	1	–	Fault output, active low
GND	10	1	Ground
IN1	4	3	Logic input 1
IN2	3	2	Logic input 2
LSS	8	7	Power return – sense resistor connection
OUT1	7	6	DMOS full bridge output 1
OUT2	9	8	DMOS full bridge output 2
PAD	–	–	Exposed pad for enhanced thermal dissipation
RTRY	2	–	Logic input
VBB	6	5	Load supply voltage
VREF	5	4	Analog input

ELECTRICAL CHARACTERISTICS Valid at T_J = 25°C, unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
General						
Load Supply Voltage Range	V_{BB}		8	–	40	V
$R_{DS(on)}$ Sink + Source Total	$R_{DS(on)}$	I_{OUT} = |1.5 A|, T_J = 25°C	–	0.8	1.0	Ω
		I_{OUT} = |1.5 A|, T_J = 125°C	–	1.3	1.6	Ω
Load Supply Current	I_{BB}	f_{PWM} < 30 kHz	–	10	–	mA
		Low Power Standby mode	–	–	10	µA
Body Diode Forward Voltage	V_f	Source diode, I_f = –1.5 A	–	–	1.5	V
		Sink diode, I_f = 1.5 A	–	–	1.5	V
Logic I/O Inputs						
Logic Input Voltage Range	$V_{IN(1)}$	INx pins	2.0	–	–	V
	$V_{IN(0)}$	INx pins	–	–	0.8	V
	$V_{IN(STANDBY)}$	INx pins, Low Power Standby mode	–	–	0.4	V
Logic Input Pull-Down Resistance	$R_{LOGIC(PD)}$	V_{IN} = 0 V = IN1 = IN2	–	50	–	kΩ
Logic Input Current	$I_{IN(1)}$	INx pins, V_{IN} = 2.0 V	–	40	100	µA
	$I_{IN(0)}$	INx pins, V_{IN} = 0.8 V	–	16	40	µA
Input Hysteresis	V_{HYS}		–	250	550	mV
Logic I/O Inputs (A4952 only)						
Retry Input Voltage	V_{RTRY}	RTRY pin = valid	–	–	200	mV
Retry Overcurrent Protection Pullup Voltage	$V_{RTRY(OC)}$	RTRY pin = open	–	3	–	V
Retry Short Circuit Current	I_{RTRY}	RTRY pin = GND	–	10	–	µA
Fault Output Voltage	V_{RST}	FLTn pin, I_{OUT} = 1 mA	–	–	0.5	V
Fault Output Leakage Current	I_{LK}	FLTn pin, no fault, pull-up to 5 V	–	–	1	µA
Timing						
Crossover Delay	t_{COD}		50	400	500	ns
V_{REF} Input Voltage Range	V_{REF}		0	–	5	V
Current Gain	A_V	V_{REF} / I_{SS}, V_{REF} = 5 V	9	–	10	V/V
		V_{REF} / I_{SS}, V_{REF} = 2.5 V	9	–	10	V/V
		V_{REF} / I_{SS}, V_{REF} = 1 V	8	–	10	V/V
Blank Time	t_{BLANK}		2	3	4	µs
Constant Off-time	t_{off}		16	25	34	µs
Standby Timer	t_{st}	IN1 = IN2 < $V_{IN(STANDBY)}$	–	1	–	ms
Power-Up Delay	t_{pu}		–	–	30	µs
Protection Circuits						
UVLO Enable Threshold	V_{BBUVLO}	V_{BB} increasing	–	7.5	7.95	V
UVLO Hysteresis	$V_{BBUVLOhys}$		–	500	–	mV
Thermal Shutdown Temperature	T_{JTSD}	Temperature increasing	–	160	–	°C
Thermal Shutdown Hysteresis	T_{TSDhys}	Recovery = T_{JTSD} – T_{TSDhys}	–	20	–	°C

Characteristic Performance

PWM Control Timing Diagram



PWM Control Truth Table

IN1	IN2	$10 \times V_S > V_{REF}$	OUT1	OUT2	Function
0	1	False	L	H	Reverse
1	0	False	H	L	Forward
0	1	True	H/L	L	Chop (mixed decay), reverse
1	0	True	L	H/L	Chop (mixed decay), forward
1	1	False	L	L	Brake (slow decay); after a Chop command
0	0	False	Z	Z	Coast, enters Low Power Standby mode after 1 ms

Note: Z indicates high impedance.

Functional Description

Device Operation

The A4952 and A4953 are designed to operate DC motors. The output drivers are all low-$R_{DS(on)}$, N-channel DMOS drivers that feature internal synchronous rectification to reduce power dissipation. The current in the output full bridge is regulated with fixed off-time pulse width modulated (PWM) control circuitry. The IN1 and IN2 inputs allow two-wire control for the bridge.

Protection circuitry includes internal thermal shutdown, and protection against shorted loads, or against output shorts to ground or supply. Undervoltage lockout prevents damage by keeping the outputs off until the driver has enough voltage to operate normally.

Standby Mode

Low Power Standby mode is activated when both input (INx) pins are low for longer than 1 ms. Low Power Standby mode disables most of the internal circuitry, including the charge pump and the regulator. When the A4952/A4953 is coming out of standby mode, the charge pump should be allowed to reach its regulated voltage (a maximum delay of 200 µs) before any PWM commands are issued to the device.

Internal PWM Current Control

Initially, a diagonal pair of source and sink FET outputs are enabled and current flows through the motor winding and the optional external current sense resistor, R_S. When the voltage across R_S equals the comparator trip value, then the current sense comparator resets the PWM latch. The latch then turns off the sink and source FETs (Mixed Decay mode).

V_{REF}

The maximum value of current limiting is set by the selection of R_{Sx} and the voltage at the VREF pin. The transconductance function is approximated by the maximum value of current limiting, $I_{TripMAX}$ (A), which is set by:

$$I_{TripMAX} = \frac{V_{REF}}{A_V \times R_S}$$

where V_{REF} is the input voltage on the VREF pin (V) and R_S is the resistance of the sense resistor (Ω) on the LSS terminal.

Overcurrent Protection

In the A4952, a current monitor will protect the IC from damage due to output shorts. The internal Overcurrent Protection (OCP) has the following features:

- Fault Output (FLTn pin). If a short is detected, the open drain FLTn output signal goes low.
- Retry Input (RTRY pin). Sets the action taken by the IC to respond to an OCP fault. If the RTRY pin is tied to GND, then the outputs will be turned-on again after a 2-ms timeout, to check if a fault condition remains. If the RTRY pin is left open, then the fault will be latched, and the IC will disable the outputs. The fault latch can only be cleared by coming out of Low Power Standby mode or by cycling the power to VBB.

Note: The A4953 overcurrent protection behaves in the same manner but the fault is latched and can only be reset by putting the device into standby mode or by cycling the power to VBB.

During OCP events, Absolute Maximum Ratings may be exceeded for a short period of time before the device latches.

Shutdown

If the die temperature increases to approximately 160°C, the full bridge outputs will be disabled until the internal temperature falls below a hysteresis, T_{TSDhys}, of 20°C. Internal UVLO is present on VBB to prevent the output drivers from turning-on below the UVLO threshold.

Braking

The braking function is implemented by driving the device in Slow Decay mode, which is done by applying a logic high to both inputs, after a bridge-enable Chop command (see PWM Control Truth Table). Because it is possible to drive current in both directions through the DMOS switches, this configuration effectively shorts-out the motor-generated BEMF, as long as the Chop command is asserted. The maximum current can be approximated by V_{BEMF} / R_L. Care should be taken to ensure that the maximum ratings of the device are not exceeded in worse case braking situations: high speed and high-inertia loads.

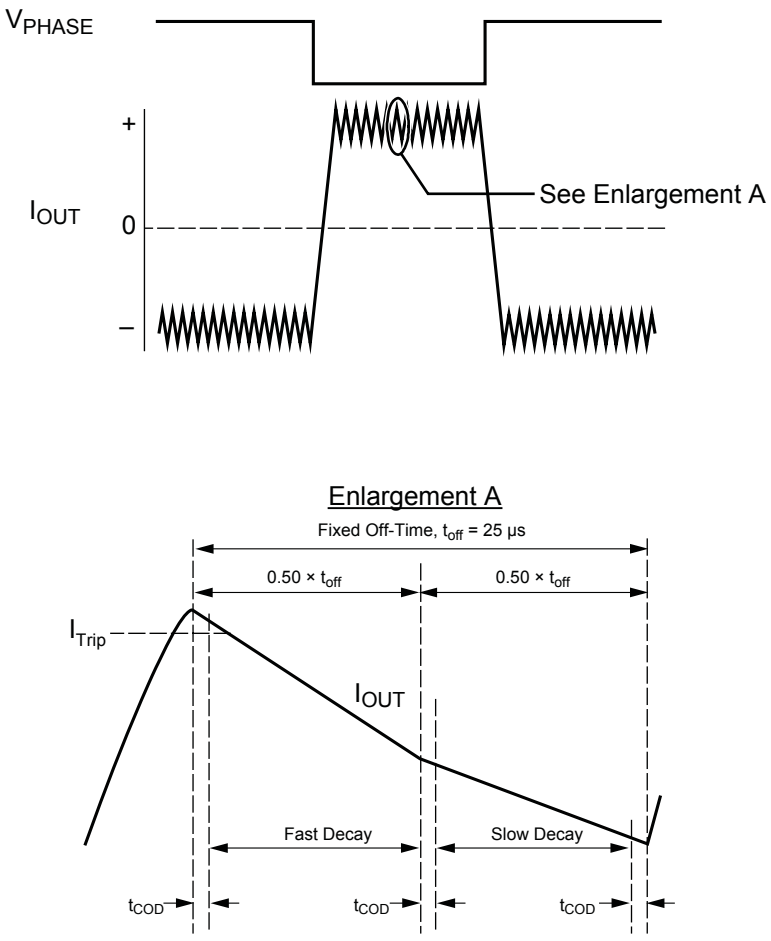
Synchronous Rectification

When a PWM off-cycle is triggered by an internal fixed off-time cycle, load current will recirculate. The A4952/A4953 synchronous rectification feature turns-on the appropriate DMOSFETs during the current decay, and effectively shorts out the body diodes with the low $R_{DS(on)}$ driver. This significantly lowers power dissipation. When a zero current level is detected, synchronous rectification is turned off to prevent reversal of the load current.

Mixed Decay Operation

The bridges operate in Mixed Decay mode. Referring to the lower panel of the figure below, as the trip point is reached, the device goes into fast decay mode for 50% of the fixed off-time period. After this fast decay portion the device switches to slow decay mode for the remainder of the off-time. During transitions from fast decay to slow decay, the drivers are forced off for the Crossover Delay, t_{COD}. This feature is added to prevent shoot-through in the bridge. During this "dead time" portion, synchronous rectification is not active, and the device operates in fast decay and slow decay only.

Mixed Decay Mode Operation



Application Information

Sense Pin (LSS)

In order to use PWM current control, a low-value resistor is placed between the LSS pin and ground for current sensing purposes. To minimize ground-trace IR drops in sensing the output current level, the current sensing resistor should have an independent ground return to the star ground point. This trace should be as short as possible. For low-value sense resistors, the IR drops in the PCB can be significant, and should be taken into account.

When selecting a value for the sense resistor be sure not to exceed the maximum voltage on the LSS pin of ±500 mV at maximum load. During overcurrent events, this rating may be exceeded for short durations.

Ground

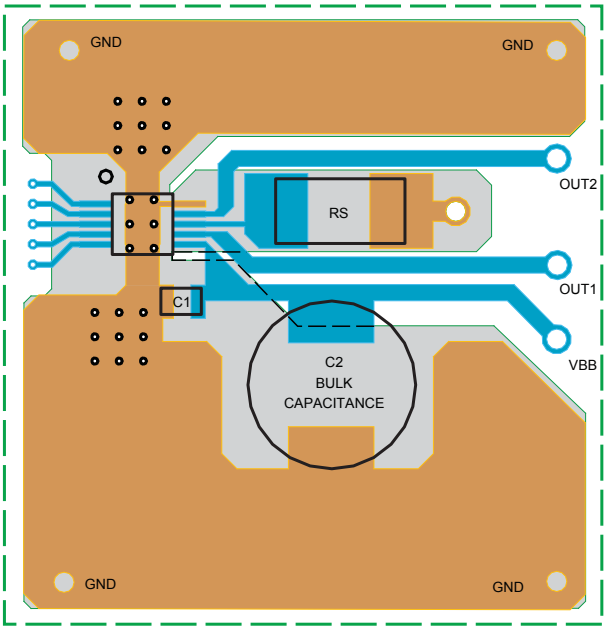
A star ground should be located as close to the A4952/ A4953 as possible. The copper ground plane directly under the exposed thermal pad of the device makes a good location for the star ground point. The exposed pad can be connected to ground for this purpose.

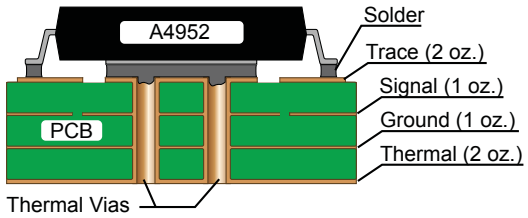
Layout

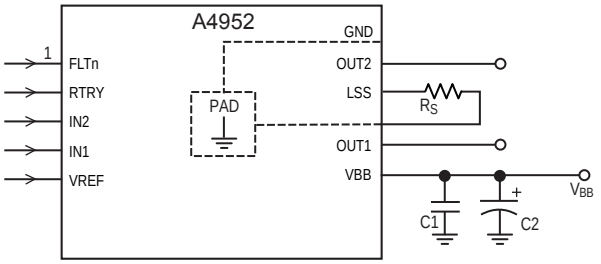
The PCB should have a thick ground plane. For optimum electrical and thermal performance, the A4952/A4953 must be soldered directly onto the board. On the underside of the A4952/A4953 package is an exposed pad, which provides a path for enhanced thermal dissipation. The thermal pad must be soldered directly to an exposed surface on the PCB in order to achieve optimal thermal conduction. Thermal vias are used to transfer heat to other layers of the PCB.

The load supply pin, VBB, should be decoupled with an electrolytic capacitor (typically 100 µF) in parallel with a lower valued ceramic capacitor placed as close as practicable to the device.

Layout for the A4952 (LY package)



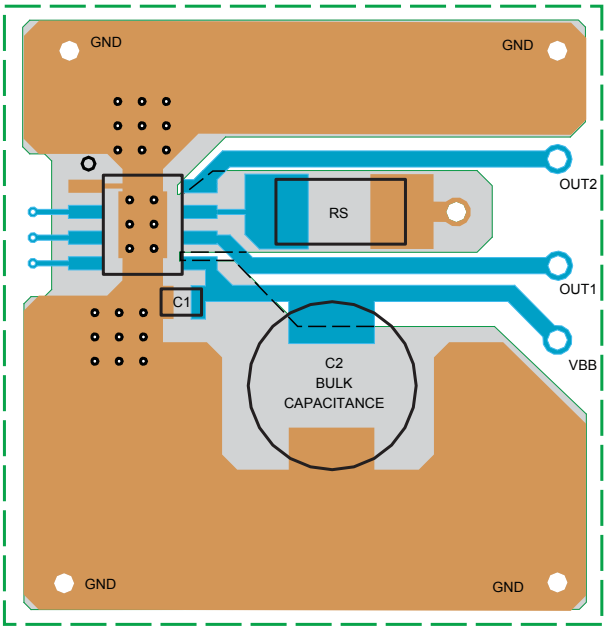


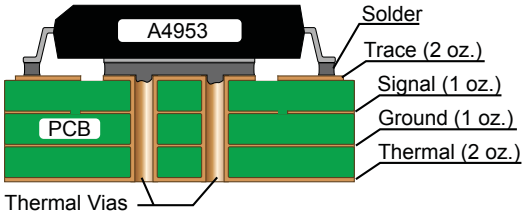


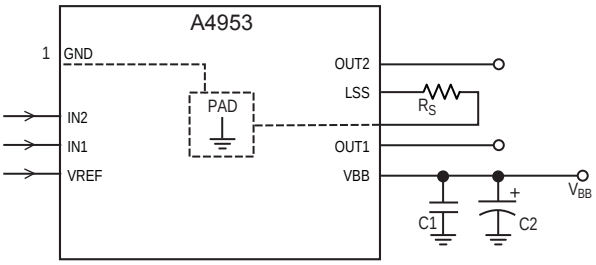
Bill of Materials

Item	Reference	Value	Units	Description
1	RS	0.25 (for V_{REF} = 5 V, I_{OUT} = 2 A)	Ω	2512, 1 W, 1% or better, carbon film chip resistor
2	C1	0.22	µF	X5R minimum, 50 V or greater
3	C2	100	µF	Electrolytic, 50 V or greater

Layout for the A4953 (LJ package)







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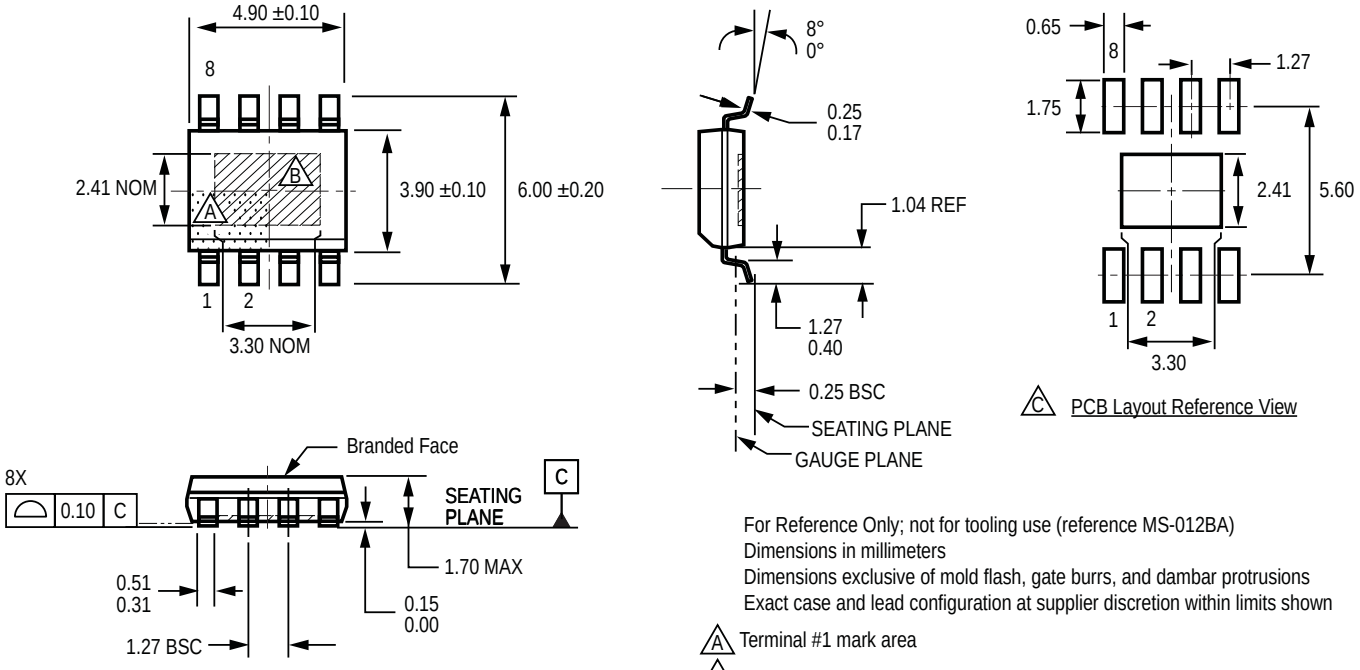
Package LJ, 8-Pin SOICN
with exposed thermal pad



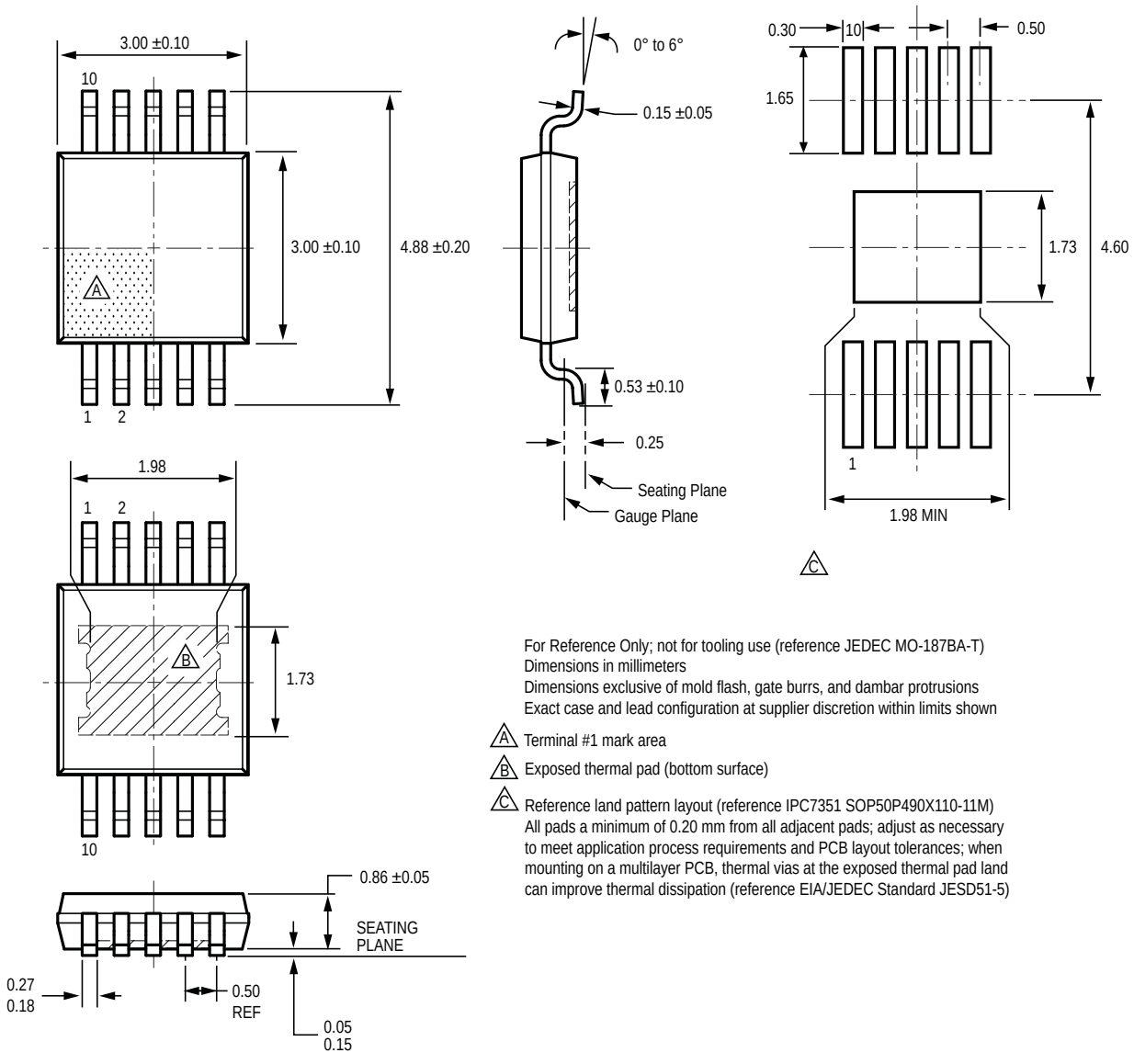
For Reference Only; not for tooling use (reference MS-012BA)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface); dimensions may vary with device

C Reference land pattern layout (reference IPC7351 SOIC127P600X175-9AM); all pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

Package LY, 10-Pin MSOP
with exposed thermal pad



For Reference Only; not for tooling use (reference JEDEC MO-187BA-T)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP50P490X110-11M)
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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