Data Sheet | July 28, 2008 | FN9223.1

Two-Phase Multiphase Buck PWM Controller with Integrated MOSFET Drivers

The ISL8101 two-phase PWM control IC provides a precision voltage regulation system for advanced loads up to 60A to 80A. Multiphase power conversion is a marked departure from single phase converter configurations employed to satisfy the increasing current demands of modern microprocessors and other electronic circuits. By distributing the power and load current, implementation of multiphase converters utilize smaller and lower cost transistors with fewer input and output capacitors. These reductions accrue from the higher effective conversion frequency with higher frequency ripple current due to the phase interleaving process of this topology.

Outstanding features of this controller IC include programmable VID codes compatible with Intel VRM9, VRM10, as well as AMD's Hammer microprocessors, along with a system regulation accuracy of ±1%. The ISL8101, though, does not intrinsically allow for load-line regulation (no droop).

Important features of this controller IC include a set of sophisticated overvoltage and overcurrent protection. Overvoltage results in the converter turning the lower MOSFETs ON to clamp the rising output voltage and protect the microprocessor. Like other Intersil multiphase controllers, the ISL8101 uses cost and space-saving $r_{DS(ON)}$ sensing for channel current balance and overcurrent protection. Channel current balancing is automatic and accurate with the integrated current-balance control system. Overcurrent protection can be tailored to any application with no need for additional parts. These features provide intelligent protection for modern power systems.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. (°C)	PACKAGE	PKG. DWG. #
ISL8101CRZ* (Note)	81 01CRZ	0 to +70	24 Ld 4x4 QFN (Pb-Free)	L24.4x4B
ISL8101IRZ* (Note)	81 01IRZ	-40 to +85	24 Ld 4x4 QFN (Pb-Free)	L24.4x4B
ISL8101EVAL1	Evaluation Platform			

*Add "-T" suffix for tape and reel. Please refer to TB347 for details on reel specifications.

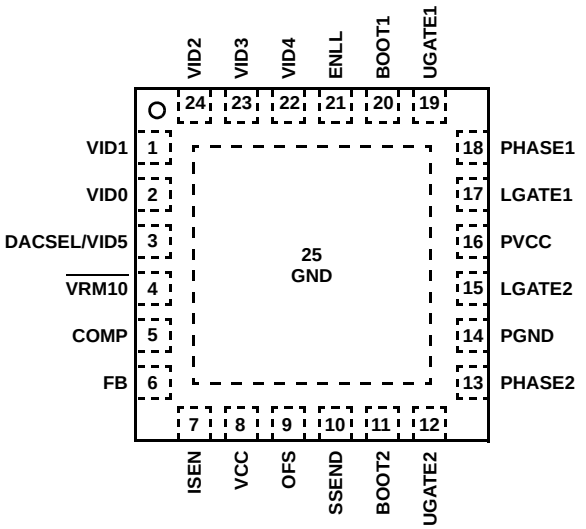
NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

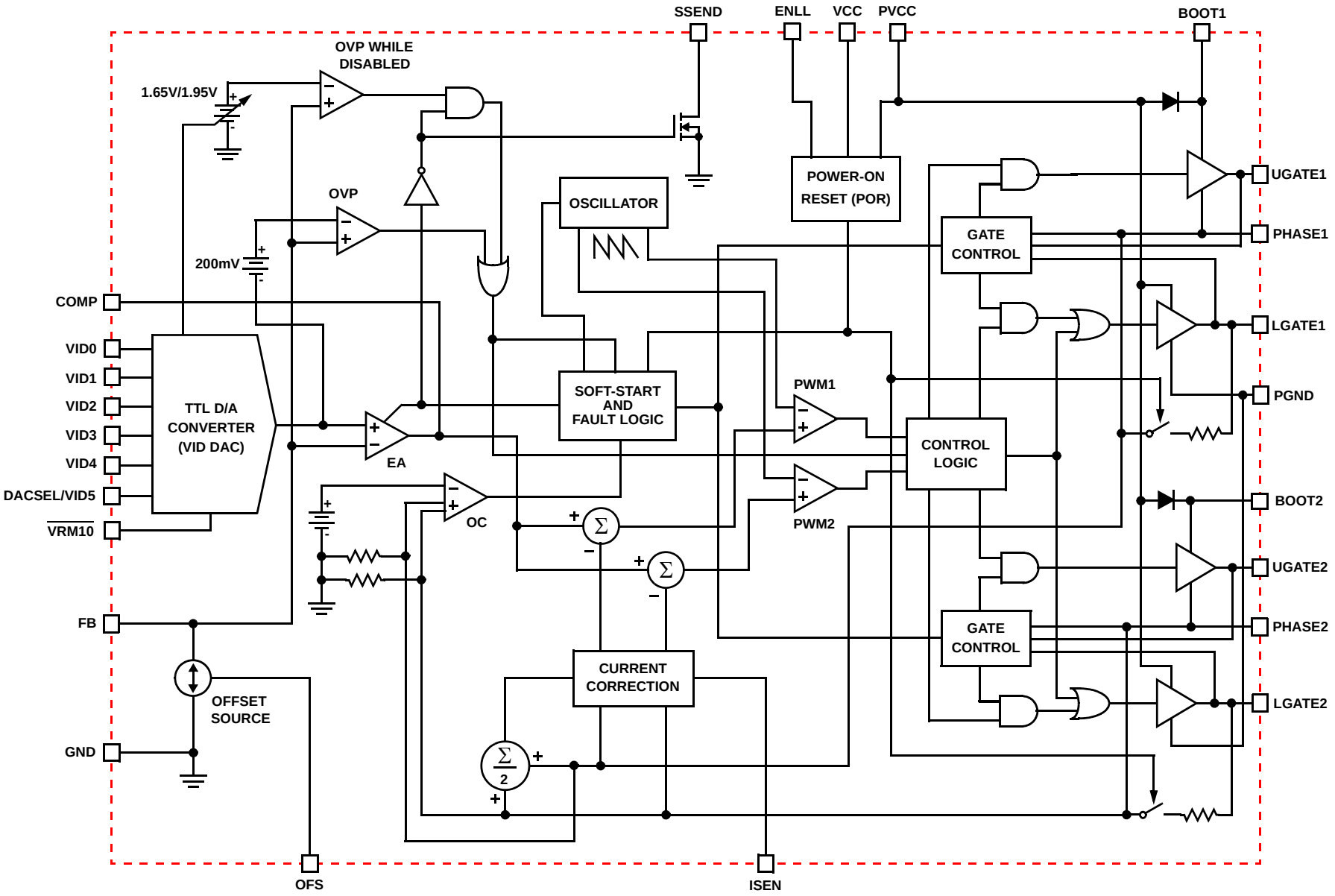
- Integrated Two-Phase Power Conversion
- 5V to 12V Input Voltage Conversion
- Precision Channel Current Sharing
  - Loss-Less Current Sampling - Uses $r_{DS(ON)}$
- Precision Output Voltage Regulation
  - ±1% System Accuracy Over-Temperature (Commercial)
- Microprocessor Voltage Identification Inputs
  - Up to a 6-Bit DAC
  - Selectable between Intel's VRM9, VRM10, or AMD's Hammer DAC codes
- Fast Transient Recovery Time
- Overcurrent Protection
- Pre-Biased Output Start-Up Operation
- Sources and Sinks Output Current
  - Bus Termination Applications
- Improved, Multi-tiered Overvoltage Protection
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package Footprint, Which Improves PCB Efficiency and has aThinner Profile
- Pb-free (RoHS compliant)

Pinout

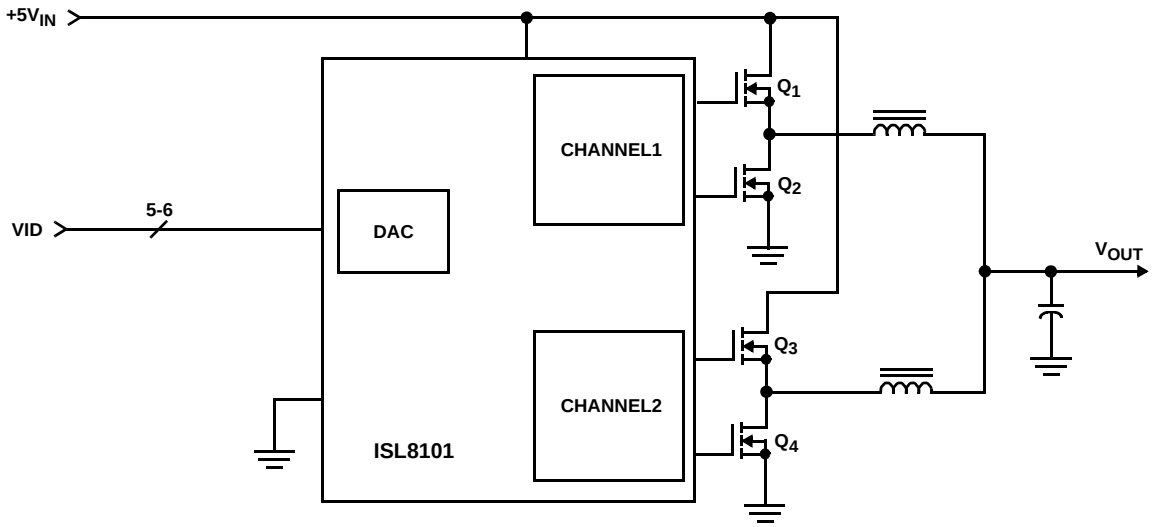
ISL8101
(24 LD QFN)
TOP VIEW



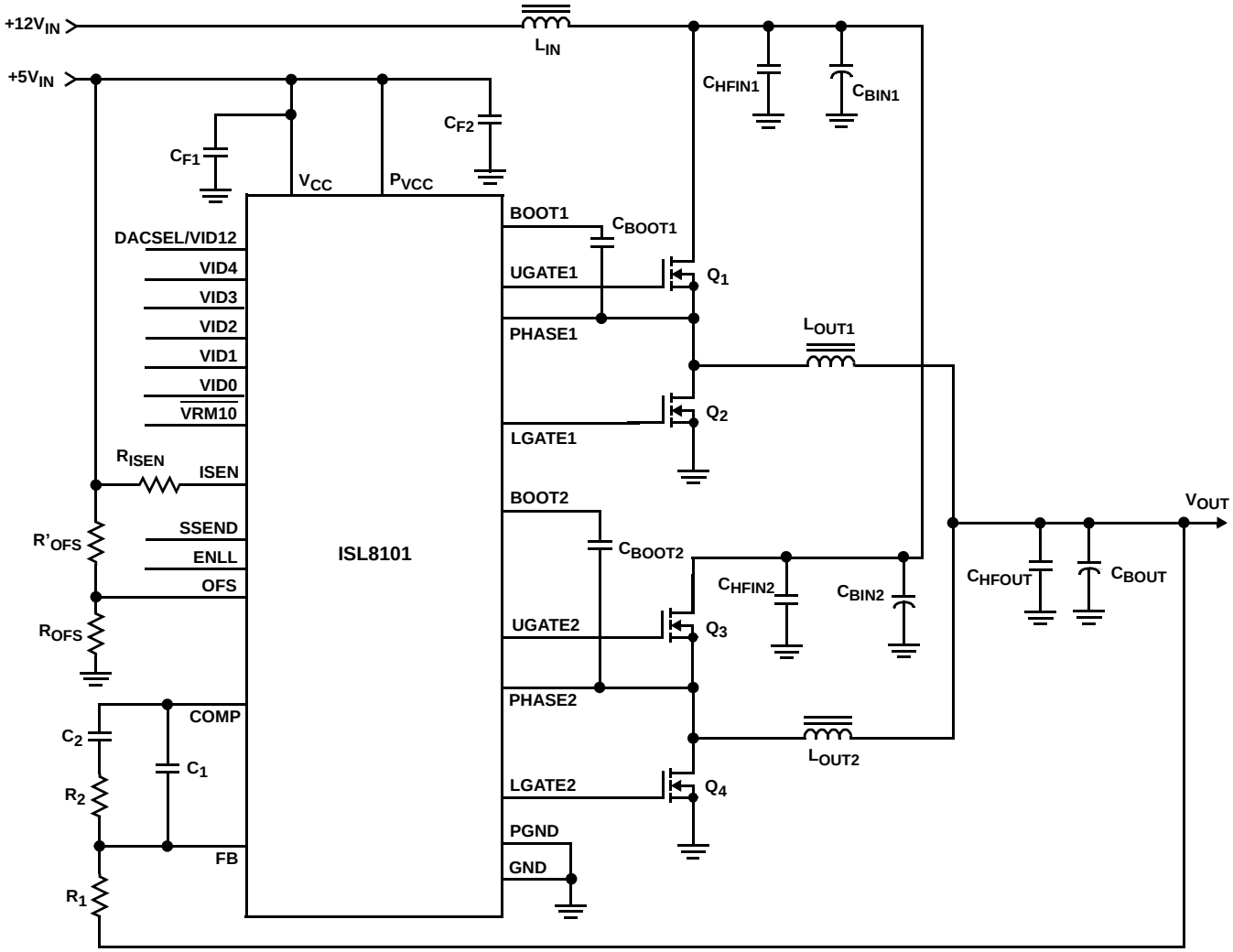
Block Diagram



Simplified Power System Diagram



Typical Application



Absolute Maximum Ratings

Supply Voltage, V_{CC}, P_{VCC} . . . . . -0.3V to +6.25V
Absolute Boot Voltage, V_{BOOT} . . . . . P_{GND} - 0.3V to P_{GND} + 27V
Phase Voltage, V_{PHASE} . . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
Upper Gate Voltage, V_{UGATE} . . . . V_{PHASE} - 0.3V to V_{BOOT} + 0.3V
Lower Gate Voltage, V_{LGATE} . . . . . P_{GND} - 0.3V to V_{CC} + 0.3V
Input, Output, or I/O Voltage . . . . . GND - 0.3V to V_{CC} + 0.3V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 1, 2)	45	7.5

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Supply Voltage . . . . . +5V ±5%
Ambient Temperature . . . . . 0°C to +70°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: V_{CC} = 5V, T_J = 0°C to +85°C, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS SUPPLY AND INTERNAL OSCILLATOR					
Input Bias Supply Current	I_{VCC}; ENLL = high	-	4	6	mA
VCC POR (Power-On Reset) Threshold	VCC Rising	4.2	4.4	4.6	V
	VCC Falling	3.7	3.9	4.1	V
PVCC POR (Power-On Reset) Threshold	PVCC Rising	-	4.3	-	V
	PVCC Falling	-	3.3	-	V
Switching Frequency (per channel)	T_J = +25°C to +85°C	189	222	255	kHz
	T_J = -40°C	166	205	241	kHz
Oscillator Ramp Amplitude (Note 3)	V_{P-P}	-	1.33	-	V
Maximum Duty Cycle		-	67	-	%
CONTROL THRESHOLDS					
ENLL Rising Threshold		-	0.645	-	V
ENLL Falling Threshold		-	0.567	-	mV
REFERENCE AND DAC					
System Accuracy		-1	-	1	%
	T_J = -40°C to +85°C	-1.5	-	1.5	%
DAC Input Low Voltage		-	-	0.4	V
DAC Input High Voltage		0.8	-	-	V
DAC Input Pull-Up Current	VIDx = 0V	-	45	-	µA
ERROR AMPLIFIER					
DC Gain (Note 3)	R_L = 10k to ground	-	96	-	dB
Gain-Bandwidth Product (Note 3)	C_L = 100pF, R_L = 10k to ground	-	20	-	MHz
Slew Rate (Note 3)	C_L = 100pF, Load = ±400µA	-	8	-	V/µs
Maximum Output Voltage	Load = 1mA	3.90	4.20	-	V
Minimum Output Voltage	Load = -1mA	-	0.80	0.90	V

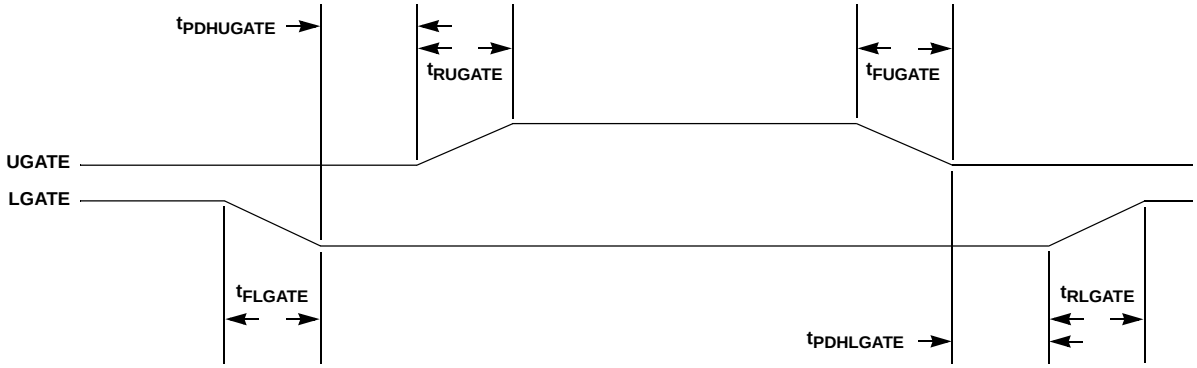
Electrical Specifications Test Conditions: V_{CC} = 5V, T_J = 0°C to +85°C, Unless Otherwise Specified. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
OVERCURRENT PROTECTION					
Overcurrent Trip Level		72	95	115	µA
PROTECTION					
Overvoltage Threshold while IC Disabled	VRM9.0 configuration	1.90	1.95	2.00	V
	Hammer and VRM10.0 configurations	1.60	1.65	1.70	V
Overvoltage Threshold	FB Rising	-	VID +200mV	-	V
Overvoltage Hysteresis		-	100	-	mV
SWITCHING TIME					
UGATE Rise Time (Note3)	t_{RUGATE}; V_{VCC} = 5V, 3nF Load	-	8	-	ns
LGATE Rise Time (Note3)	t_{RLGATE}; V_{VCC} = 5V, 3nF Load	-	8	-	ns
UGATE Fall Time (Note 3)	t_{FUGATE}; V_{VCC} = 5V, 3nF Load	-	8	-	ns
LGATE Fall Time (Note 3)	t_{FLGATE}; V_{VCC} = 5V, 3nF Load	-	4	-	ns
UGATE Turn-On Non-overlap (Note 3)	$t_{PDHUGATE}$; V_{VCC} = 5V, 3nF Load	-	8	-	ns
LGATE Turn-On Non-overlap (Note 3)	$t_{PDHLGATE}$; V_{VCC} = 5V, 3nF Load	-	8	-	ns
OUTPUT					
Upper Drive Source Resistance	100mA Source Current	-	1.0	2.5	Ω
Upper Drive Sink Resistance	100mA Sink Current	-	1.0	2.5	Ω
Lower Drive Source Resistance	100mA Source Current	-	1.0	2.5	Ω
Lower Drive Sink Resistance	100mA Sink Current	-	0.4	1.0	Ω

NOTE:

3. Limits should be considered typical and are not production tested.

Timing Diagram



Functional Pin Description

VCC (Pin 8)

Bias supply for the IC's small-signal circuitry. Connect this pin to a 5V supply and locally decouple using a quality 0.1µF ceramic capacitor. This pin is monitored for Power-On Reset (POR) purpose.

PVCC (Pin 16)

Power supply pin for the MOSFET drives. Connect this pin to a 5V supply and locally decouple using a quality 1µF ceramic capacitor. This pin is monitored for POR purpose.

GND and PGND (Pins 25 and 14)

Connect these pins to the circuit ground using the shortest possible paths. All internal small-signal circuitry is

referenced to the GND pin. LGATE drive is referenced to the PGND pin.

VID0-4 (Pins 2, 1, 24-22)

Voltage identification inputs from microprocessor. These pins respond to TTL logic thresholds. The ISL8101 decodes the VID inputs to establish the output voltage; see VID Tables beginning on page 9 for correspondence between DAC codes and output voltage settings. These pins are internally pulled high, to approximately 1.2V, by 40µA (typically) internal current sources; the internal pull-up current decrease to 0 as the VID voltage approaches the internal pull-up voltage. All VID pins are compatible with external pull-up voltages not exceeding the IC's bias voltage.

DACSEL/VID5 (Pin 3)

If $\overline{\text{VRM10}}$ pin is grounded, DACSEL/VID5 represents the 6th voltage identification input from the VRM10-compliant microprocessor, otherwise known as VID5. If $\overline{\text{VRM10}}$ pin is open or pulled high, DACSEL/VID5 selects the compliance standard for the internal DAC: pulled to ground it encodes the DAC with AMD Hammer VID codes, while left open or pulled high, it encodes the DAC with Intel VRM9.0 codes.

$\overline{\text{VRM10}}$ (Pin 4)

This pin selects VRM10.0 DAC compliance when grounded. Left open, it allows selection of either VRM9.0 or Hammer DAC compliance via DACSEL pin.

ENLL (Pin 21)

This pin is a precision-threshold (approximately 0.6V) enable pin. Held low, this pin disables controller operation. Pulled high, the pin enables the controller for operation.

FB and COMP (Pins 6, 5)

The internal error amplifier's inverting input and output respectively. These pins are connected to the external network used to compensate the regulator's feedback loop.

An internal current source injects the offset (OFS) current sampled into the FB pin. Pulling COMP to ground through an impedance lower than 15Ω disables the controller (same effect as ENLL pulled low).

ISEN (Pin 7)

This pin is used to close the current-balance loop and set the overcurrent protection threshold. A resistor connected between this pin and V_{CC} has a voltage drop forced across it equal to that sampled across the lower MOSFET's $r_{DS(ON)}$ during approximately the middle of its conduction interval. The resulting current through this resistor is used for channel current balancing and overcurrent protection. The voltage across the R_{ISEN} resistor is time multiplexed between the two channels.

To select the proper R_{ISEN} resistor, use Equation 1.

$$R_{ISEN} = \frac{r_{DS(ON)MAX} \times I_{OUT}}{95\mu A} \quad \text{(EQ. 1)}$$

where:

$r_{DS(ON)MAX}$ = lower MOSFET's highest drain-source ON resistance (Ω; include temperature effects)

I_{OUT} = channel maximum output current (A)

See "Channel Balance Current Loop" on page 7 for more information.

UGATE1, 2 (Pins 19, 12)

Connect these pins to the upper MOSFETs' gates. These pins are used to control the upper MOSFETs and are monitored for shoot-through prevention purposes. Maximum individual channel duty cycle is limited to 66%.

BOOT1, 2 (Pins 20, 11)

These pins provide the bias voltage for the upper MOSFETs' drives. Connect these pins to appropriately-chosen external bootstrap capacitors. Internal bootstrap diodes connected to the PVCC pins provide the necessary bootstrap charge.

PHASE1, 2 (Pins 18, 13)

Connect these pins to the sources of the upper MOSFETs. These pins are the return path for the upper MOSFETs' drives.

LGATE1, 2 (Pins 17, 15)

These pins are used to control the lower MOSFETs and are monitored for shoot-through prevention purposes. Connect these pins to the lower MOSFETs' gates.

OFS (Pin 9)

This pin is used to create an adjustable output voltage offset. For no offset, leave this pin open. For negative offset, connect a R'_{OFS} resistor from this pin to V_{CC} and size it according to Equation 2.

$$R'_{OFS} = R_1 \times \frac{1500}{V_{OFFSET}} \quad \text{(EQ. 2)}$$

where:

V_{OFFSET} = desired output voltage offset magnitude (mV)

For positive output voltage offset, connect a R_{OFS} resistor from this pin to GND, sizing it according to Equation 3.

$$R_{OFS} = R_1 \times \frac{500}{V_{OFFSET}} \quad \text{(EQ. 3)}$$

For more information, refer to "Output Voltage Setting" on page 9 .

SSEND (Pin 10)

This pin is an end of soft-start (SS) indicator; open drain output device stays ON during soft-start, and goes open when soft-start ends.

Operation

The ISL8101 employs simple voltage-mode control. Figure 1 shows a simplified diagram of the voltage regulation and current balance loops. Voltage feedback is used to precisely regulate the output voltage, while current feedback tightly controls the individual channel currents, I_{L1} and I_{L2}, and trips the OC protection, if so necessary.

VOLTAGE LOOP

Feedback from the output voltage is applied via resistor R_1 to the inverting input of the Error Amplifier. This signal can drive the Error Amplifier output either high or low, depending upon the output voltage. Low output voltage makes the amplifier output move towards a higher output voltage level. Amplifier output voltage is applied to the positive inputs of the PWM Circuit comparators via the channel current correction summing networks. Out-of-phase sawtooth signals are applied to the two PWM comparators inverting inputs. Increasing Error Amplifier voltage results in increased Comparator output duty cycle. This increased duty cycle signal is passed through the output drivers with no phase reversal to drive the external upper MOSFETs. Increased duty cycle or ON time for the upper MOSFET transistors results in increased output voltage to compensate for the low output voltage sensed.

CHANNEL BALANCE CURRENT LOOP

The current balance control loop works in a similar fashion to the voltage control loop, but with current control information applied individually to each channel's PWM circuit. The information used for this control is the voltage that is developed across the $r_{DS(ON)}$ of each lower MOSFET, while they are conducting. A single resistor converts and scales the voltage across the MOSFETs to a current that is applied to the Current Sensing circuit within the ISL8101. Output from these sensing circuits is applied to the current averaging circuit. Each PWM channel receives the difference current signal from the summing circuit that compares the average sensed current to the individual channel current. When a power channel's current is greater than the average current, the signal applied via the summing Correction circuit to the Comparator, reduces the output pulse width of the Comparator to compensate for the detected "above average" current in that channel.

MULTIPHASE POWER CONVERSION

Multiphase power conversion provides a cost-effective power solution when load currents are no longer easily supported by single-phase converters. Although its greater complexity presents additional technical challenges, the multiphase approach offers cost-saving advantages with improved response time, superior ripple cancellation, and thermal distribution.

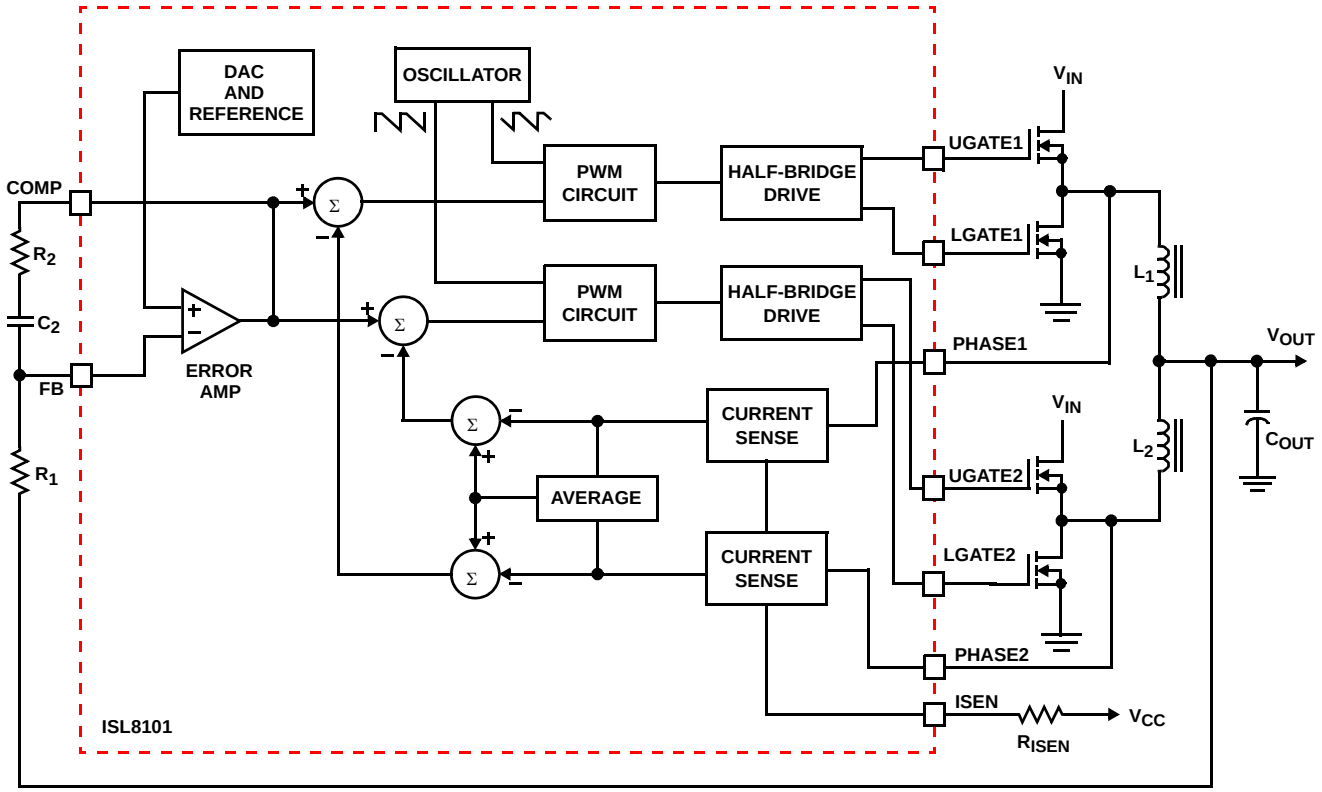


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM OF THE ISL8101 VOLTAGE AND CURRENT FEEDBACK

INTERLEAVING

The switching of each channel in a ISL8101-based converter is timed to be symmetrically out of phase with the other channel. As a result, the two-phase converter has a combined ripple frequency twice the frequency of one of its phases. In addition, the peak-to-peak amplitude of the combined inductor currents is proportionately reduced. Increased ripple frequency and lower ripple amplitude generally translate to lower per-channel inductance and lower total output capacitance for a given set of performance specifications.

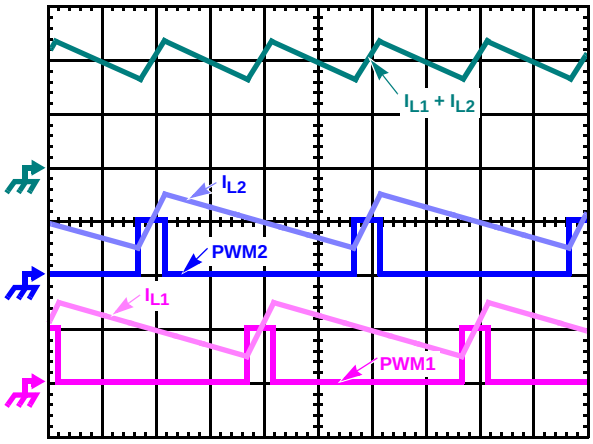


FIGURE 2. PWM AND INDUCTOR-CURRENT WAVEFORMS FOR 2-PHASE CONVERTER

Figure 2 illustrates the additive effect on output ripple frequency. The two channel currents (I_{L1} and I_{L2}), combine to form the AC ripple current and the DC load current. The ripple component has two times the ripple frequency of each individual channel current.

To understand the reduction of ripple current amplitude in the multiphase circuit, examine Equation 4 representing an individual channel's peak-to-peak inductor current.

$$I_{L,P\text{-}P} = \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 4)}$$

V_{IN} and V_{OUT} are the input and output voltages, respectively, L is the single-channel inductor value, and f_S is the switching frequency.

The output capacitors conduct the ripple component of the inductor current. In the case of multiphase converters, the capacitor current is the sum of the ripple currents from each of the individual channels (see Equation 5).

$$I_{P\text{-}P} = \frac{(V_{IN} - N \cdot V_{OUT}) \cdot V_{OUT}}{L \cdot f_S \cdot V_{IN}} \quad \text{(EQ. 5)}$$

Peak-to-peak ripple current, $I_{P\text{-}P}$, decreases by an amount proportional to the number of channels. Output-voltage ripple is a function of capacitance, capacitor equivalent series resistance (ESR), and inductor ripple current. Reducing the inductor ripple current allows the designer to use fewer or less costly output capacitors (should output ripple be an important design parameter).

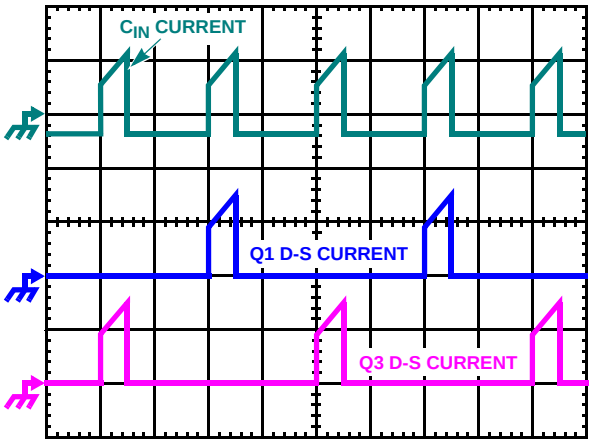


FIGURE 3. INPUT CAPACITOR CURRENT AND INDIVIDUAL CHANNEL CURRENTS IN A 2-PHASE CONVERTER

Another benefit of interleaving is the reduction of input ripple current. Input capacitance is determined in a large part by the maximum input ripple current. Multiphase topologies can improve overall system cost and size by lowering input ripple current and allowing the designer to reduce the cost of input capacitance. The example in Figure 3 illustrates input currents from a two-phase converter combining to reduce the total input ripple current.

Figure 12, part of the section entitled "Input Capacitor Selection" on page 19, can be used to determine the input-capacitor RMS current based on load current and duty cycle. The figure is provided as an aid in determining the optimal input capacitor solution.

PWM OPERATION

One switching cycle for the ISL8101 is defined as the time between consecutive PWM pulse terminations (turn-off of the upper MOSFET on a channel). Each cycle begins when a switching clock signal commands the upper MOSFET to go off. The other channel's upper MOSFET conduction is terminated 1/2 of a cycle later.

Once a channel's upper MOSFET is turned off, the lower MOSFET remains on for a minimum of 1/3 cycle. This forced off time is required to assure an accurate current sample. Following the 1/3-cycle forced off time, the controller enables the upper MOSFET output. Once enabled, the upper MOSFET output transitions high when the sawtooth signal crosses the adjusted error-amplifier output signal, as illustrated in the ISL8101's block diagram. Just prior to the upper drive turning the MOSFET on, the lower MOSFET

drive turns the freewheeling element off. The upper MOSFET is kept on until the clock signals the beginning of the next switching cycle and the PWM pulse is terminated.

CURRENT SENSING

ISL8101 senses current by sampling the voltage across the lower MOSFET during its conduction interval. MOSFET $r_{DS(ON)}$ sensing is a no-added-cost method to sense current for channel current balance and overcurrent protection.

The PHASE pins are used as inputs for each channel. Internal circuitry samples the lower MOSFETs' $r_{DS(ON)}$ voltage, once each cycle, during their conduction periods and time multiplexes the sampled voltages across the ISEN resistor. The current that is thus developed through the ISEN resistor is duplicated and used for channel current balancing and overcurrent detection.

CHANNEL-CURRENT BALANCE

Another benefit of multiphase operation is the thermal advantage gained by distributing the dissipated heat over multiple devices and greater area. By doing this, the designer avoids the complexity of driving multiple parallel MOSFETs and the expense of using expensive heat sinks and exotic magnetic materials.

In order to fully realize the thermal advantage, it is important that each channel in a multiphase converter be controlled to deliver about the same current at any load level. Intersil multiphase controllers ensure current balance by comparing each channel's current to the average current delivered by all channels and making appropriate adjustments to each channel's pulse width based on the error. The error signal modifies the pulse width to correct any unbalance and force the error toward zero.

OVERCURRENT PROTECTION

The individual channel currents, as sensed via the PHASE pins and scaled via the ISEN resistor, are continuously monitored and compared with an internal 95µA reference current. If both channels' currents exceed, at any time, the reference current, the overcurrent comparator triggers an overcurrent event. Similarly, an OC event is also triggered if either channel's current exceeds the 95µA reference for 7 consecutive switching cycles.

As a result of an OC event, output drives on both channels turn off both upper and lower MOSFETs. The system then waits in this state for a period of 4096 switching clock cycles.

The wait period is followed by a soft-start attempt. If the soft-start attempt is successful, operation continues as normal. Should the soft-start attempt fail, the ISL8101 repeats the 2048-cycle wait period and follows with another soft-start attempt. This hiccup mode of operation continues indefinitely (as depicted in Figure 4) for as long as the controller is enabled or until the overcurrent condition is removed.

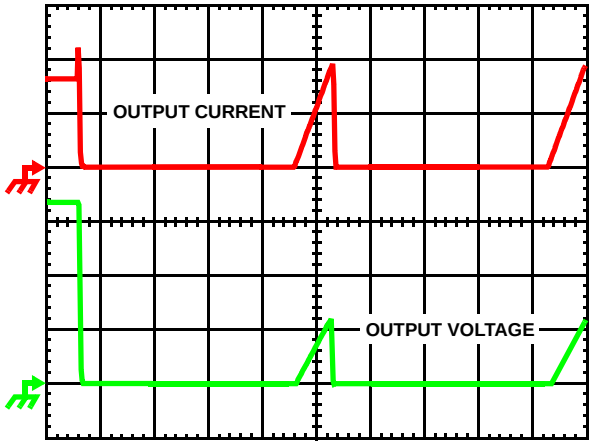


FIGURE 4. OVERCURRENT BEHAVIOR IN HICCUP MODE

OUTPUT VOLTAGE SETTING

The ISL8101 uses a digital to analog converter (DAC) to generate a reference voltage based on the logic signals at the VID pins. The DAC decodes the 5 or 6-bit logic signals into one of the discrete voltages shown in Tables 1, 2 and 3. Each VID pin is pulled up to an internal 1.2V voltage by weak current sources (about 45µA current, decreasing to 0 as the voltage at the VID pins varies from 0 to the internal 1.2V pull-up voltage). External pull-up resistors or active-high output stages can augment the pull-up current sources, up to a voltage of 5V.

The ISL8101 accommodates three different DAC ranges: Intel VRM9.0, AMD Hammer, or Intel VRM10.0. See "Functional Pin Description" on page 5 for proper connections for desired DAC range compatibility.

TABLE 1. AMD HAMMER VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	0.800
1	1	1	0	1	0.825
1	1	1	0	0	0.850
1	1	0	1	1	0.875
1	1	0	1	0	0.900
1	1	0	0	1	0.925
1	1	0	0	0	0.950
1	0	1	1	1	0.975
1	0	1	1	0	1.000
1	0	1	0	1	1.025
1	0	1	0	0	1.050
1	0	0	1	1	1.075

TABLE 1. AMD HAMMER VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
1	0	0	1	0	1.100
1	0	0	0	1	1.125
1	0	0	0	0	1.150
0	1	1	1	1	1.175
0	1	1	1	0	1.200
0	1	1	0	1	1.225
0	1	1	0	0	1.250
0	1	0	1	1	1.275
0	1	0	1	0	1.300
0	1	0	0	1	1.325
0	1	0	0	0	1.350
0	0	1	1	1	1.375
0	0	1	1	0	1.400
0	0	1	0	1	1.425
0	0	1	0	0	1.450
0	0	0	1	1	1.475
0	0	0	1	0	1.500
0	0	0	0	1	1.525
0	0	0	0	0	1.550

TABLE 2. VRM9 VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VDAC
1	1	1	1	1	Off
1	1	1	1	0	1.100
1	1	1	0	1	1.125
1	1	1	0	0	1.150
1	1	0	1	1	1.175
1	1	0	1	0	1.200
1	1	0	0	1	1.225
1	1	0	0	0	1.250
1	0	1	1	1	1.275
1	0	1	1	0	1.300
1	0	1	0	1	1.325
1	0	1	0	0	1.350
1	0	0	1	1	1.375
1	0	0	1	0	1.400
1	0	0	0	1	1.425
1	0	0	0	0	1.450

TABLE 2. VRM9 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VDAC
0	1	1	1	1	1.475
0	1	1	1	0	1.500
0	1	1	0	1	1.525
0	1	1	0	0	1.550
0	1	0	1	1	1.575
0	1	0	1	0	1.600
0	1	0	0	1	1.625
0	1	0	0	0	1.650
0	0	1	1	1	1.675
0	0	1	1	0	1.700
0	0	1	0	1	1.725
0	0	1	0	0	1.750
0	0	0	1	1	1.775
0	0	0	1	0	1.800
0	0	0	0	1	1.825
0	0	0	0	0	1.850

TABLE 3. VRM10 VOLTAGE IDENTIFICATION CODES

VID4	VID3	VID2	VID1	VID0	VID5	VDAC
1	1	1	1	1	1	Off
1	1	1	1	1	0	Off
0	1	0	1	0	0	0.8375
0	1	0	0\	1	1	0.8500
0	1	0	0	1	0	0.8625
0	1	0	0	0	1	0.8750
0	1	0	0	0	0	0.8875
0	0	1	1	1	1	0.9000
0	0	1	1	1	0	0.9125
0	0	1	1	0	1	0.9250
0	0	1	1	0	0	0.9375
0	0	1	0	1	1	0.9500
0	0	1	0	1	0	0.9625
0	0	1	0	0	1	0.9750
0	0	1	0	0	0	0.9875
0	0	0	1	1	1	1.0000
0	0	0	1	1	0	1.0125
0	0	0	1	0	1	1.0250
0	0	0	1	0	0	1.0375
0	0	0	0	1	1	1.0500
0	0	0	0	1	0	1.0625
0	0	0	0	0	1	1.0750

TABLE 3. VRM10 VOLTAGE IDENTIFICATION CODES (Continued)

VID4	VID3	VID2	VID1	VID0	VID5	VDAC
0	0	0	0	0	0	1.0875
1	1	1	1	0	1	1.1000
1	1	1	1	0	0	1.1125
1	1	1	0	1	1	1.1250
1	1	1	0	1	0	1.1375
1	1	1	0	0	1	1.1500
1	1	1	0	0	0	1.1625
1	1	0	1	1	1	1.1750
1	1	0	1	1	0	1.1875
1	1	0	1	0	1	1.2000
1	1	0	1	0	0	1.2125
1	1	0	0	1	1	1.2250
1	1	0	0	1	0	1.2375
1	1	0	0	0	1	1.2500
1	1	0	0	0	0	1.2625
1	0	1	1	1	1	1.2750
1	0	1	1	1	0	1.2875
1	0	1	1	0	1	1.300
1	0	1	1	0	0	1.3125
1	0	1	0	1	1	1.3250
1	0	1	0	1	0	1.3375
1	0	1	0	0	1	1.3500
1	0	1	0	0	0	1.3625
1	0	0	1	1	1	1.3750
1	0	0	1	1	0	1.3875
1	0	0	1	0	1	1.4000
1	0	0	1	0	0	1.4125
1	0	0	0	1	1	1.4250
1	0	0	0	1	0	1.4375
1	0	0	0	0	1	1.4500
1	0	0	0	0	0	1.4625
0	1	1	1	1	1	1.4750
0	1	1	1	1	0	1.4875
0	1	1	1	0	1	1.5000
0	1	1	1	0	0	1.5125
0	1	1	0	1	1	1.5250
0	1	1	0	1	0	1.5375
0	1	1	0	0	1	1.5500
0	1	1	0	0	0	1.5625
0	1	0	1	1	1	1.5750
0	1	0	1	1	0	1.5875
0	1	0	1	0	1	1.6000

DYNAMIC VID (VID-ON-THE-FLY)

The ISL8101 is capable of executing on-the-fly output voltage changes. The way the ISL8101 reacts to a change in the VID code is dependent on the VID configuration. In VRM9 or AMD Hammer settings, the ISL8101 checks for a change in the VID code four times each switching cycle. The VID code is the bit pattern present at pins VID4-VID0. If a new code is established and it stays the same for 12 switching cycles, the ISL8101 begins changing the reference by making one step change every four switching cycles until it reaches the new VID code. Figure 5 depicts such a transition, from 1.5V to 1.7V

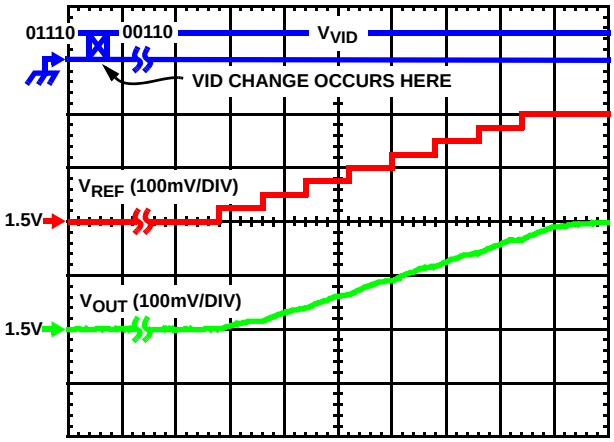


FIGURE 5. TYPICAL DYNAMIC-VID OPERATION, VRM9 DAC SETTING

In VRM10 setting, the ISL8101 checks for a change in the VID code six times each switching cycle. If a new code is established and it stays the same for 3 consecutive readings, the ISL8101 recognizes the change and increments the reference. Specific to VRM10, the processor controls the VID transitions and is responsible for incrementing or decrementing one VID step at a time. In VRM10 setting, the ISL8101 will immediately change the reference to the new requested value as soon as the request is validated; in cases where the reference step is too large, the sudden change can trigger overcurrent or overvoltage events.

In non-VRM10 settings, due to the way the ISL8101 recognizes VID code changes, up to one full switching period may pass before a VID change registers. Thus, the total time required for a VID change, t_{DVID}, is dependent on the switching frequency (f_S), the size of the change (ΔV_{ID}), and the time required to register the VID change. The approximate time required for a ISL8101-based converter in VRM9 configuration running at typical f_S (222kHz) to perform a 1.5V-to-1.7V reference voltage change is about 196µs, as calculated using Equation 6. (this example is also illustrated in Figure 5).

$$t_{DVID} \cong \frac{1}{f_S}\left(\frac{4\Delta V_{VID}}{0.025} + 13\right) \quad \text{(EQ. 6)}$$

OVERVOLTAGE PROTECTION

The ISL8101 benefits from a multi-tiered approach to overvoltage protection.

A pre-POR mechanism is at work while the chip does not have sufficient bias voltage to initiate an active response to an OV situation. Thus, while VCC is below its POR level, the lower drives are three-stated and internal 5kΩ (typically) resistors are connected from PHASE to their respective LGATE pins. As a result, output voltage, duplicated at the PHASE nodes via the output inductors, is effectively clamped at the lower MOSFETs' threshold level. This approach ensures no catastrophic output voltage can be developed at the output of an ISL8101-based regulator (for most typical applications).

The pre-POR mechanism is removed once the bias is above the POR level, and a fixed-threshold OVP goes into effect. Based on the specific chip configuration, the OVP goes into effect once the voltage sensed at the FB pin exceeds about 1.65V (Hammer/VR10) or 1.95V (VR9 configuration). Should the output voltage exceed these thresholds, the lower MOSFETs are turned on.

During soft-start, the OVP threshold changes to the higher of the fixed threshold (1.65V/1.95V) or the DAC setting plus 200mV. At the end of the soft-start, the OVP threshold changes to the DAC setting plus 200mV.

In any of the described post-POR functionality, OVP results in the turn-on of the lower MOSFETs. Once turned on, the lower MOSFETs are only turned off when the output voltage drops below the OV comparator's hysteretic threshold. The OVP process repeats if the voltage rises back above the designated threshold. The occurrence of an OVP event does not latch the controller; should the phenomenon be transitory, the controller resumes normal operation following such an event.

ON/OFF CONTROL

The internal power-on reset circuit (POR) prevents the ISL8101 from starting before the bias voltage at VCC and PVCC reach the rising POR thresholds, as defined in "Electrical Specifications" on page 4. The POR levels are sufficiently high to guarantee that all parts of the ISL8101 can perform their functions properly once bias is applied to the part. While bias is below the rising POR thresholds, the controlled MOSFETs are kept in an off state.

A secondary disablement feature is available via the threshold-sensitive enable input (ENLL). This optional feature prevents the ISL8101 from operating until a certain other voltage rail is available and above some selectable threshold. For example, when down-converting off a 12V input, it may be desirable the ISL8101-based converter does not start up until the power input is sufficiently high. The schematic in Figure 6 demonstrates coordination of the ISL8101 with such a rail; the resistor components are chosen to enable the ISL8101 as the 12V input exceeds approximately 9.75V. Additionally, an open-drain or open-collector device can be used to wire-AND a second (or multiple) control signal, as shown in Figure 6. To defeat the threshold-sensitive enable, connect ENLL to VCC directly or via a pull-up resistor.

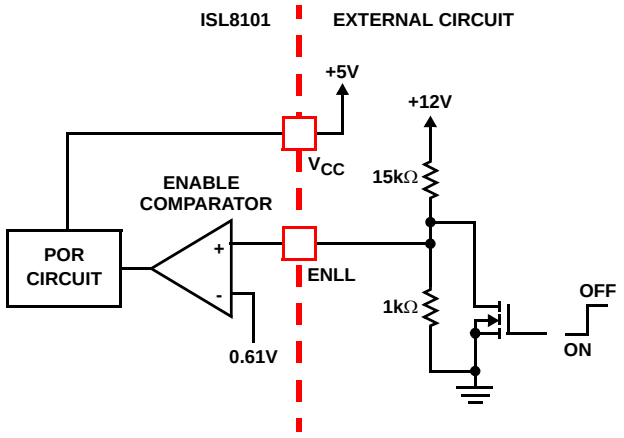


FIGURE 6. START-UP COORDINATION USING THRESHOLD-SENSITIVE ENABLE (ENLL) PIN

The '11111' VID code is reserved as a signal to the controller that no load is present. The controller is disabled while receiving this VID code and will subsequently start up upon receiving any other code.

In summary, for the ISL8101 to operate, the following conditions need be met: V_{CC} and P_{VCC} must be greater than their respective POR thresholds, the voltage at ENLL must be greater than 0.61V, and VID has to be different than '11111'. Once all these conditions are met, the controller immediately initiates a soft-start sequence.

SOFT-START

The soft-start function allows the converter to bring up the output voltage in a controlled fashion, resulting in a linear ramp-up. Following a delay of 16 PHASE clock cycles (about 70µs) between enabling the chip and the start of the ramp, the output voltage progresses at a fixed rate of 12.5mV per 16 PHASE clock cycles.

Thus, the soft-start period (not including the 70µs wait) up to a given voltage, V_{DAC}, can be approximated by Equation 7.

$$t_{SS} = \frac{V_{DAC} \cdot 1280}{f_S} \quad \text{(EQ. 7)}$$

where V_{DAC} is the DAC-set VID voltage, and f_S is the switching frequency (typically 222kHz).

The ISL8101 also has the ability to start-up into a pre-charged output, without causing any unnecessary disturbance. The FB pin is monitored during soft-start, and should it be higher than the equivalent internal ramping reference voltage, the output drives hold both MOSFETs off. Once the internal ramping reference exceeds the FB pin

potential, the output drives are enabled, allowing the output to ramp from the pre-charged level to the final level dictated by the DAC setting. Should the output be pre-charged to a level exceeding the DAC setting, the output drives are enabled at the end of the soft-start period, leading to an abrupt correction in the output voltage down to the DAC-set level.

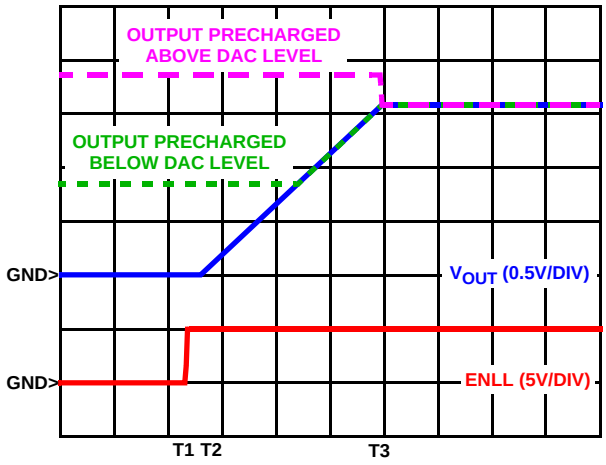


FIGURE 7. SOFT-START WAVEFORMS FOR ISL8101-BASED MULTIPHASE CONVERTER

FREQUENCY COMPENSATION

The ISL8101 multiphase converter behaves in a similar manner to a voltage-mode controller. This section highlights the design consideration for a voltage-mode controller requiring external compensation. To address a broad range of applications, a type-3 feedback network is recommended.

Figure 8 highlights the voltage-mode control loop for a synchronous-rectified buck converter, applicable, with a small number of adjustments, to the multiphase ISL8101 circuit. The output voltage (V_{OUT}) is regulated to the reference voltage, VREF, level. The error amplifier output (COMP pin voltage) is compared with the oscillator (OSC) modified saw-tooth wave to provide a pulse-width modulated wave with an amplitude of V_{IN} at the PHASE node. The PWM wave is smoothed by the output filter (L and C). The output filter capacitor bank's equivalent series resistance is represented by the series resistor E.

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC gain, given by $d_{MAX}V_{IN}/V_{OSC}$, and shaped by the output filter, with a double pole break frequency at F_{LC} and a zero at F_{CE}. For the purpose of this analysis, L and D represent the individual channel inductance and its DCR divided by 2 (equivalent parallel value of the two output inductors), while C and E represents the total output capacitance and its equivalent series resistance (see Equation 8).

$$F_{LC} = \frac{1}{2\pi \cdot \sqrt{L \cdot C}} \qquad F_{CE} = \frac{1}{2\pi \cdot C \cdot E} \qquad \text{(EQ. 8)}$$

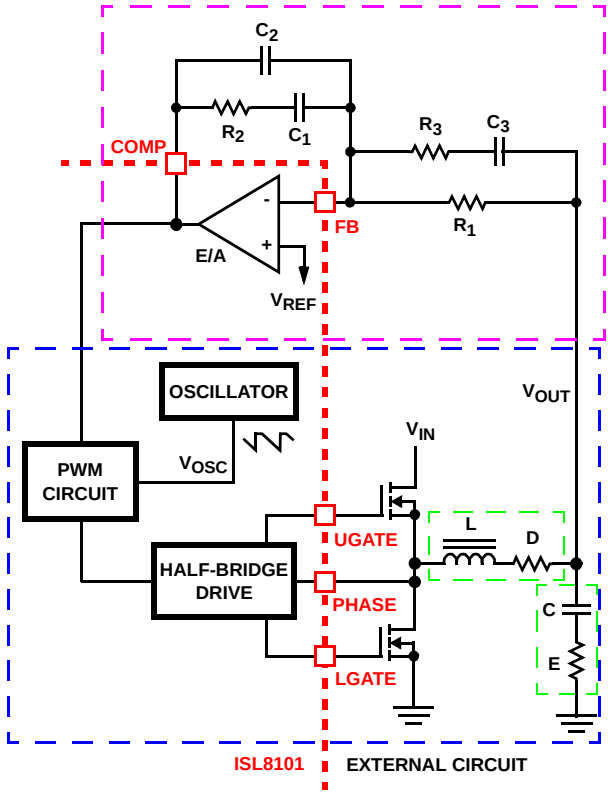


FIGURE 8. VOLTAGE-MODE BUCK CONVERTER COMPENSATION DESIGN

The compensation network consists of the error amplifier (internal to the ISL8101) and the external R_1-R_3, C_1-C_3 components. The goal of the compensation network is to provide a closed loop transfer function with high 0dB crossing frequency (F_0; typically 0.1 to 0.3 of F_{SW}) and adequate phase margin (better than 45°). Phase margin is the difference between the closed loop phase at F_{0dB} and 180°. Equations 9,10, 11, and 12 relate the compensation network's poles, zeros and gain to the components (R_1, R_2, R_3, C_1, C_2, and C_3) (see Figure 8). Use the following guidelines for locating the poles and zeros of the compensation network:

1. Select a value for R_1 (1kΩ to 5kΩ, typically). Calculate value for R_2 for desired converter bandwidth (F_0).

$$R2 = \frac{V_{OSC} \cdot R_1 \cdot F_0}{d_{MAX} \cdot V_{IN} \cdot F_{LC}} \qquad \text{(EQ. 9)}$$

2. Calculate C_1 such that F_{Z1} is placed at a fraction of the F_{LC}, at 0.1 to 0.75 of F_{LC} (to adjust, change the 0.5 factor to desired number). The higher the quality factor of the output filter and/or the higher the ratio F_{CE}/F_{LC}, the lower the F_{Z1} frequency (to maximize phase boost).

$$C_1 = \frac{1}{2\pi \cdot R_2 \cdot 0.5 \cdot F_{LC}} \qquad \text{(EQ. 10)}$$

3. Calculate C_2 such that F_{P1} is placed at F_{CE}.

$$C_2 = \frac{C_1}{2\pi \cdot R_2 \cdot C_1 \cdot F_{CE} - 1} \quad \text{(EQ. 11)}$$

4. Calculate R_3 (see Equation 12) such that F_{Z2} is placed at F_{LC}. Calculate C_3 such that F_{P2} is placed below F_{SW} (typically, 0.5 to 1.0 times F_{SW}). F_{SW} represents the per-channel switching frequency. Change the numerical factor to reflect desired placement of this pole. Placement of F_{P2} lower in frequency helps reduce the gain of the compensation network at high frequency, in turn reducing the HF ripple component at the COMP pin and minimizing resultant duty cycle jitter.

$$R_3 = \frac{R_1}{\frac{F_{SW}}{F_{LC}} - 1} \quad \text{(EQ. 12)}$$

$$C_3 = \frac{1}{2\pi \cdot R_3 \cdot 0.7 \cdot F_{SW}}$$

It is recommended a mathematical model is used to plot the loop response. Check the loop gain against the error amplifier's open-loop gain. Verify phase margin results and adjust as necessary. Equations 13 and 14 describe the frequency response of the modulator (G_{MOD}), feedback compensation (G_{FB}) and closed-loop response (G_{CL}):

$$G_{MOD}(f) = \frac{d_{MAX} \cdot V_{IN}}{V_{OSC}} \cdot \frac{1 + s(f) \cdot E \cdot C}{1 + s(f) \cdot (E + D) \cdot C + s^2(f) \cdot L \cdot C}$$

$$G_{FB}(f) = \frac{1 + s(f) \cdot R_2 \cdot C_1}{s(f) \cdot R_1 \cdot (C_1 + C_2)} \cdot \frac{1 + s(f) \cdot (R_1 + R_3) \cdot C_3}{(1 + s(f) \cdot R_3 \cdot C_3) \cdot \left(1 + s(f) \cdot R_2 \cdot \left(\frac{C_1 \cdot C_2}{C_1 + C_2}\right)\right)} \quad \text{(EQ. 13)}$$

$$G_{CL}(f) = G_{MOD}(f) \cdot G_{FB}(f) \qquad \text{where, } s(f) = 2\pi \cdot f \cdot j$$

COMPENSATION BREAK FREQUENCY EQUATIONS

$$F_{Z1} = \frac{1}{2\pi \cdot R_2 \cdot C_1} \qquad F_{P1} = \frac{1}{2\pi \cdot R2 \cdot \frac{C_1 \cdot C_2}{C_1 + C_2}} \quad \text{(EQ. 14)}$$

$$F_{Z2} = \frac{1}{2\pi \cdot (R_1 + R_3) \cdot C_3} \qquad F_{P2} = \frac{1}{2\pi \cdot R_3 \cdot C_3}$$

Figure 9 shows an asymptotic plot of the DC/DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak dependent on the quality factor (Q) of the output filter, which is not shown. Using the above guidelines should yield a compensation gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at F_{P2} against the capabilities of the error amplifier. The closed loop gain, G_{CL}, is constructed on the log-log graph of Figure 9 by adding the modulator gain, G_{MOD} (in dB), to the feedback compensation gain, G_{FB} (in dB). This is equivalent to multiplying the modulator transfer function and the compensation transfer function and then plotting the resulting gain.

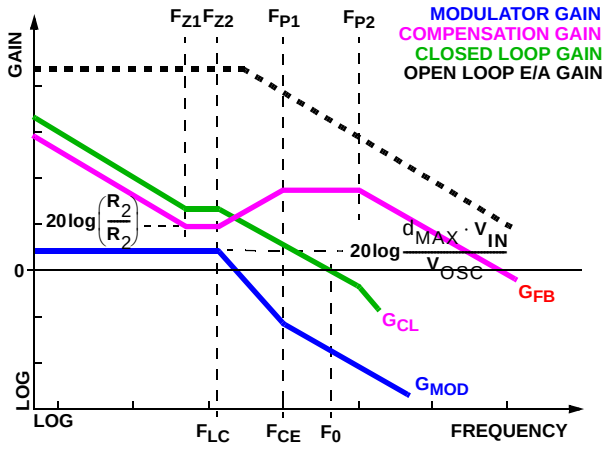


FIGURE 9. ASYMPTOTIC BODE PLOT OF CONVERTER GAIN

A stable control loop has a gain crossing with close to a -20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin. The mathematical model presented makes a number of approximations and is generally not accurate at frequencies approaching or exceeding half the switching frequency. When designing compensation networks, select target crossover frequencies in the range of 10% to 30% of the per-channel switching frequency, F_{SW}.

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to create a multiphase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced below. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts for all common microprocessor applications.

MOSFETs

Given the fixed switching frequency of the ISL8101 and the integrated output drives, the selection of MOSFETs revolves closely around the current each MOSFET is required to conduct, the capability of the devices to dissipate heat, as well as the characteristics of available heat sinking. Since the ISL8101 drives the MOSFETs with 5V, the selection of appropriate MOSFETs should be done by comparing and evaluating their characteristics at this specific V_{GS} bias voltage.

LOWER MOSFET POWER CALCULATION

Since virtually all of the heat loss in the lower MOSFET is conduction loss (due to current conducted through the channel resistance, $r_{DS(ON)}$), a quick approximation for heat

dissipated in the lower MOSFET can be found in Equation 15.

$$P_{LMOS1} = r_{DS(ON)}\left[\left(\frac{I_{OUT}}{2}\right)^2(1-D) + \frac{I_{L,P\text{-}P}^2(1-D)}{12}\right] \quad \text{(EQ. 15)}$$

where: I_M is the maximum continuous output current, $I_{L,P\text{-}P}$ is the peak-to-peak inductor current, and D is the duty cycle (approximately V_{OUT}/V_{IN}).

An additional term can be added to the lower-MOSFET loss equation to account for additional loss accrued during the dead time when inductor current is flowing through the lower-MOSFET body diode. This term is dependent on the diode forward voltage at I_M, $V_{D(ON)}$; the switching frequency, f_S; and the length of dead times, t_{d1} and t_{d2}, at the beginning and the end of the lower-MOSFET conduction interval, respectively.

$$P_{LMOS2} = V_{D(ON)}f_S\left[\left(\frac{I_{OUT}}{2} + \frac{I_{P\text{-}P}}{2}\right)t_{d1} + \left(\frac{I_{OUT}}{2} - \frac{I_{P\text{-}P}}{2}\right)t_{d2}\right] \quad \text{(EQ. 16)}$$

Equation 16 assumes the current through the lower MOSFET is always positive; if so, the total power dissipated in each lower MOSFET is approximated by the summation of P_{LMOS1} and P_{LMOS2}.

UPPER MOSFET POWER CALCULATION

In addition to $r_{DS(ON)}$ losses, a large portion of the upper MOSFET losses are switching losses, due to currents conducted through the device while the input voltage is present as V_{DS}. Upper MOSFET losses can be divided into separate components, separating the upper MOSFET switching losses, the lower MOSFET body diode reverse recovery charge loss, and the upper MOSFET $r_{DS(ON)}$ conduction loss.

In most typical circuits, when the upper MOSFET turns off, it continues to conduct the inductor current until the voltage at the phase node falls below ground. Once the lower MOSFET begins conducting (via its body diode or enhancement channel), the current in the upper MOSFET falls to zero. In the following equation, the required time for this commutation is t_1 and the associated power loss is $P_{UMOS,1}$.

$$P_{UMOS,1} \approx V_{IN}\left(\frac{I_{OUT}}{N} + \frac{I_{L,P\text{-}P}}{2}\right)\left(\frac{t_1}{2}\right)f_S \quad \text{(EQ. 17)}$$

Similarly, the upper MOSFET begins conducting as soon as it begins turning on. Assuming the inductor current is in the positive domain, the upper MOSFET sees approximately the input voltage applied across its drain and source terminals, while it turns on and starts conducting the inductor current.

This transition occurs over a time t_2, and the approximate the power loss is $P_{UMOS,2}$.

$$P_{UMOS,2} \approx V_{IN}\left(\frac{I_{OUT}}{N} - \frac{I_{L,P\text{-}P}}{2}\right)\left(\frac{t_2}{2}\right)f_S \quad \text{(EQ. 18)}$$

A third component involves the lower MOSFET's reverse-recovery charge, Q_{RR}. Since the lower MOSFET's body diode conducts the full inductor current before it has fully switched to the upper MOSFET, the upper MOSFET has to provide the charge required to turn off the lower MOSFET's body diode. This charge is conducted through the upper MOSFET across VIN, the power dissipated as a result, $P_{UMOS,3}$ can be approximated as shown in Equation 19.

$$P_{UMOS,3} = V_{IN}Q_{rr}f_S \quad \text{(EQ. 19)}$$

Lastly, the conduction loss part of the upper MOSFET's power dissipation, $P_{UMOS,4}$, can be calculated using Equation 20.

$$P_{UMOS,4} = r_{DS(ON)} \cdot d \cdot \left[\left(\frac{I_{OUT}}{N}\right)^2 + \frac{I_{P\text{-}P}^2}{12}\right] \quad \text{(EQ. 20)}$$

In this case, of course, $r_{DS(ON)}$ is the ON-resistance of the upper MOSFET.

The total power dissipated by the upper MOSFET at full load can be approximated as the summation of these results. Since the power equations depend on MOSFET parameters, choosing the correct MOSFETs can be an iterative process that involves repetitively solving the loss equations for different MOSFETs and different switching frequencies until converging upon the best solution.

OUTPUT FILTER DESIGN

The output inductors and the output capacitor bank together form a low-pass filter responsible for smoothing the square wave voltage at the phase nodes. Additionally, the output capacitors must also provide the energy required by a fast transient load during the short interval of time required by the controller and power train to respond. Because it has a low bandwidth compared to the switching frequency, the output filter limits the system transient response leaving the output capacitor bank to supply the load current or sink the inductor currents, all while the current in the output inductors increases or decreases to meet the load demand.

In high-speed converters, the output capacitor bank is amongst the costlier (and often the physically largest) parts of the circuit. Output filter design begins with consideration of the critical load parameters: maximum size of the load step, ΔI, the load-current slew rate, di/dt, and the maximum allowable output voltage deviation under transient loading, ΔV_{MAX}. Capacitors are characterized according to their capacitance, ESR, and ESL (equivalent series inductance).

At the beginning of the load transient, the output capacitors supply all of the transient current. The output voltage will initially deviate by an amount approximated by the voltage drop across the ESL. As the load current increases, the voltage drop across the ESR increases linearly until the load current reaches its final value. The capacitors selected must have sufficiently low ESL and ESR so that the total output-voltage deviation is less than the allowable maximum. Neglecting the contribution of inductor current and regulator response, the output voltage initially deviates according to Equation 21.

$$\Delta V \approx (ESL)\frac{di}{dt} + (ESR)\Delta I \quad \text{(EQ. 21)}$$

The filter capacitor must have sufficiently low ESL and ESR so that $\Delta V < \Delta V_{MAX}$.

Most capacitor solutions rely on a mixture of high-frequency capacitors with relatively low capacitance in combination with bulk capacitors having high capacitance but limited high-frequency performance. Minimizing the ESL of the high-frequency capacitors allows them to support the output voltage as the current increases. Minimizing the ESR of the bulk capacitors allows them to supply the increased current with less output voltage deviation.

The ESR of the bulk capacitors is also responsible for the majority of the output-voltage ripple. As the bulk capacitors sink and source the inductor ac ripple current, a voltage develops across the bulk-capacitor ESR equal to I_{P-P}. Thus, once the output capacitors are selected and a maximum allowable ripple voltage, $V_{P-P(MAX)}$, is determined from an analysis of the available output voltage budget. Equation 22 can be used to determine a lower limit on the output inductance.

$$L \geq ESR \cdot \frac{(V_{IN} - 2 \cdot V_{OUT}) \cdot V_{OUT}}{f_S \cdot V_{IN} \cdot V_{P-P(MAX)}} \quad \text{(EQ. 22)}$$

Since the capacitors are supplying a decreasing portion of the load current while the regulator recovers from the transient, the capacitor voltage becomes slightly depleted. The output inductors must be capable of assuming the entire load current before the output voltage decreases more than ΔV_{MAX}. This places an upper limit on inductance.

$$L \leq \frac{4 \cdot C \cdot V_{OUT}}{(\Delta I)^2} \cdot (\Delta V_{MAX} - \Delta I \cdot ESR) \quad \text{(EQ. 23)}$$

While Equation 23 addresses the leading edge, Equation 24 gives the upper limit on L for cases where the trailing edge of the current transient causes a greater output voltage deviation than the leading edge.

$$L \leq \frac{2.5 \cdot C}{(\Delta I)^2} \cdot (\Delta V_{MAX} - \Delta I \cdot ESR) \cdot (V_{IN} - V_O) \quad \text{(EQ. 24)}$$

Normally, the trailing edge dictates the selection of L, since duty cycles are usually less than 50%. Nevertheless, both inequalities should be evaluated, and L should be selected based on the lower of the two results. In all equations in this paragraph, L is the per-channel inductance and C is the total output bulk capacitance.

LAYOUT CONSIDERATIONS

MOSFETs switch very fast and efficiently. The speed with which the current transitions from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit and lead to device overvoltage stress. Careful component layout and printed circuit design minimizes the voltage spikes in the converter. Consider, as an example, the turn-off transition of the upper PWM MOSFET. Prior to turn-off, the upper MOSFET was carrying channel current. During the turnoff, current stops flowing in the upper MOSFET and is picked up by the lower MOSFET. Any inductance in the switched current path generates a large voltage spike during the switching interval. Careful component selection, tight layout of the critical components, and short, wide circuit traces minimize the magnitude of voltage spikes.

There are two sets of critical components in a DC/DC converter using a ISL8101 controller. The power components are the most critical because they switch large amounts of energy. Next are small signal components that connect to sensitive nodes or supply critical bypassing current and signal coupling.

Note that as the ISL8101 does not allow external adjustment of the channel-to-channel current balancing (current information is multiplexed across a single R_{ISEN} resistor), it is important to have a symmetrical layout, preferably with the controller equidistantly located from the two power trains it controls. Equally important are the gate drive lines (UGATE, LGATE, PHASE): since they drive the power train MOSFETs using short, high current pulses, it is important to size them accordingly and reduce their overall impedance. Equidistant placement of the controller to the two power trains also helps keeping these traces equally long (equal impedances, resulting in similar driving of both sets of MOSFETs).

The power components should be placed first. Locate the input capacitors close to the power switches. Minimize the length of the connections between the input capacitors, C_{IN}, and the power switches. Locate the output inductors and output capacitors between the MOSFETs and the load. Locate the high-frequency decoupling capacitors (ceramic) as close as practicable to the decoupling target, making use of the shortest connection paths to any internal planes, such as vias to GND immediately next, or even onto the capacitor solder pad.

The critical small components include the bypass capacitors for VCC and PVCC. Locate the bypass capacitors, C_{BP},

close to the device. It is especially important to locate the components associated with the feedback circuit close to their respective controller pins, since they belong to a high-impedance circuit loop, sensitive to EMI pick-up. It is important to place the R_{ISEN} resistor close to the respective terminal of the ISL8101.

A multi-layer printed circuit board is recommended. Figure 10 shows the connections of the critical components for one output channel of the converter. Note that capacitors C_{xxIN} and C_{xxOUT} could each represent numerous physical capacitors. Dedicate one solid layer, usually the one underneath the component side of the board, for a ground plane and make all critical component ground connections with vias to this layer. Dedicate another solid layer as a power plane and break this plane into smaller islands of common voltage levels. Keep the metal runs from the PHASE terminal to inductor L_{OUT} short. The power plane should support the input power and output power nodes. Use copper filled polygons on the top and bottom circuit layers for the phase nodes. Use the remaining printed circuit layers for small signal wiring. The wiring traces from the IC to the MOSFETs' gates and sources should be sized to carry at least one ampere of current (0.02" to 0.05").

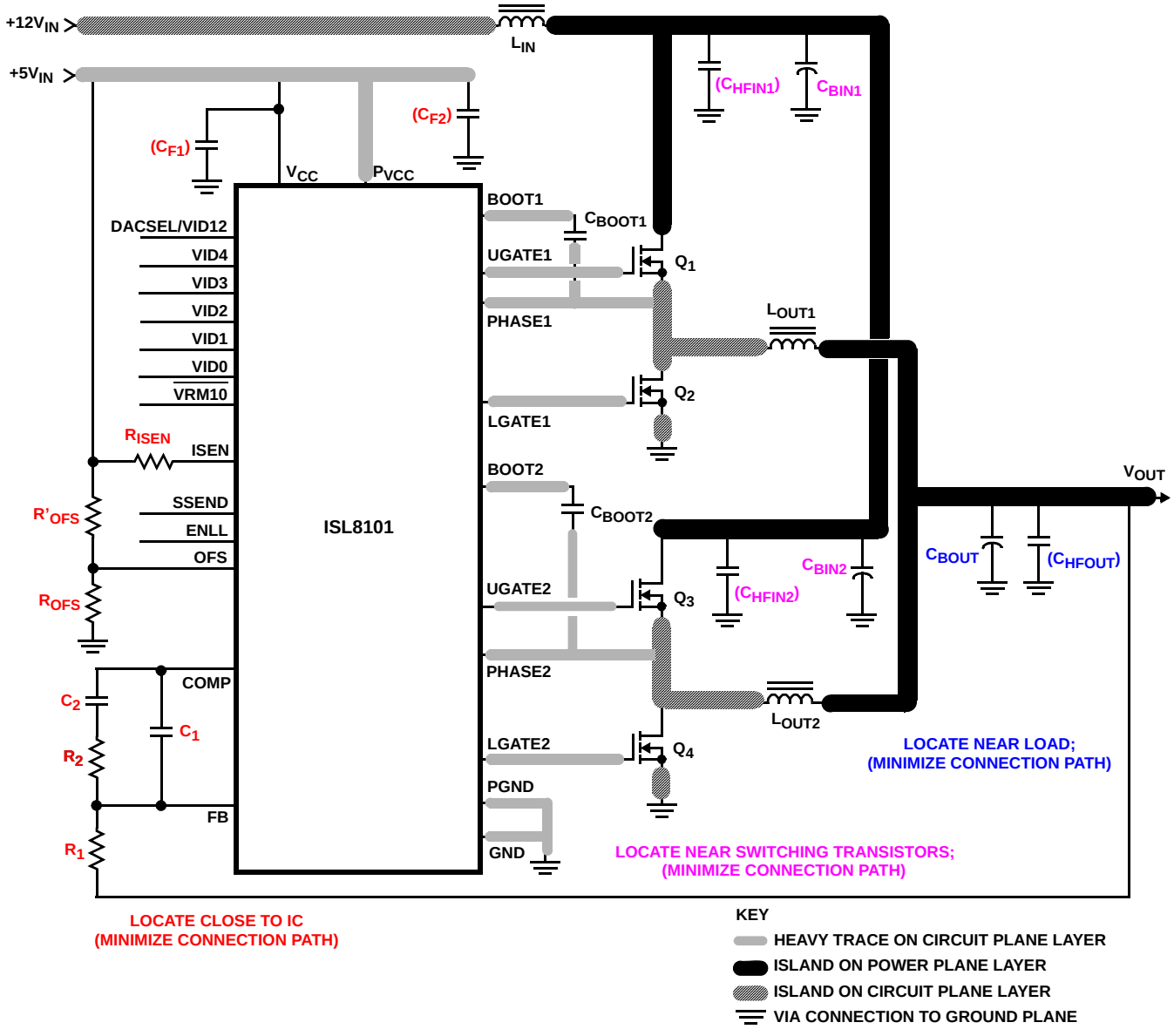


FIGURE 10. PRINTED CIRCUIT BOARD POWER PLANES AND ISLANDS

Component Selection Guidelines

Output Capacitor Selection

The output capacitor is selected to meet both the dynamic load requirements and the voltage ripple requirements. The load transient a microprocessor impresses is characterized by high slew rate (di/dt) current demands. In general, multiple high quality capacitors of different size and dielectric are paralleled to meet the design constraints.

Should the load be characterized by high slew rates, attention should be particularly paid to the selection and placement of high-frequency decoupling capacitors (MLCCs, typically multi-layer ceramic capacitors). High frequency capacitors supply the initially transient current and slow the load rate-of-change seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the ESR (effective series resistance) and capacitance requirements.

High frequency decoupling capacitors should be placed as close to the power pins of the load, or for that reason, to any decoupling target they are meant for, as physically possible. Attention should be paid as not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load on specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR determines the output ripple voltage and the initial voltage drop following a high slew-rate transient's edge. In most cases, multiple capacitors of small case size perform better than a single large case capacitor.

Bulk capacitor choices include aluminum electrolytic, OS-Con, Tantalum and even ceramic dielectrics. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the equivalent series inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Consult the capacitor manufacturer and/or measure the capacitor's impedance with frequency to help select a suitable component.

Output Inductor Selection

One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. In a multiphase converter, small inductors reduce the response time with less impact to the total output ripple current (as compared to single-phase converters).

The output inductor of each power channel controls the ripple current. The control IC is stable for channel ripple current (peak-to-peak) up to twice the average current. A single channel's ripple current is approximated by using Equation 25.

$$I_{L,P\text{-}P} = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot L} \times \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 25)}$$

The current from multiple channels tend to cancel each other and reduce the total ripple current. The total output ripple current can be determined using the curve in Figure 11; it provides the total ripple current as a function of duty cycle and number of active channels, normalized to the parameter K_{NORM} at zero duty cycle (see Equation 26).

$$K_{NORM} = \frac{V_{OUT}}{L \cdot F_{SW}} \quad \text{(EQ. 26)}$$

where L is the channel inductor value.

Find the intersection of the active channel curve and duty cycle for your particular application. The resulting ripple current multiplier from the y-axis is then multiplied by the normalization factor, K_{NORM}, to determine the total output ripple current for the given application (see Equation 27).

$$\Delta I_{TOTAL} = K_{NORM} \cdot K_{CM} \quad \text{(EQ. 27)}$$

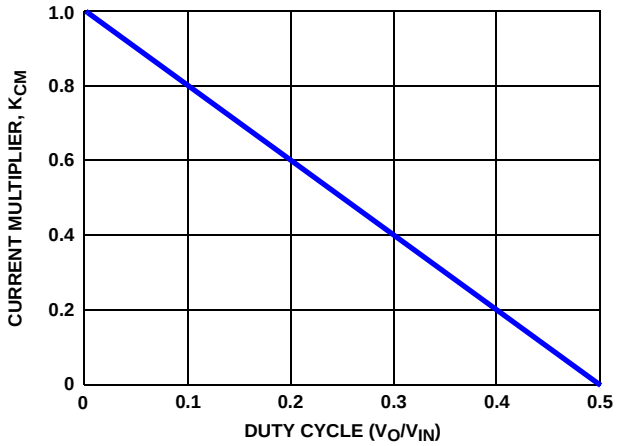


FIGURE 11. RIPPLE CURRENT vs DUTY CYCLE

Input Capacitor Selection

The important parameters for the bulk input capacitors are the voltage rating and the RMS current rating. For reliable operation, select bulk input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25x greater than the maximum input voltage. The input RMS current required for a multiphase converter can be approximated with the aid of Figure 12.

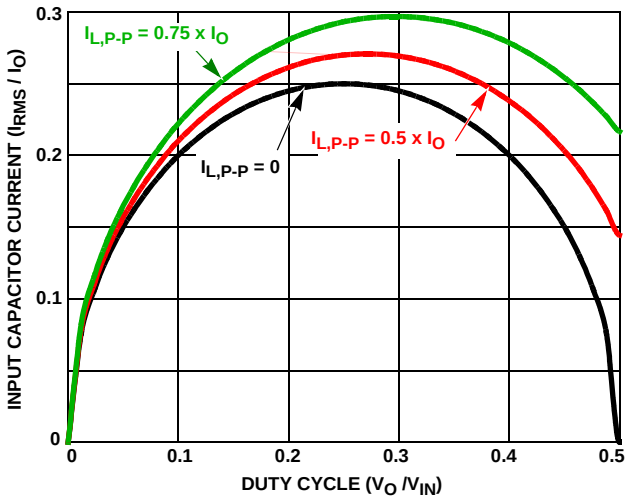


FIGURE 12. NORMALIZED INPUT RMS CURRENT vs DUTY CYCLE FOR A 2-PHASE CONVERTER

As the input capacitors are responsible for sourcing the AC component of the input current flowing into the upper MOSFETs, their RMS current capacity must be sufficient to handle the AC component of the current drawn by the upper MOSFETs. Figure 12 can be used to determine the input-capacitor RMS current function of duty cycle, maximum sustained output current (I_O), and the ratio of the peak-to-peak inductor current ($I_{L,P-P}$) to the maximum sustained load current, I_O. Figure 12 can also be used as a reference demonstrating the dramatic reduction in input capacitor RMS current in a 2-phase DC/DC converter, as compared to a single-phase regulator.

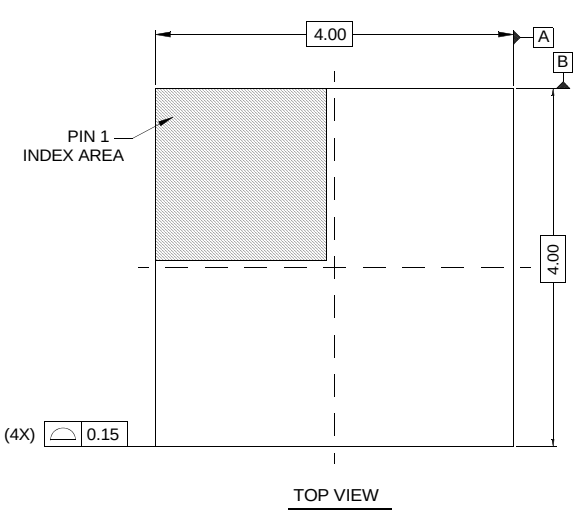
Use a mix of input bypass capacitors to control the input voltage ripple. Use ceramic capacitance for the high frequency decoupling and bulk capacitors to supply the RMS current. Minimize the connection path inductance of the high frequency decoupling ceramic capacitors (from drain of upper MOSFET to source of lower MOSFET).

For bulk capacitance, several electrolytic or high-capacity MLC capacitors may be needed. For surface mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor surge current rating. These capacitors must be capable of handling the surge-current at power-up.

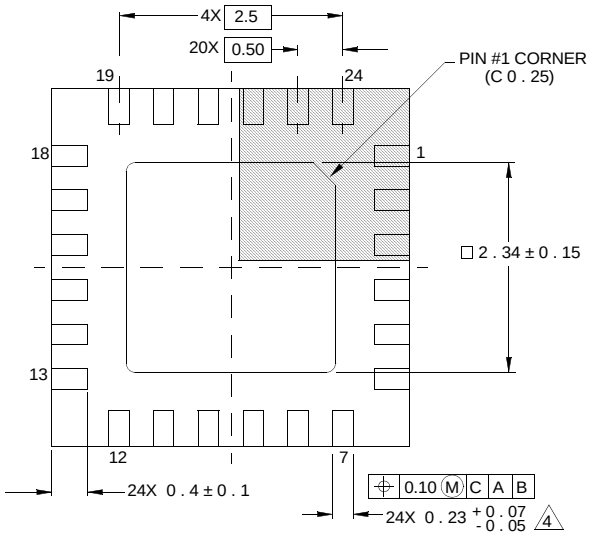
Package Outline Drawing

L24.4x4B

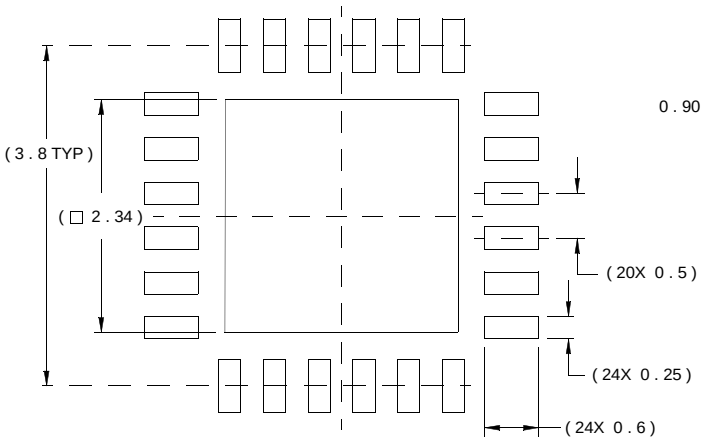
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



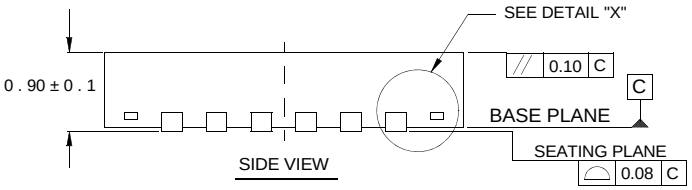
TOP VIEW



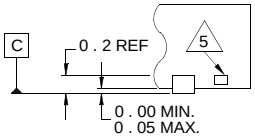
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.