

Unidirectional Measurement Current-Shunt Monitor with Dual Comparators

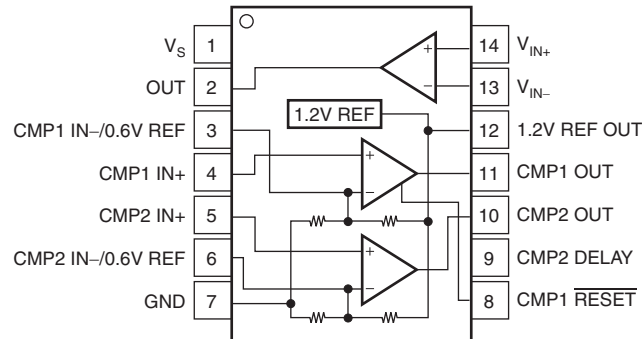
Check for Samples: [INA203-Q1](#)

FEATURES

- **Qualified for Automotive Applications**
- **Complete Current Sense Solution**
- **Dual Comparators:**
 - **Comparator 1 with Latch**
 - **Comparator 2 with Optional Delay**
- **Common-Mode Range: –16V to +80V**
- **High Accuracy: 3.5% (max) Over Temperature**
- **Bandwidth: 500kHz**
- **Quiescent Current: 1.8mA**
- **Latch-Up Performance Meets 100 mA Per AEC-Q100, Level I**
- **Packages: SO-14, TSSOP-14, MSOP-10**

APPLICATIONS

- **Automotive**
- **Power Management**
- **Battery Chargers**

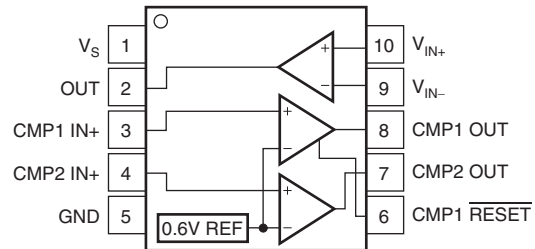


DESCRIPTION

The INA203-Q1 is a unidirectional current-shunt monitor with voltage output, dual comparators, and voltage reference. The INA203-Q1 can sense drops across shunts at common-mode voltages from –16V to +80V. The INA203-Q1 is available with three output voltage scales: 20V/V, 50V/V, and 100V/V, with up to 500kHz bandwidth.

The INA203-Q1 also incorporates two open-drain comparators with internal 0.6V references. On 14-pin versions, the comparator references can be overridden by external inputs. Comparator 1 includes a latching capability, and Comparator 2 has a user-programmable delay. 14-pin versions also provide a 1.2V reference output.

The INA203-Q1 operates from a single +2.7V to +18V supply. It is specified over the extended operating temperature range of –40°C to +125°C.



RELATED PRODUCTS

FEATURES	PRODUCT
Variant of INA203-Q1–INA205 Comparator 2 polarity	INA206–INA208
Current-shunt monitor with single Comparator and V _{REF}	INA200–INA202
Current-shunt monitor only	INA193–INA198
Current-shunt monitor with split stages for filter options	INA270–INA271



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Table 1. ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE		ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC-8	Reel of 2000	INA203AQPWRQ1	I203AQ

- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

		VALUE	UNIT
Supply Voltage, V ₊		18	V
Current-Shunt Monitor Analog Inputs, V _{IN+} and V _{IN-}	Differential (V _{IN+}) – (V _{IN-})	-18 to +18	V
	Common-Mode	-16 to +80	V
Comparator Analog Input and Reset Pins		GND – 0.3 to (V ₊) + 0.3	V
Analog Output, Out Pin		GND – 0.3 to (V ₊) + 0.3	V
Comparator Output, Out Pin		GND – 0.3 to 18	V
V _{REF} and CMP2 Delay Pin		GND – 0.3 to 10	V
Input Current Into Any Pin		5	mA
Storage Temperature		-65 to +150	°C
Junction Temperature		+150	°C
ESD Ratings	Human Body Model (HBM)	2000	V
	Charged Device Model (CDM)	500	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not supported.

ELECTRICAL CHARACTERISTICS: CURRENT-SHUNT MONITOR
Boldface limits apply over the specified temperature range: $T_A = -40^\circ\text{C}$ to $+125^\circ\text{C}$.

At $T_A = +25^\circ\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, $V_{SENSE} = 100\text{mV}$, $R_L = 10\text{k}\Omega$ to GND, $R_{PULL-UP} = 5.1\text{k}\Omega$ each connected from CMP1 OUT and CMP2 OUT to V_S , and CMP1 IN+ = 1V and CMP2 IN- = GND, unless otherwise noted.

CURRENT-SHUNT MONITOR PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNIT	
INPUT							
Full-Scale Sense Input Voltage	V_{SENSE}	$V_{SENSE} = V_{IN+} - V_{IN-}$		0.15	$(V_S - 0.25)/\text{Gain}$	V	
Common-Mode Input Range	V_{CM}		-16		80	V	
Common-Mode Rejection Ratio	CMRR	$V_{CM} = -16\text{V}$ to $+80\text{V}$	80	100		dB	
		$V_{CM} = +12\text{V}$ to $+80\text{V}$	100	123		dB	
Offset Voltage, RTI ⁽¹⁾	V_{OS}			± 0.5	± 2.5	mV	
		$+25^\circ\text{C}$ to $+125^\circ\text{C}$				± 3	mV
		-40°C to $+25^\circ\text{C}$				± 3.5	mV
vs Temperature	dV_{OS}/dT	T_{MIN} to T_{MAX}		5		$\mu\text{V}/^\circ\text{C}$	
vs Power Supply	PSR	$V_{OUT} = 2\text{V}$, $V_{CM} = +18\text{V}$		2.5	100	$\mu\text{V}/\text{V}$	
Input Bias Current, V_{IN-} Pin	I_B			± 9	± 16	μA	
OUTPUT ($V_{SENSE} \geq 20\text{mV}$)							
Gain	G			20		V/V	
Gain Error		$V_{SENSE} = 20\text{mV}$ to 100mV		± 0.2	± 1	%	
Over Temperature		$V_{SENSE} = 20\text{mV}$ to 100mV			± 2	%	
Total Output Error ⁽²⁾		$V_{SENSE} = 120\text{mV}$, $V_S = +16\text{V}$		± 0.75	± 2.2	%	
Over Temperature		$V_{SENSE} = 120\text{mV}$, $V_S = +16\text{V}$			± 3.5	%	
Nonlinearity Error ⁽³⁾		$V_{SENSE} = 20\text{mV}$ to 100mV		± 0.002		%	
Output Impedance, Pin 2	R_O			1.5		Ω	
Maximum Capacitive Load		No Sustained Oscillation		10		nF	
OUTPUT ($V_{SENSE} < 20\text{mV}$)⁽⁴⁾							
		$-16\text{V} \leq V_{CM} < 0\text{V}$		300		mV	
		$0\text{V} \leq V_{CM} \leq V_S$, $V_S = 5\text{V}$			0.4	V	
		$V_S < V_{CM} \leq 80\text{V}$		300		mV	
VOLTAGE OUTPUT⁽⁵⁾							
Output Swing to the Positive Rail		$V_{IN-} = 11\text{V}$, $V_{IN+} = 12\text{V}$		$(V+) - 0.15$	$(V+) - 0.25$	V	
Output Swing to GND ⁽⁶⁾		$V_{IN-} = 0\text{V}$, $V_{IN+} = -0.5\text{V}$		$(V_{GND}) + 0.004$	$(V_{GND}) + 0.05$	V	
FREQUENCY RESPONSE							
Bandwidth	BW	$C_{LOAD} = 5\text{pF}$		500		kHz	
Phase Margin		$C_{LOAD} < 10\text{nF}$		40		Degrees	
Slew Rate	SR			1		V/ μs	
Settling Time (1%)		$V_{SENSE} = 10\text{mV}_{PP}$ to 100mV_{PP} , $C_{LOAD} = 5\text{pF}$		2		μs	
NOISE, RTI							
Output Voltage Noise Density				40		$\text{nV}/\sqrt{\text{Hz}}$	

(1) Offset is extrapolated from measurements of the output at 20mV and 100mV V_{SENSE} .

(2) Total output error includes effects of gain error and V_{OS} .

(3) Linearity is best fit to a straight line.

(4) For details on this region of operation, see the [Accuracy Variations](#) section in the [Applications Information](#).

(5) See Typical Characteristic curve *Positive Output Voltage Swing vs Output Current* (Figure 8).

(6) Specified by design; not production tested.

ELECTRICAL CHARACTERISTICS: COMPARATOR

Boldface limits apply over the specified temperature range: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $V_S = +12\text{V}$, $V_{\text{CM}} = +12\text{V}$, $V_{\text{SENSE}} = 100\text{mV}$, $R_L = 10\text{k}\Omega$ to GND, and $R_{\text{PULL-UP}} = 5.1\text{k}\Omega$ each connected from CMP1 OUT and CMP2 OUT to V_S , unless otherwise noted.

COMPARATOR PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE					
Offset Voltage	Comparator Common-Mode Voltage = Threshold Voltage		2		mV
Offset Voltage Drift, Comparator 1			± 2		$\mu\text{V}/^{\circ}\text{C}$
Offset Voltage Drift, Comparator 2			+5.4		$\mu\text{V}/^{\circ}\text{C}$
Threshold	Rising Edge on Non-Inverting input, $T_A = +25^{\circ}\text{C}$	590	608	620	mV
Over Temperature		586		625	mV
Hysteresis ⁽¹⁾ , CMP1	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		-8		mV
Hysteresis ⁽¹⁾ , CMP2	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		8		mV
INPUT BIAS CURRENT⁽²⁾					
CMP1 IN+, CMP2 IN+			0.005	10	nA
vs Temperature				15	nA
INPUT IMPEDANCE					
Pins 3 and 6 (14-pin packages only)			10		k Ω
INPUT RANGE					
CMP1 IN+ and CMP2 IN+			0V to $V_S - 1.5\text{V}$		V
Pins 3 and 6 (14-pin packages only) ⁽³⁾			0V to $V_S - 1.5\text{V}$		V
OUTPUT					
Large-Signal Differential Voltage Gain	CMP V_{OUT} 1V to 4V, $R_L \geq 15\text{k}\Omega$ Connected to 5V		200		V/mV
High-Level Output Current	$V_{\text{ID}} = 0.4\text{V}$, $V_{\text{OH}} = V_S$		0.0001	1	μA
Low-Level Output Voltage	$V_{\text{ID}} = -0.6\text{V}$, $I_{\text{OL}} = 2.35\text{mA}$		220	300	mV
RESPONSE TIME⁽⁴⁾					
Comparator 1	R_L to 5V, $C_L = 15\text{pF}$, 100mV Input Step with 5mV Overdrive		1.3		μs
Comparator 2	R_L to 5V, $C_L = 15\text{pF}$, 100mV Input Step with 5mV Overdrive, C_{DELAY} Pin Open		1.3		μs
RESET					
RESET Threshold ⁽⁵⁾			1.1		V
Logic Input Impedance			2		M Ω
Minimum RESET Pulse Width			1.5		μs
RESET Propagation Delay			3		μs
Comparator 2 Delay Equation ⁽⁶⁾			$C_{\text{DELAY}} = t_D/5$		μF
Comparator 2 Delay	t_D		0.5		s
					$C_{\text{DELAY}} = 0.1\mu\text{F}$

- (1) Hysteresis refers to the threshold (the threshold specification applies to a rising edge of a noninverting input) of a falling edge on the noninverting input of the comparator; refer to [Figure 1](#).
- (2) Specified by design; not production tested.
- (3) See the [Comparator Maximum Input Voltage Range](#) section in the [Applications Information](#).
- (4) The comparator response time specified is the interval between the input step function and the instant when the output crosses 1.4V.
- (5) The CMP1 RESET input has an internal 2M Ω (typical) pull-down. Leaving the CMP1 RESET open results in a LOW state, with transparent comparator operation.
- (6) The Comparator 2 delay applies to both rising and falling edges of the comparator output.

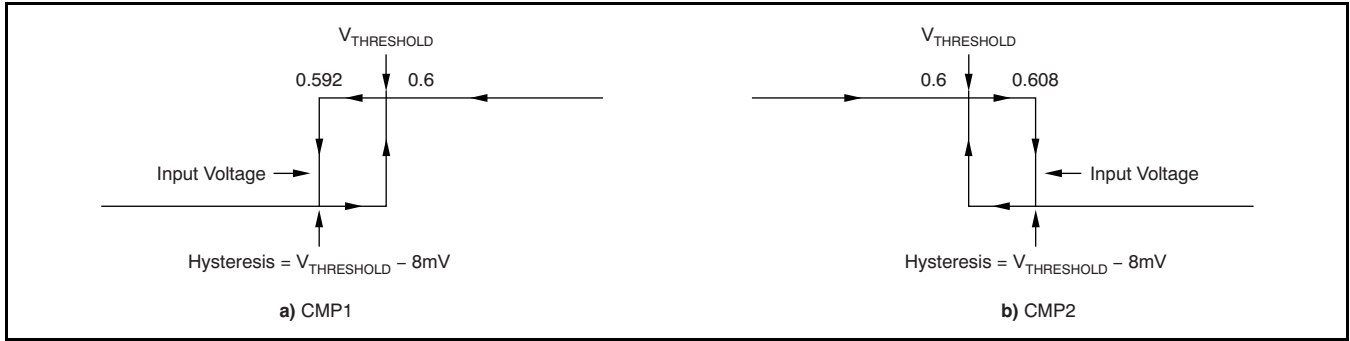


Figure 1. Comparator Hysteresis

ELECTRICAL CHARACTERISTICS: REFERENCE

Boldface limits apply over the specified temperature range: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

At $T_A = +25^{\circ}\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, $V_{SENSE} = 100\text{mV}$, $R_L = 10\text{k}\Omega$ to GND, and $R_{PULL-UP} = 5.1\text{k}\Omega$ each connected from CMP1 OUT and CMP2 OUT to V_S , unless otherwise noted.

REFERENCE PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE VOLTAGE					
1.2V _{REFOUT} Output Voltage		1.188	1.2	1.212	V
Reference Drift ⁽¹⁾	dV_{OUT}/dT $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		40	100	ppm/ $^{\circ}\text{C}$
0.6V _{REF} Output Voltage (Pins 3 and 6 of 14-pin packages only)			0.6		V
Reference Drift ⁽¹⁾	dV_{OUT}/dT $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		40	100	ppm/ $^{\circ}\text{C}$
LOAD REGULATION					
	dV_{OUT}/dI_{LOAD}				
V_{REFOUT} = 1.2V					
Sourcing	$0\text{mA} < I_{SOURCE} < 0.5\text{mA}$		0.4	2	mV/mA
Sinking	$0\text{mA} < I_{SINK} < 0.5\text{mA}$		0.4		mV/mA
LOAD CURRENT					
	I_{LOAD}		1		mA
LINE REGULATION					
	dV_{OUT}/dV_S	$2.7\text{V} < V_S < 18\text{V}$		30	$\mu\text{V}/\text{V}$
CAPACITIVE LOAD					
Reference Output Maximum Capacitive Load	No Sustained Oscillations		10		nF
OUTPUT IMPEDANCE					
Pins 3 and 6 of 14-Pin Packages Only			10		k Ω

(1) Specified by design; not production tested.

ELECTRICAL CHARACTERISTICS: GENERAL

Boldface limits apply over the specified temperature range: $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$.

All specifications at $T_A = +25^{\circ}\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, $V_{SENSE} = 100\text{mV}$, $R_L = 10\text{k}\Omega$ to GND, $R_{PULL-UP} = 5.1\text{k}\Omega$ each connected from CMP1 OUT and CMP2 OUT to V_S , and CMP1 IN+ = 1V and CMP2 IN- = GND, unless otherwise noted.

GENERAL PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY					
Operating Power Supply	V_S	+2.7		+18	V
Quiescent Current	I_Q $V_{OUT} = 2\text{V}$		1.8	2.2	mA
Over Temperature	$V_{SENSE} = 0\text{mV}$			2.8	mA
Comparator Power-On Reset Threshold ⁽¹⁾			1.5		V
TEMPERATURE					
Specified Temperature Range		-40		+125	$^{\circ}\text{C}$
Operating Temperature Range		-55		+150	$^{\circ}\text{C}$
Storage Temperature Range		-65		+150	$^{\circ}\text{C}$
Thermal Resistance	θ_{JA}				
MSOP-10 Surface-Mount			200		$^{\circ}\text{C}/\text{W}$
SO-14, TSSOP-14 Surface-Mount			150		$^{\circ}\text{C}/\text{W}$

(1) The INA203, INA204, and INA205 are designed to power-up with the comparator in a defined reset state as long as CMP1 **RESET** is open or grounded. The comparator will be in reset as long as the power supply is below the voltage shown here. The comparator assumes a state based on the comparator input above this supply voltage. If CMP1 **RESET** is high at power-up, the comparator output comes up high and requires a reset to assume a low state, if appropriate.

TYPICAL CHARACTERISTICS

All specifications at $T_A = +25^\circ\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, and $V_{SENSE} = 100\text{mV}$, unless otherwise noted.

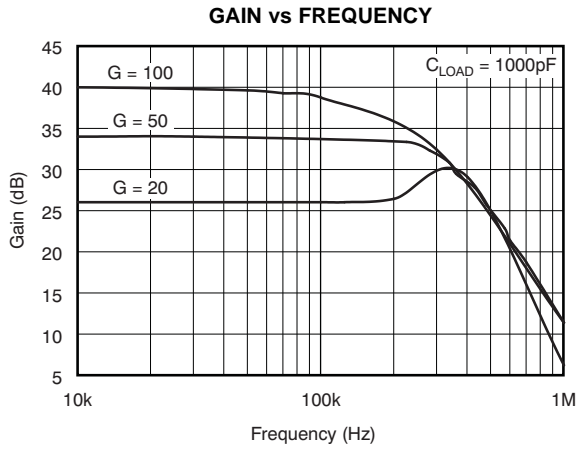


Figure 2.

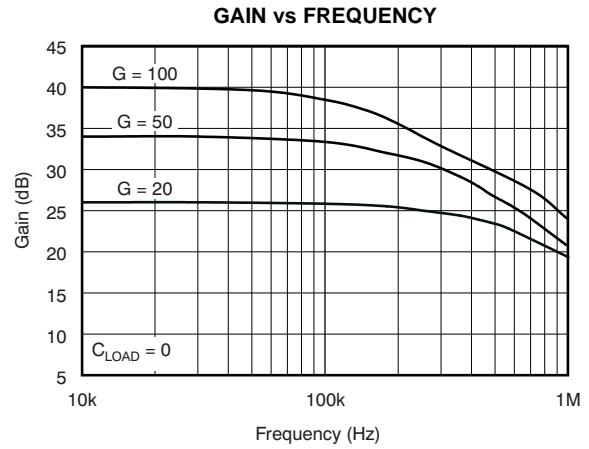


Figure 3.

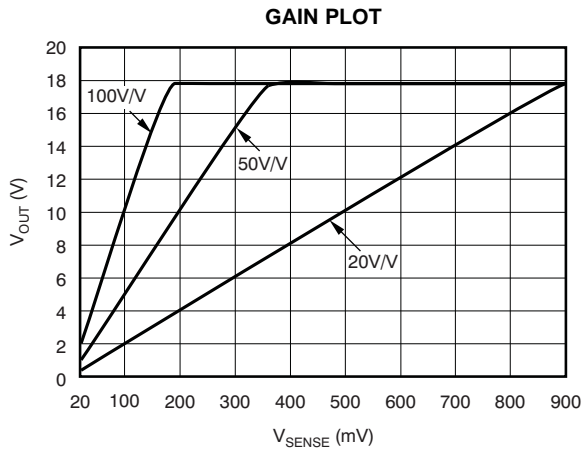


Figure 4.

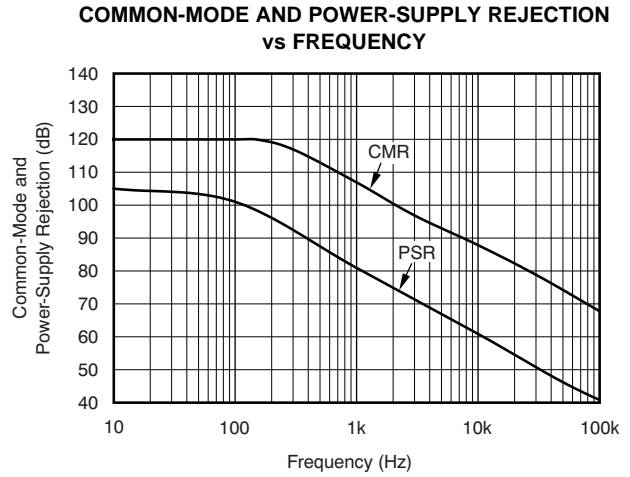


Figure 5.

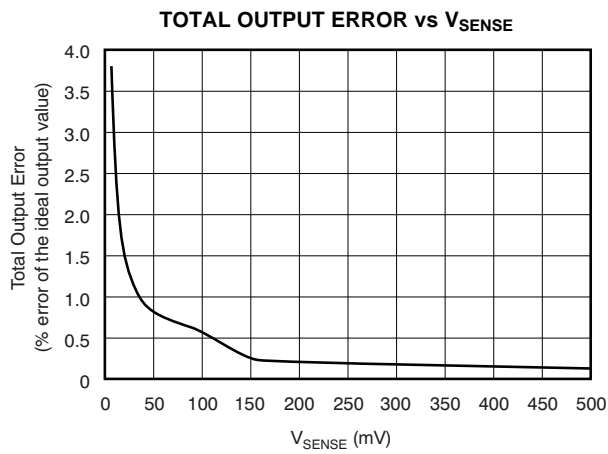


Figure 6.

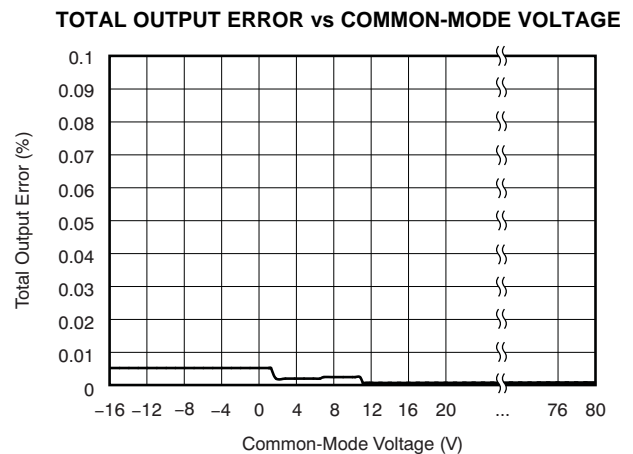


Figure 7.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = +25^\circ\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, and $V_{SENSE} = 100\text{mV}$, unless otherwise noted.

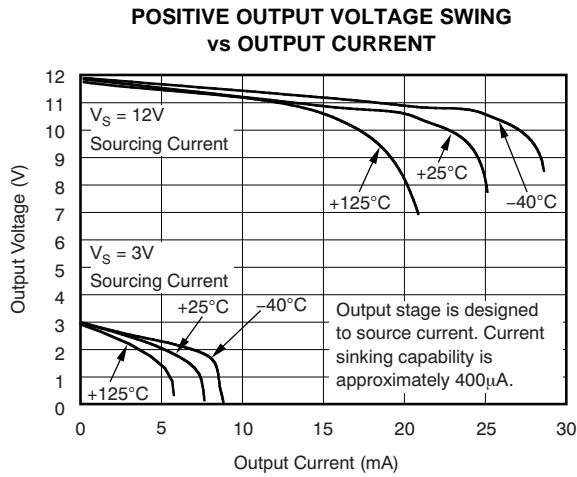


Figure 8.

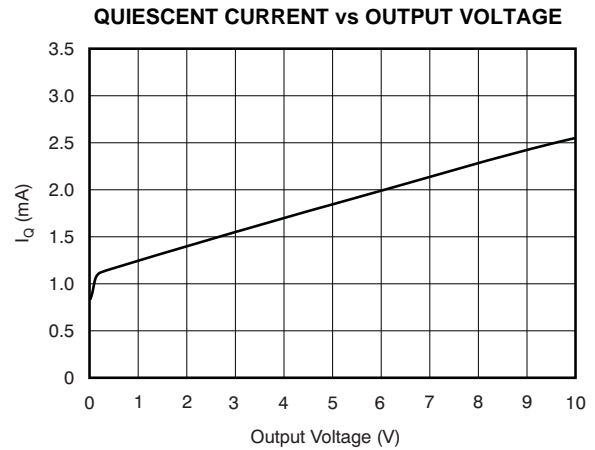


Figure 9.

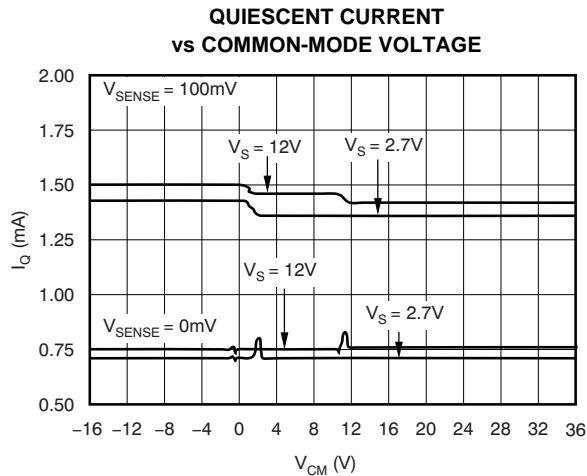


Figure 10.

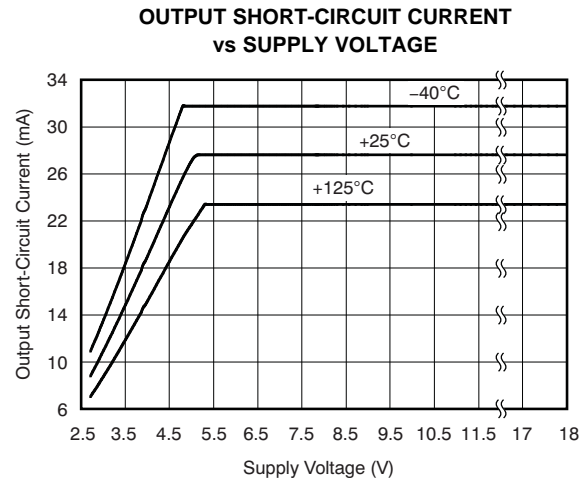


Figure 11.

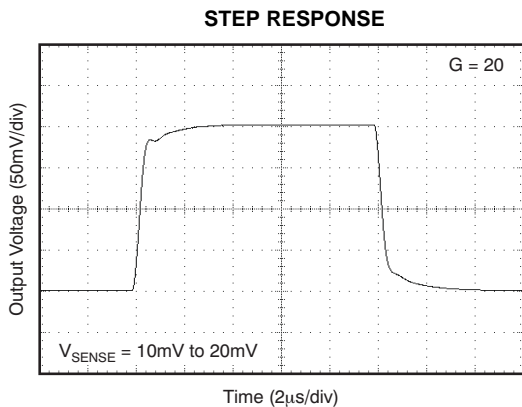


Figure 12.

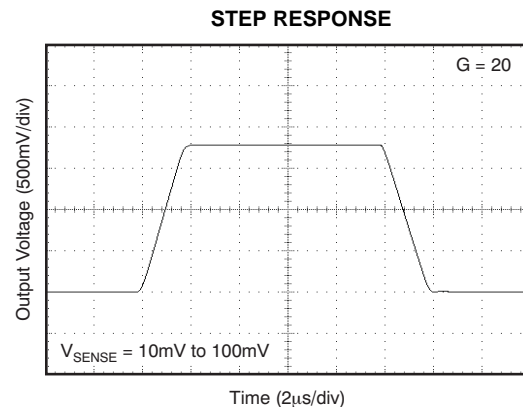


Figure 13.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = +25^\circ\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, and $V_{SENSE} = 100\text{mV}$, unless otherwise noted.

STEP RESPONSE

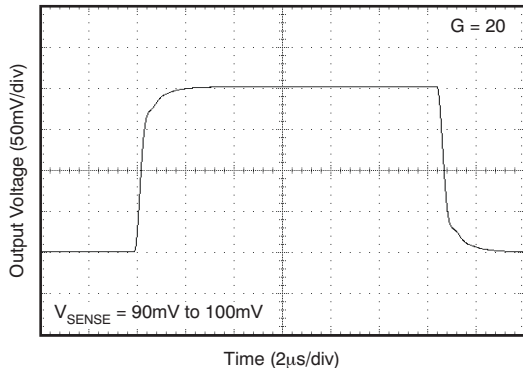


Figure 14.

STEP RESPONSE

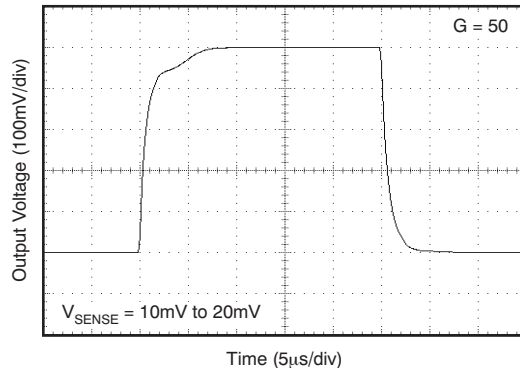


Figure 15.

STEP RESPONSE

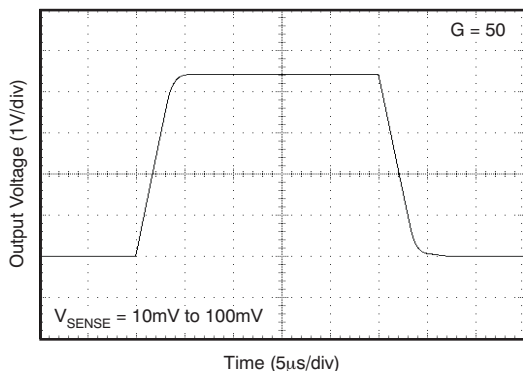


Figure 16.

STEP RESPONSE

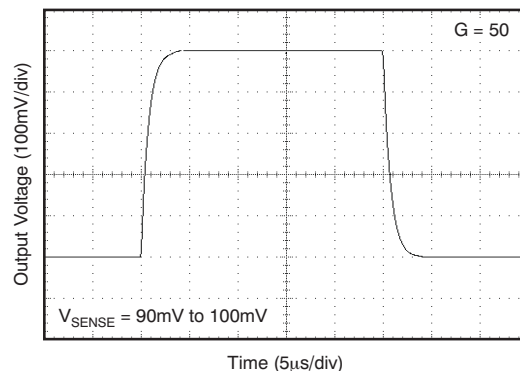


Figure 17.

STEP RESPONSE

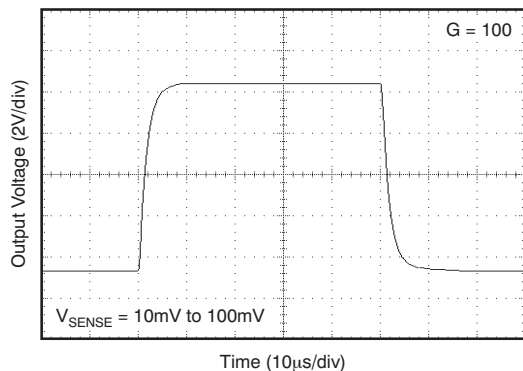


Figure 18.

COMPARATOR V_{OL} VS I_{SINK}

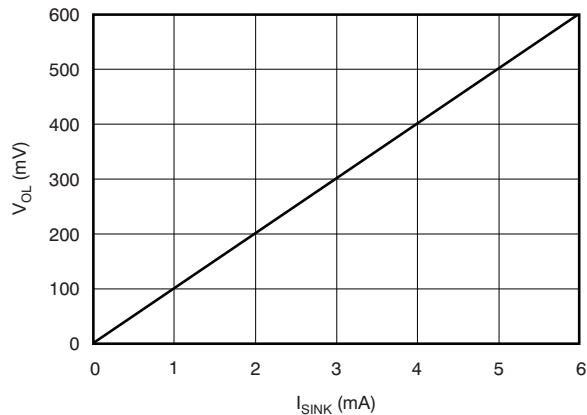


Figure 19.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = +25^\circ\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, and $V_{SENSE} = 100\text{mV}$, unless otherwise noted.

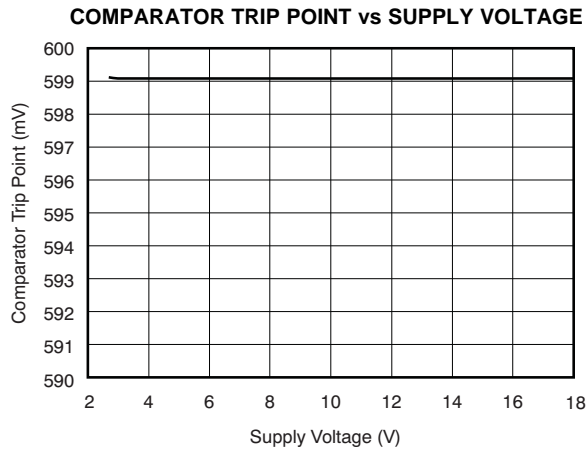


Figure 20.

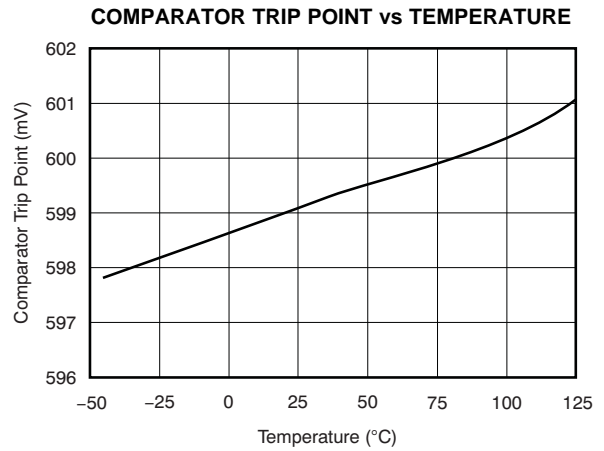


Figure 21.

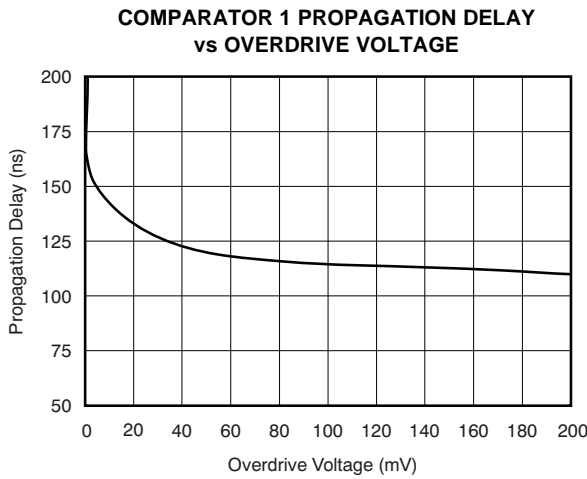


Figure 22.

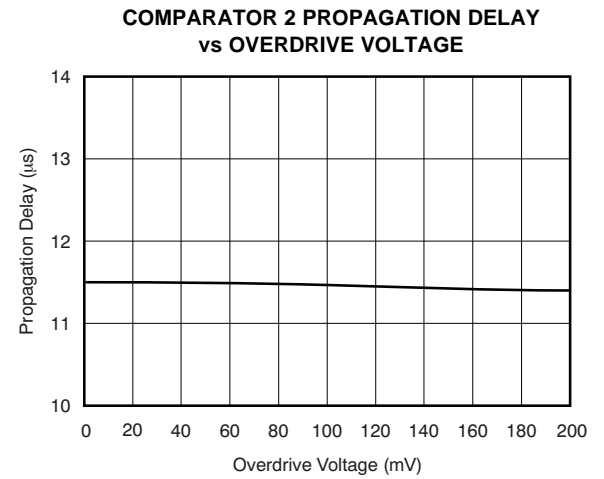


Figure 23.

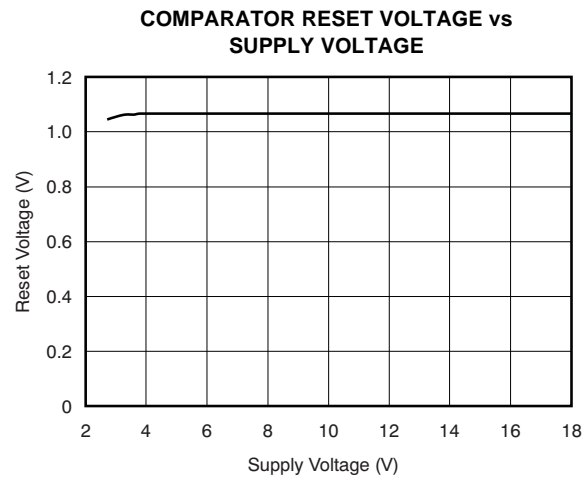


Figure 24.

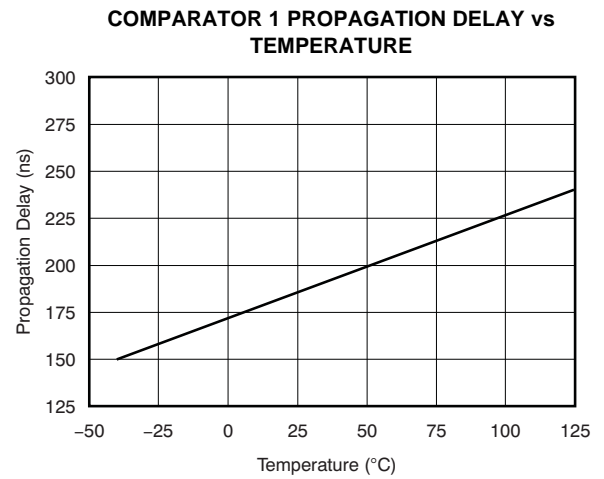


Figure 25.

TYPICAL CHARACTERISTICS (continued)

All specifications at $T_A = +25^\circ\text{C}$, $V_S = +12\text{V}$, $V_{CM} = +12\text{V}$, and $V_{SENSE} = 100\text{mV}$, unless otherwise noted.

COMPARATOR 2 PROPAGATION DELAY vs CAPACITANCE

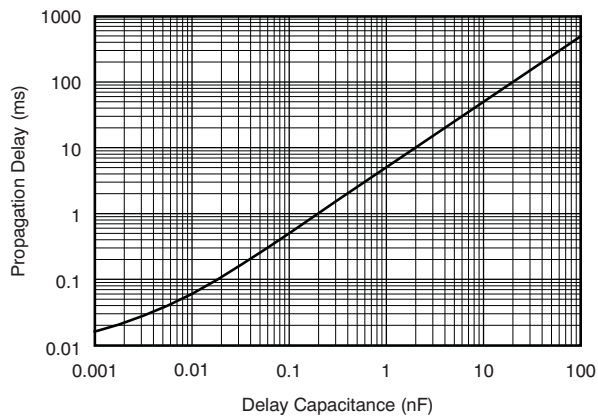


Figure 26.

COMPARATOR 1 PROPAGATION DELAY

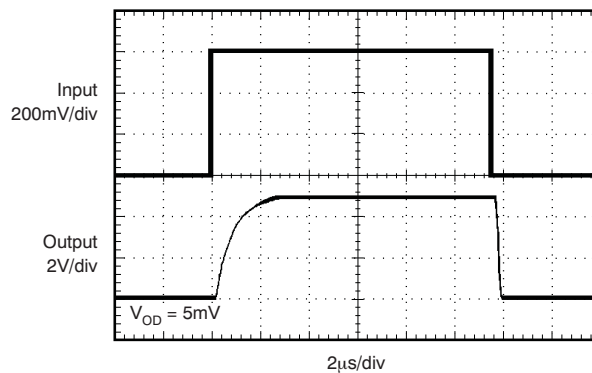


Figure 27.

COMPARATOR 2 PROPAGATION DELAY

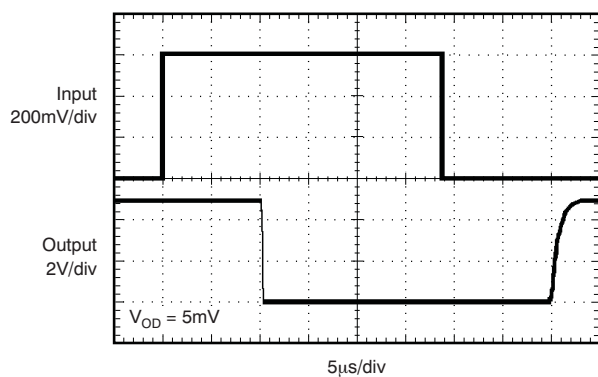


Figure 28.

REFERENCE VOLTAGE vs TEMPERATURE

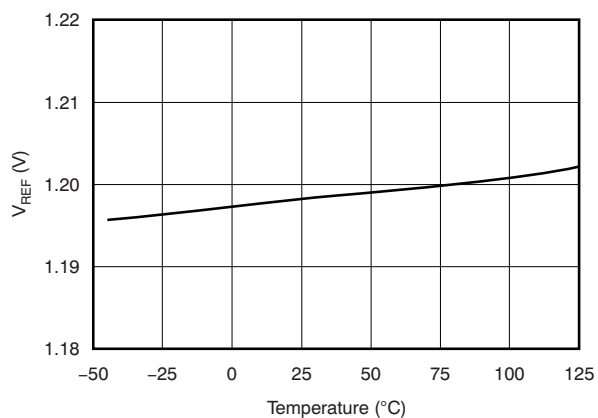


Figure 29.

APPLICATIONS INFORMATION

BASIC CONNECTIONS

Figure 30 shows the basic connections of the INA203-Q1. The input pins, V_{IN+} and V_{IN-} , should be connected as closely as possible to the shunt resistor to minimize any resistance in series with the shunt resistance.

Power-supply bypass capacitors are required for stability. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise. Connect bypass capacitors close to the device pins.

POWER SUPPLY

The input circuitry of the INA203-Q1 can accurately measure beyond the power-supply voltage, $V+$. For example, the $V+$ power supply can be 5V, whereas the load power-supply voltage is up to +80V. The output voltage range of the OUT terminal, however, is limited by the voltages on the power-supply pin.

ACCURACY VARIATIONS AS A RESULT OF V_{SENSE} AND COMMON-MODE VOLTAGE

The accuracy of the INA203-Q1 current shunt monitors is a function of two main variables: V_{SENSE} ($V_{IN+} - V_{IN-}$) and common-mode voltage, V_{CM} , relative to the supply voltage, V_S . V_{CM} is expressed as $(V_{IN+} + V_{IN-})/2$; however, in practice, V_{CM} is seen as the voltage at V_{IN+} because the voltage drop across V_{SENSE} is usually small.

This section addresses the accuracy of these specific operating regions:

- Normal Case 1: $V_{SENSE} \geq 20\text{mV}$, $V_{CM} \geq V_S$
- Normal Case 2: $V_{SENSE} \geq 20\text{mV}$, $V_{CM} < V_S$
- Low V_{SENSE} Case 1: $V_{SENSE} < 20\text{mV}$, $-16\text{V} \leq V_{CM} < 0$
- Low V_{SENSE} Case 2: $V_{SENSE} < 20\text{mV}$, $0\text{V} \leq V_{CM} \leq V_S$
- Low V_{SENSE} Case 3: $V_{SENSE} < 20\text{mV}$, $V_S < V_{CM} \leq 80\text{V}$

Normal Case 1: $V_{SENSE} \geq 20\text{mV}$, $V_{CM} \geq V_S$

This region of operation provides the highest accuracy. Here, the input offset voltage is characterized and measured using a two-step method. First, the gain is determined by Equation 1.

$$G = \frac{V_{OUT1} - V_{OUT2}}{100\text{mV} - 20\text{mV}} \tag{1}$$

where:

V_{OUT1} = Output Voltage with $V_{SENSE} = 100\text{mV}$

V_{OUT2} = Output Voltage with $V_{SENSE} = 20\text{mV}$

Then the offset voltage is measured at $V_{SENSE} = 100\text{mV}$ and referred to the input (RTI) of the current shunt monitor, as shown in Equation 2.

$$V_{OS\text{RTI}} (\text{Referred-To-Input}) = \left[\frac{V_{OUT1}}{G} \right] - 100\text{mV} \tag{2}$$

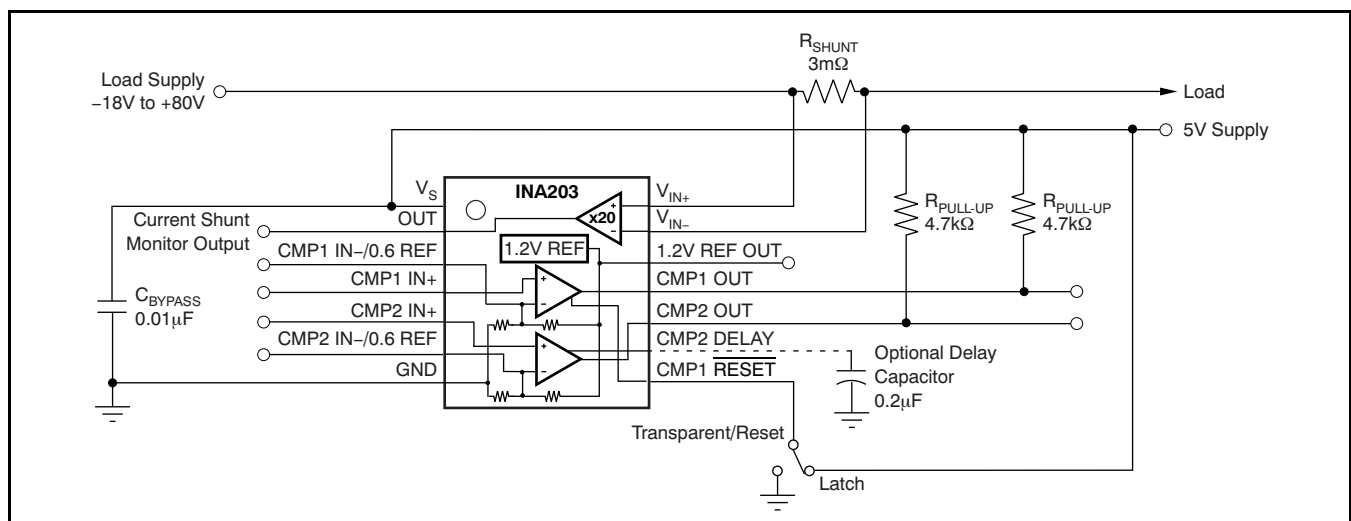


Figure 30. INA20x Basic Connection

In the [Typical Characteristics](#), the *Output Error vs Common-Mode Voltage* curve ([Figure 7](#)) shows the highest accuracy for this region of operation. In this plot, $V_S = 12V$; for $V_{CM} \geq 12V$, the output error is at its minimum. This case is also used to create the $V_{SENSE} \geq 20mV$ output specifications in the [Electrical Characteristics](#) table.

Normal Case 2: $V_{SENSE} \geq 20mV, V_{CM} < V_S$

This region of operation has slightly less accuracy than Normal Case 1 as a result of the common-mode operating area in which the part functions, as seen in the *Output Error vs Common-Mode Voltage* curve ([Figure 7](#)). As noted, for this graph $V_S = 12V$; for $V_{CM} < 12V$, the Output Error increases as V_{CM} becomes less than 12V, with a typical maximum error of 0.005% at the most negative $V_{CM} = -16V$.

Low V_{SENSE} Case 1:

$V_{SENSE} < 20mV, -16V \leq V_{CM} < 0$; and

Low V_{SENSE} Case 3:

$V_{SENSE} < 20mV, V_S < V_{CM} \leq 80V$

Although the INA203-Q1 is not designed for accurate operation in either of these regions, some applications are exposed to these conditions; for example, when monitoring power supplies that are switched on and off while V_S is still applied to the INA203-Q1. It is important to know what the behavior of the devices will be in these regions.

As V_{SENSE} approaches 0mV, in these V_{CM} regions, the device output accuracy degrades. A larger-than-normal offset can appear at the current shunt monitor output with a typical maximum value of $V_{OUT} = 300mV$ for $V_{SENSE} = 0mV$. As V_{SENSE} approaches 20mV, V_{OUT} returns to the expected output value with accuracy as specified in the [Electrical Characteristics](#). [Figure 31](#) illustrates this effect (Gain = 100).

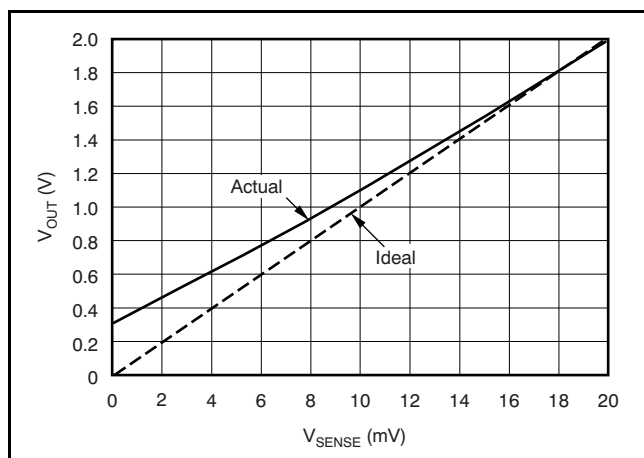


Figure 31. Example for Low V_{SENSE} Cases 1 and 3 (Gain = 100)

Low V_{SENSE} Case 2: $V_{SENSE} < 20mV, 0V \leq V_{CM} \leq V_S$

This region of operation is the least accurate for the INA203-Q1. To achieve the wide input common-mode voltage range, these devices use two op amp front ends in parallel. One op amp front end operates in the positive input common-mode voltage range, and the other in the negative input region. For this case, neither of these two internal amplifiers dominates and overall loop gain is very low. Within this region, V_{OUT} approaches voltages close to linear operation levels for Normal Case 2. This deviation from linear operation becomes greatest the closer V_{SENSE} approaches 0V. Within this region, as V_{SENSE} approaches 20mV, device operation is closer to that described by Normal Case 2. [Figure 32](#) illustrates this behavior. The V_{OUT} maximum peak for this case is tested by maintaining a constant V_S , setting $V_{SENSE} = 0mV$, and sweeping V_{CM} from 0V to V_S . The exact V_{CM} at which V_{OUT} peaks during this test varies from part to part, but the V_{OUT} maximum peak is tested to be less than the specified V_{OUT} Tested Limit.

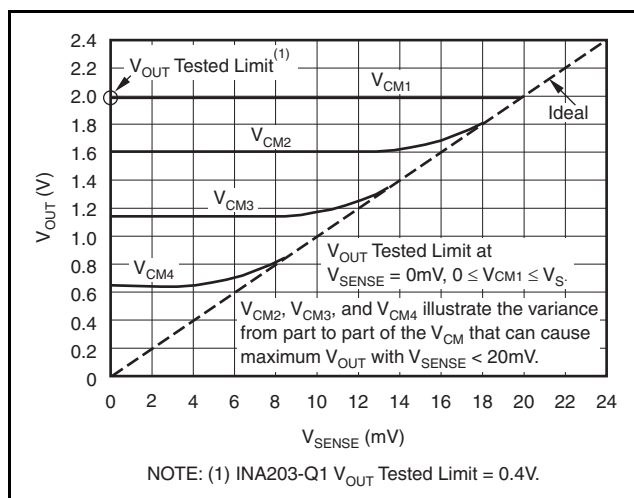


Figure 32. Example for Low V_{SENSE} Case 2 (Gain = 100)

SELECTING R_{SHUNT}

The value chosen for the shunt resistor, R_{SHUNT} , depends on the application and is a compromise between small-signal accuracy and maximum permissible voltage loss in the measurement line. High values of R_{SHUNT} provide better accuracy at lower currents by minimizing the effects of offset, while low values of R_{SHUNT} minimize voltage loss in the supply line. For most applications, best performance is attained with an R_{SHUNT} value that provides a full-scale shunt voltage range of 50mV to 100mV. Maximum input voltage for accurate measurements is $(V_{SHUNT} - 0.25)/Gain$.

TRANSIENT PROTECTION

The -16V to +80V common-mode range of the INA203-Q1 is ideal for withstanding automotive fault conditions ranging from 12V battery reversal up to +80V transients, since no additional protective components are needed up to those levels. In the event that the INA203-Q1 is exposed to transients on the inputs in excess of their ratings, then external transient absorption with semiconductor transient absorbers (zeners or *Transzorbs*) are necessary. Use of metal oxide varistors (MOVs) or video disk recorders (VDRs) is not recommended except when they are used in addition to a semiconductor transient absorber. Select the transient absorber such that it will never allow the INA203-Q1 to be exposed to transients greater than +80V (that is, allow for transient absorber tolerance, as well as additional voltage because of transient absorber dynamic impedance). Despite the use of internal zener-type ESD protection, the INA203-Q1 does not lend itself to using external resistors in series with the inputs because the internal gain resistors can vary up to ±30% but are closely matched. (If gain accuracy is not important, then resistors can be added in series with the INA203-Q1 inputs with two equal resistors on each input.)

OUTPUT VOLTAGE RANGE

The output of the INA203-Q1 is accurate within the output voltage swing range set by the power-supply pin, V+. This performance is best illustrated when using a gain of 100, where a 100mV full-scale input from the shunt resistor requires an output voltage swing of +10V, and a power-supply voltage sufficient to achieve +10V on the output.

INPUT FILTERING

An obvious and straightforward location for filtering is at the output of the INA203-Q1 series; however, this location negates the advantage of the low output impedance of the internal buffer. The only other option for filtering is at the input pins of the INA203-Q1, which is complicated by the internal 5kΩ + 30% input impedance; this configuration is illustrated in Figure 33. Using the lowest possible resistor values minimizes both the initial shift in gain and effects of tolerance. The effect on initial gain is given by Equation 3:

$$\text{Gain Error \%} = 100 - \left[100 \times \frac{5\text{k}\Omega}{5\text{k}\Omega + R_{\text{FILT}}} \right] \tag{3}$$

Total effect on gain error can be calculated by replacing the 5kΩ term with 5kΩ - 30%, (or 3.5kΩ) or 5kΩ + 30% (or 6.5kΩ). The tolerance extremes of R_{FILT} can also be inserted into the equation. If a pair of 100Ω 1% resistors are used on the inputs, the initial gain error will be 1.96%. Worst-case tolerance conditions will always occur at the lower excursion of the internal 5kΩ resistor (3.5kΩ), and the higher excursion of R_{FILT} - 3% in this case.

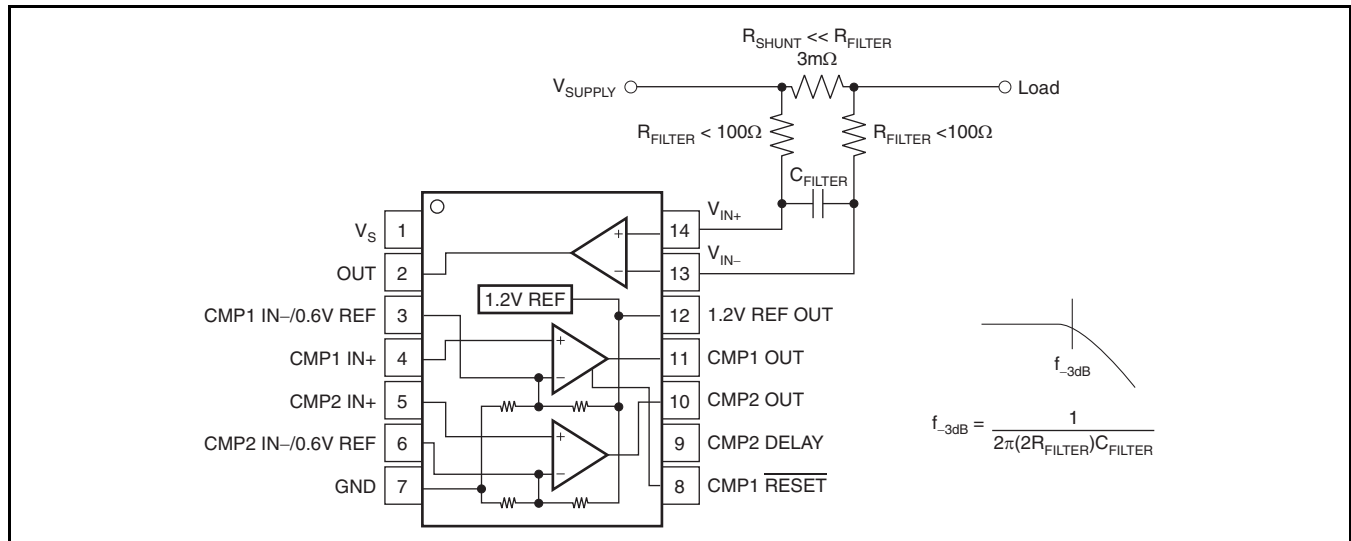


Figure 33. Input Filter (Gain Error: 1.5% to -2.2%)

Note that the specified accuracy of the INA203-Q1 must then be combined in addition to these tolerances. While this discussion treated accuracy worst-case conditions by combining the extremes of the resistor values, it is appropriate to use geometric mean or root sum square calculations to total the effects of accuracy variations.

REFERENCE

The INA203-Q1 include an internal voltage reference that has a load regulation of 0.4mV/mA (typical), and not more than 100ppm/°C of drift. Only the 14-pin package allows external access to reference voltages, where voltages of 1.2V and 0.6V are both available. Output current versus output voltage is illustrated in the [Typical Characteristics](#) section.

COMPARATOR

The INA203-Q1 incorporates two open-drain comparators. These comparators typically have 2mV of offset and a 1.3μs (typical) response time. The output of Comparator 1 latches and is reset through the CMP1 RESET pin, as shown in [Figure 35](#). This configuration applies to both the 10- and 14-pin versions. [Figure 34](#) illustrates the comparator delay.

The 14-pin versions of the INA203-Q1 include

additional features for comparator functions. The comparator reference voltage of both Comparator 1 and Comparator 2 can be overridden by external inputs for increased design flexibility. Comparator 2 has a programmable delay.

COMPARATOR DELAY (14-Pin Version Only)

The Comparator 2 programmable delay is controlled by a capacitor connected to the CMP2 Delay Pin; see [Figure 30](#). The capacitor value (in μF) is selected by using [Equation 4](#):

$$C_{\text{DELAY}} \text{ (in } \mu\text{F)} = \frac{t_{\text{D}}}{5} \quad (4)$$

A simplified version of the delay circuit for Comparator 2 is shown in [Figure 34](#). The delay comparator consists of two comparator stages with the delay between them. Note that I1 and I2 cannot be turned on simultaneously; I1 corresponds to a U1 low output and I2 corresponds to a U1 high output. Using an initial assumption that the U1 output is low, I1 is on, then U2 +IN is zero. If U1 goes high, I2 supplies 120nA to C_{DELAY}. The voltage at U2 +IN begins to ramp toward a 0.6V threshold. When the voltage crosses this threshold, the U2 output goes high while the voltage at U2 +IN continues to ramp up to a maximum of 1.2V when given sufficient time (twice the value of the delay specified for C_{DELAY}). This entire sequence is reversed when the comparator outputs go low, so that returning to low exhibits the same delay.

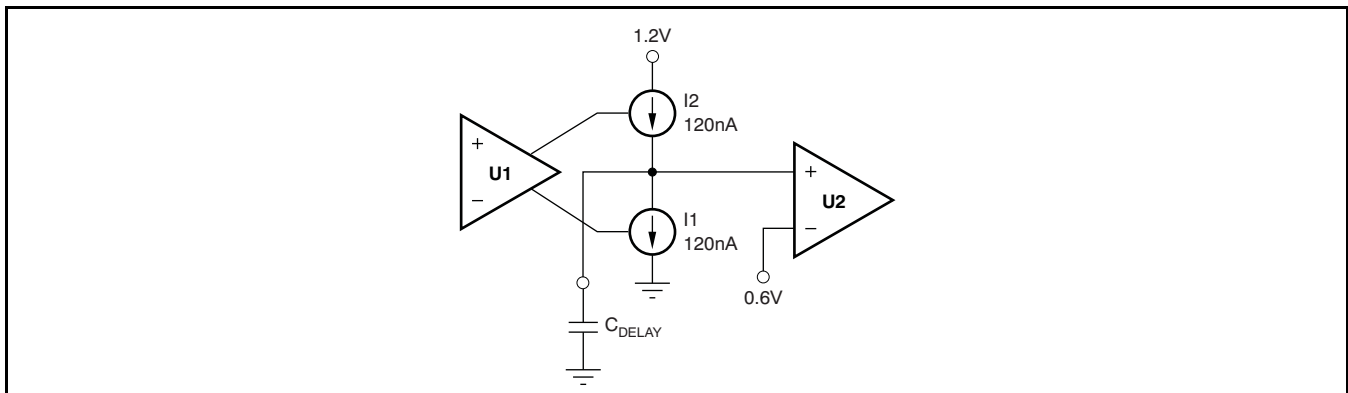


Figure 34. Simplified Model of the Comparator 2 Delay Circuit

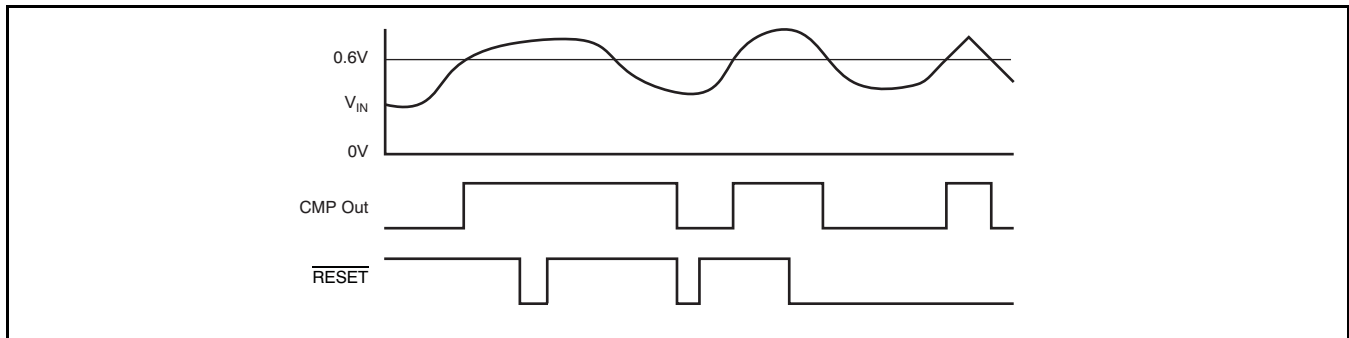


Figure 35. Comparator Latching Capability

It is important to note what will happen if events occur more rapidly than the delay timeout; for example, when the U1 output goes high (turning on I2), but returns low (turning I1 back on) prior to reaching the 0.6V transition for U2. The voltage at U2 +IN ramps back down at a rate determined by the value of C_{DELAY}, and only returns to zero if given sufficient time.

In essence, when analyzing Comparator 2 for behavior with events more rapid than its delay setting, use the model shown in Figure 34.

COMPARATOR MAXIMUM INPUT VOLTAGE RANGE

The maximum voltage at the comparator input for normal operation is up to (V+) – 1.5V. There are special considerations when overdriving the reference inputs (pins 3 and 6). Driving either or both inputs high enough to drive 1mA into the reference introduces errors into the reference. Figure 36 shows the basic input structure. A general guideline is to limit the voltage on both inputs to a total of 20V. The exact limit depends on the available voltage and

whether either or both inputs are subject to the large voltage. When making this determination, consider the 20kΩ from each input back to the comparator. Figure 37 shows the maximum input voltage that avoids creating a reference error when driving both inputs (an equivalent resistance back into the reference of 10kΩ).

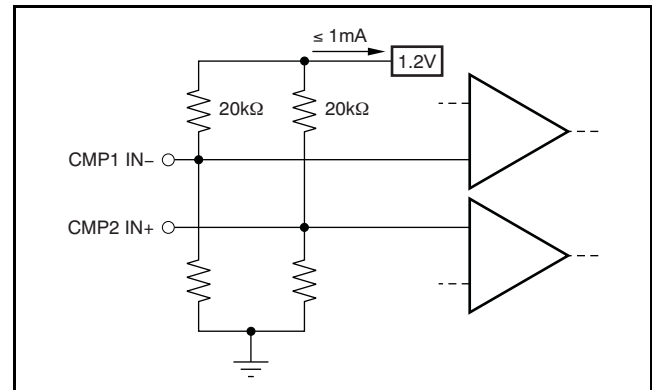


Figure 36. Limit Current Into Reference $\le 1\text{mA}$

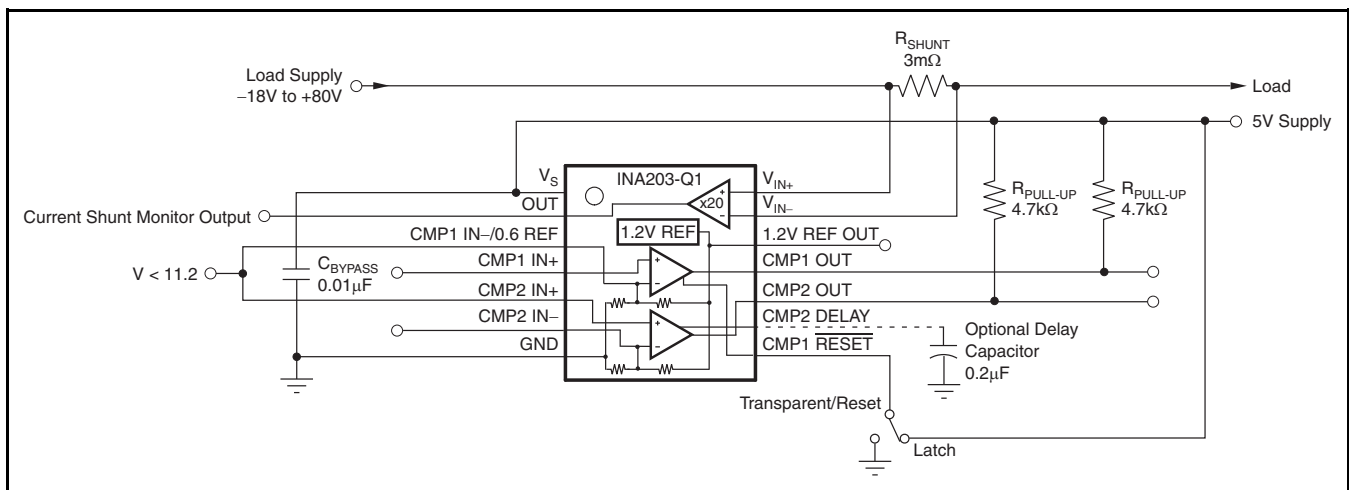


Figure 37. Overdriving Comparator Inputs Without Generating a Reference Error

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/ Ball Finish	MSL Peak Temp ⁽³⁾	Samples (Requires Login)
INA203AQPWRQ1	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Purchase Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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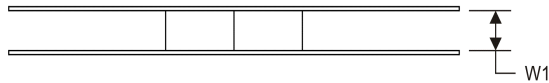
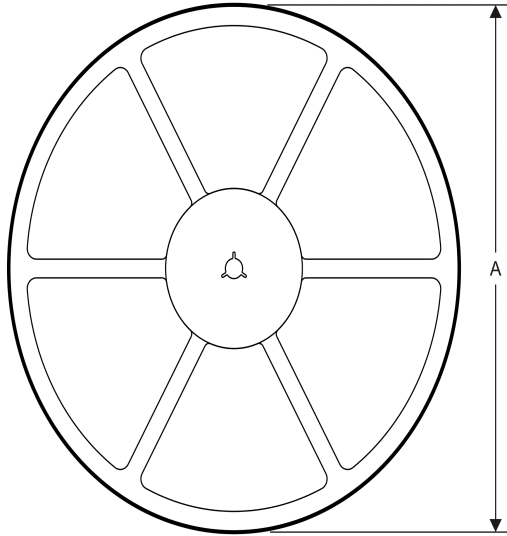
- Catalog: [INA203](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA203AQPWRQ1	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA203AQPWRQ1	TSSOP	PW	14	2000	367.0	367.0	35.0

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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