

OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC

FEATURES

- Provides Protection for Three Variables:
 - Input Overvoltage Protection
 - User-Programmable Overcurrent with Current Limiting
 - Battery Overvoltage
- 30V Maximum Input Voltage
- Supports up to 1.5A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- Status Indication – Fault Condition

- Available in Space-Saving Small 8 Lead 2x2 SON

APPLICATIONS

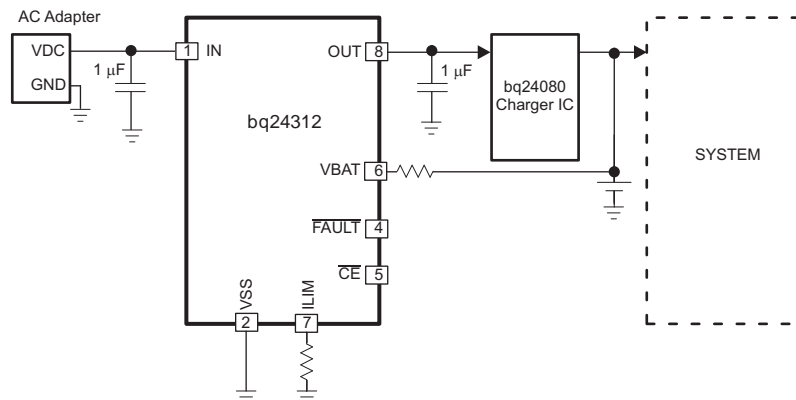
- Mobile Phones and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

DESCRIPTION

The bq24312 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable.

The IC can be controlled by a processor and also provides status information about fault conditions to the host.

APPLICATION SCHEMATIC



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

Bluetooth is a trademark of Bluetooth SIG, Inc.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

DEVICE ⁽²⁾	OVP THRESHOLD	PACKAGE	MARKING
bq24312DSG	5.85 V	2mm x 2mm SON	OUE

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.
 (2) To order a 3000-piece reel add R to the part number, or to order a 250-piece reel add T to the part number.

PACKAGE DISSIPATION RATINGS

PART NO.	PACKAGE	R _{θJC}	R _{θJA}
bq24312DSG	10 pin 2mm x 2mm SON	5°C/W	75°C/W

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	PIN	VALUE	UNIT
V _I	Input voltage	IN (with respect to VSS)	–0.3 to 30	V
		OUT (with respect to VSS)	–0.3 to 12	
		ILIM, FAULT, CE, VBAT (with respect to VSS)	–0.3 to 7	
I _I	Input current	IN	–1.8 ⁽²⁾ to 2	A
I _O	Output current	OUT	2	A
	Output sink current	FAULT	15	mA
ESD	Withstand Voltage	All (Human Body Model per JESD22-A114-E)	2000	V
		All (Machine Model per JESD22-A115-E)	200	V
		All (Charge Device Model per JESD22-C101-C)	500	V
		IN(IEC 61000-4-2) (with IN bypassed to the VSS with a 1-μF low-ESR ceramic capacitor)	15 (Air Discharge) 8 (Contact)	kV
T _J	Junction temperature		–40 to 150	°C
T _{stg}	Storage temperature		–65 to 150	°C

- (1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
 (2) Negative current is specified for a maximum of 50 hours at T_J = 175°C.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V _{IN}	Input voltage range	3	30	V
I _{IN}	Input current, IN pin		1.5	A
I _{OUT}	Output current, OUT pin		1.5	A
R _{ILIM}	OCP Programming resistor	15	90	k
T _J	Junction temperature	–40	125	°C

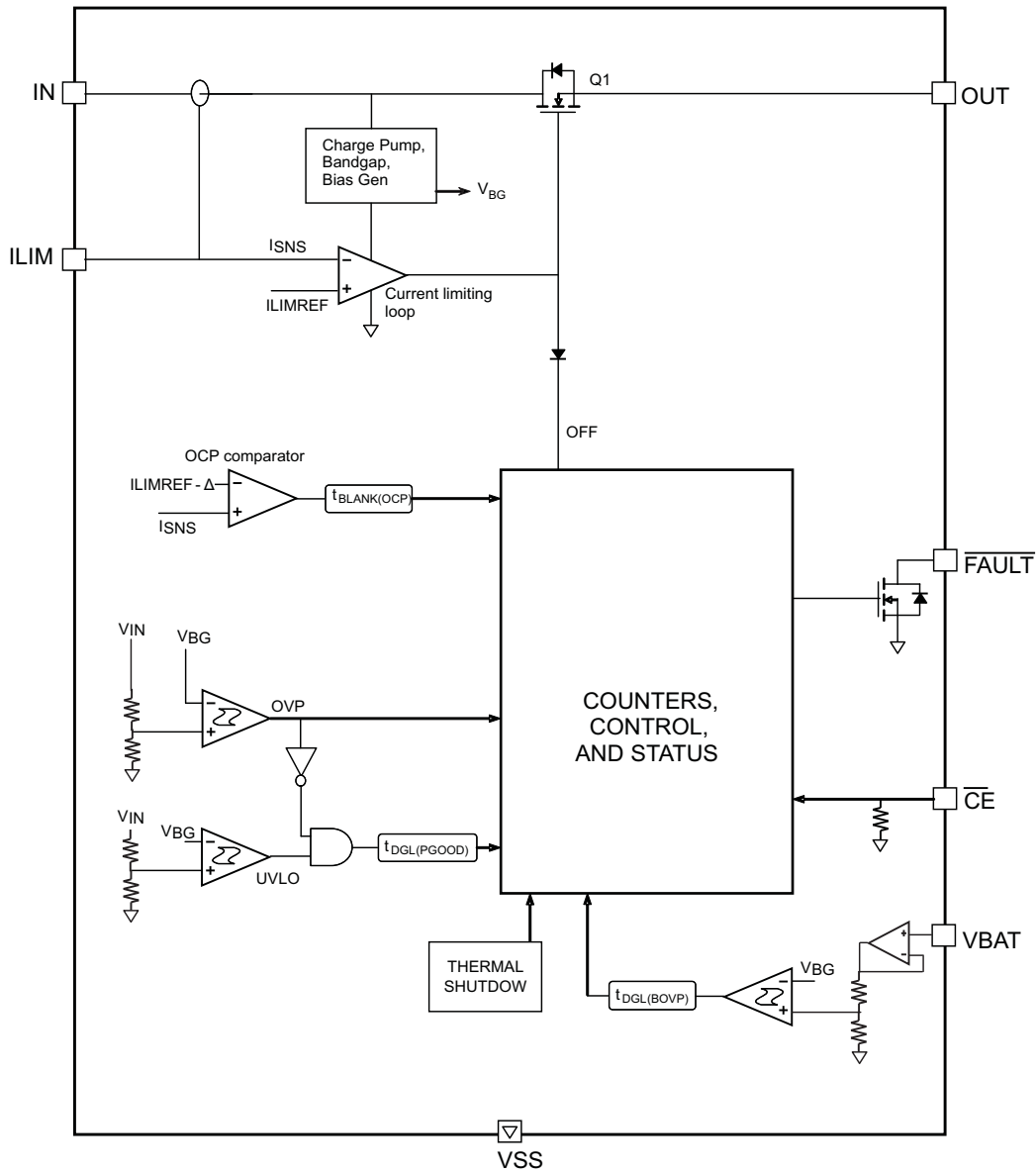


Figure 1. Simplified Block Diagram

TYPICAL OPERATING PERFORMANCE

Test conditions (unless otherwise noted) for typical operating performance: $V_{IN} = 5\text{ V}$, $C_{IN} = 1\ \mu\text{F}$, $C_{OUT} = 1\ \mu\text{F}$, $R_{ILIM} = 25\text{ k}$, $R_{BAT} = 100\text{ k}$, $T_A = 25^\circ\text{C}$, $V_{PU} = 3.3\text{V}$ (see Figure 20 for the Typical Application Circuit)

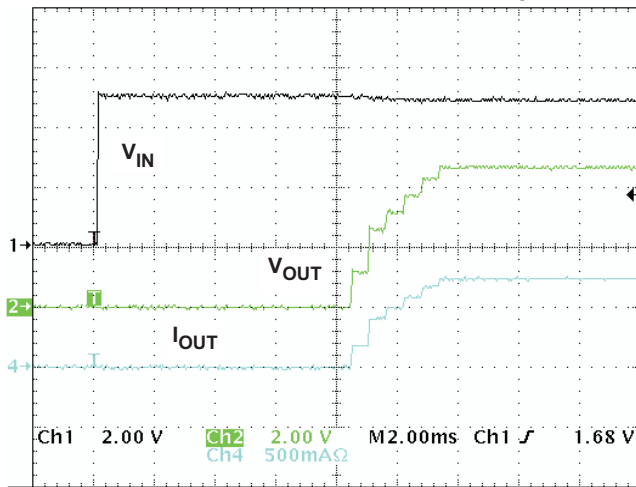


Figure 2. Normal Power-On Showing Soft-Start, $R_{OUT} = 6.6\Omega$

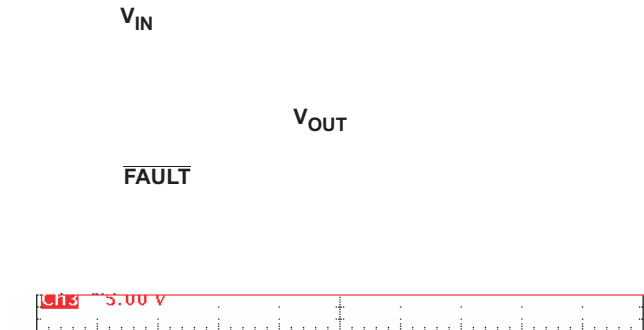


Figure 3. OVP at Power-On, $V_{IN} = 0\text{V to }9\text{V}$, $t_r = 50\mu\text{s}$

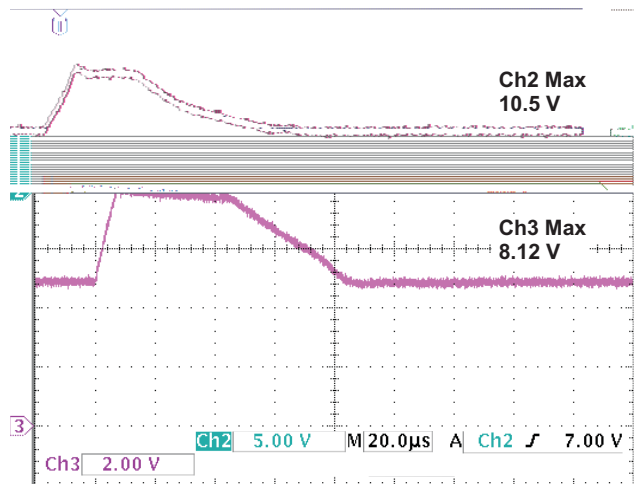


Figure 4. OVP Response for Input Step, $V_{IN} = 5\text{V to }10\text{V}$ back to 5V, $t_r = 10\mu\text{s}$, CH2 input voltage peak = 10.5V, CH3 output voltage peak = 8.12V. OVP duration is shorter than Blanking time.

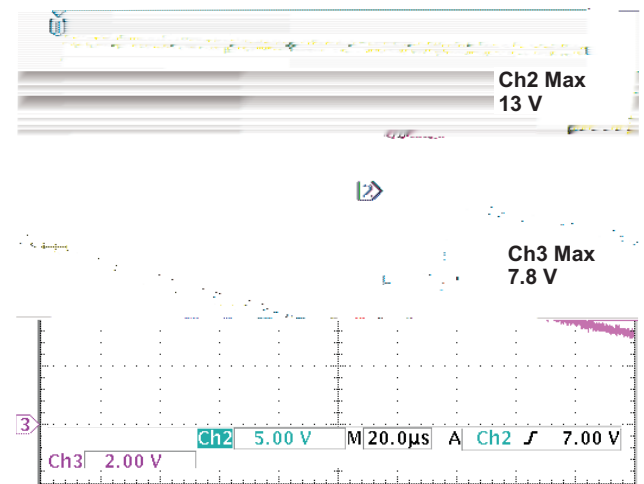


Figure 5. OVP Response for Input Step, $V_{IN} = 5\text{V to }12\text{V}$, $t_r = 4\mu\text{s}$. CH2 input voltage peak = 13V, CH3 output voltage peak = 7.8V. OVP duration is longer than Blanking time.

TYPICAL OPERATING PERFORMANCE (continued)

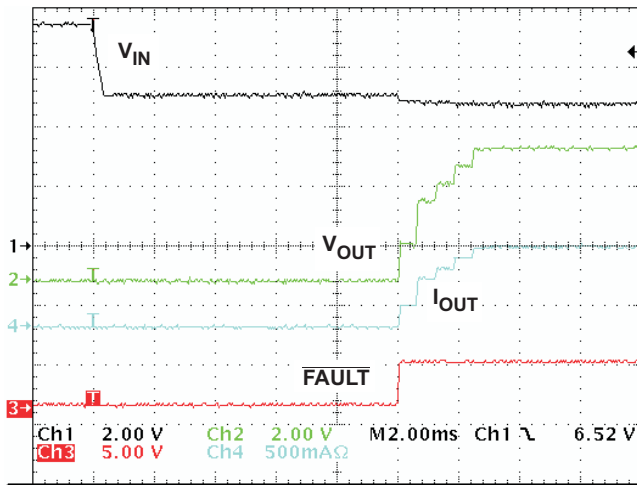


Figure 6. Recovery from OVP, $V_{IN} = 7.5V$ to $5V$, $t_f = 400\mu s$

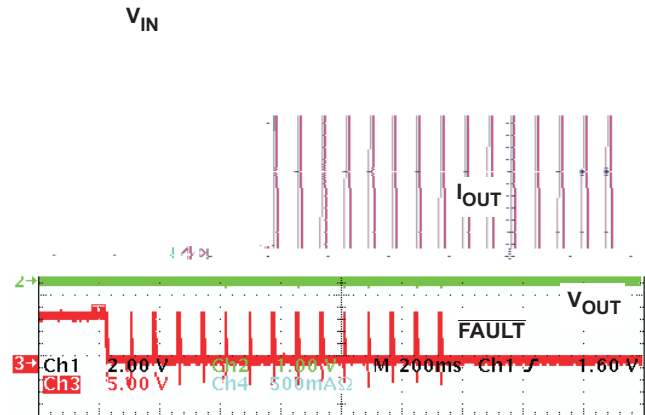


Figure 7. OCP, Powering Up into a Short Circuit on OUT Pin, OCP Counter Counts to 15 Before Switching OFF the Device

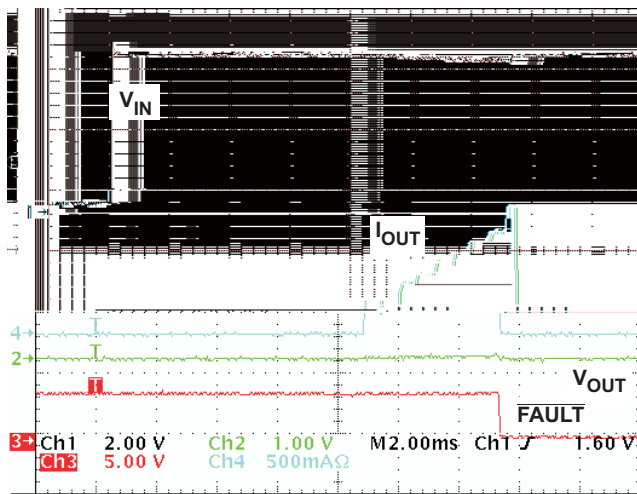


Figure 8. OCP, Zoom-in on the First Cycle of Figure 7

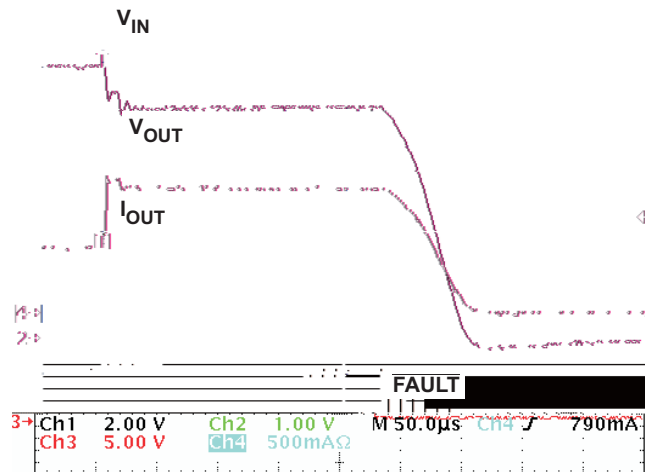
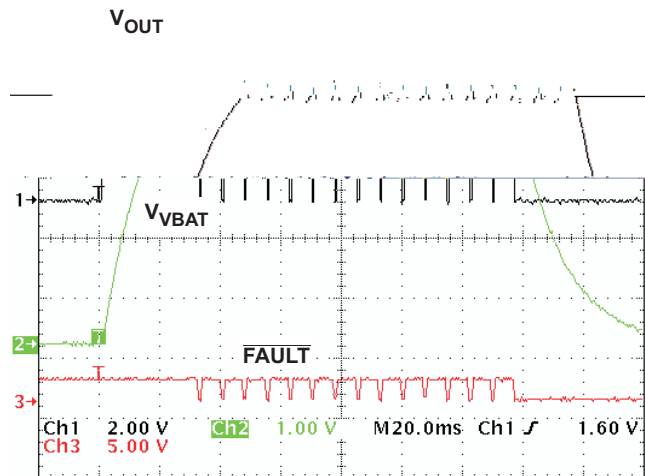
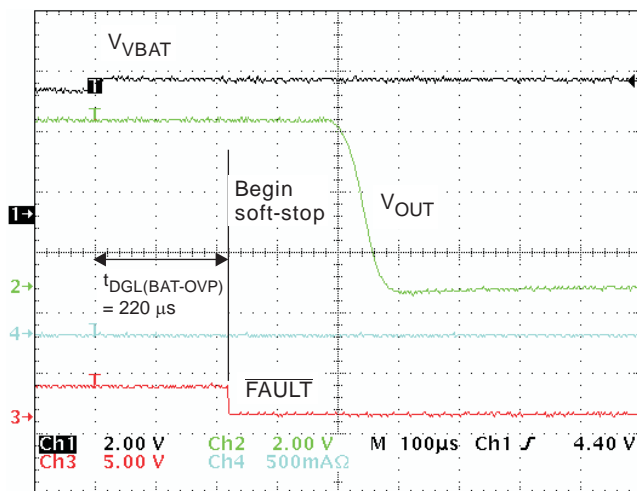
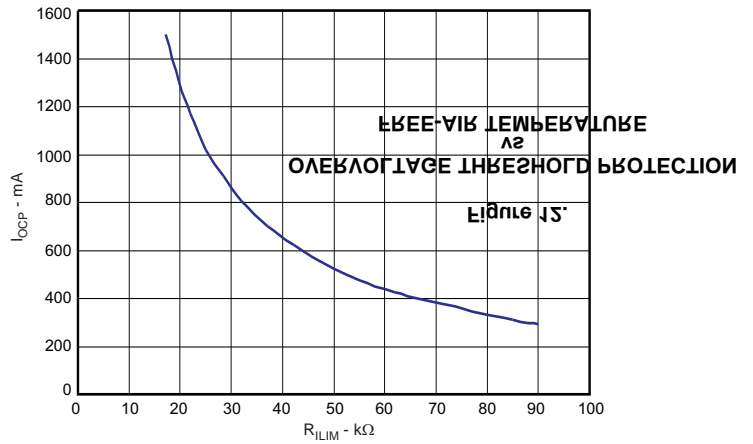
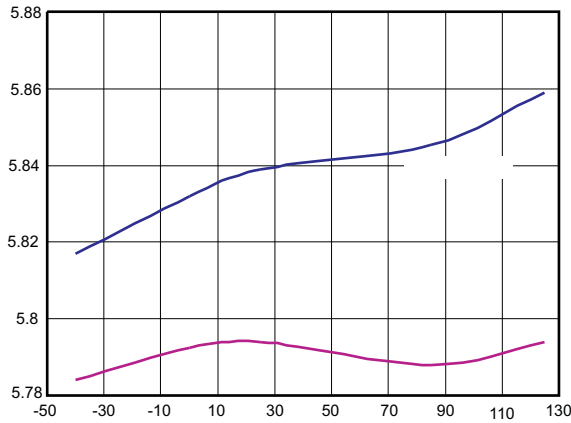
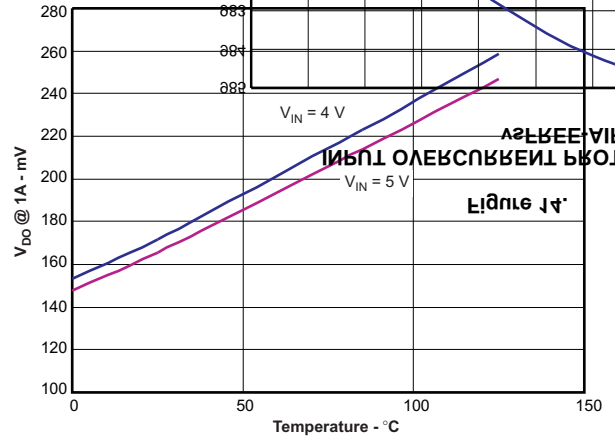
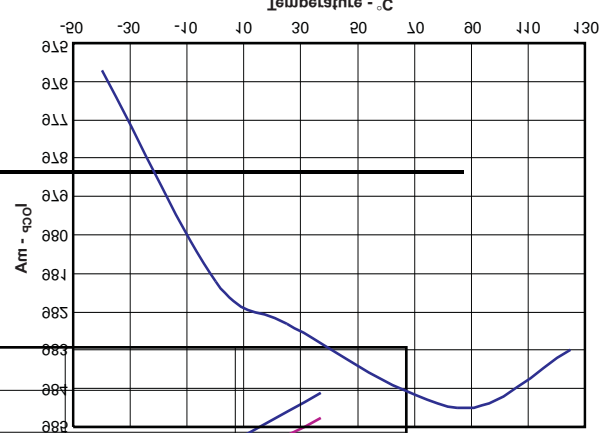
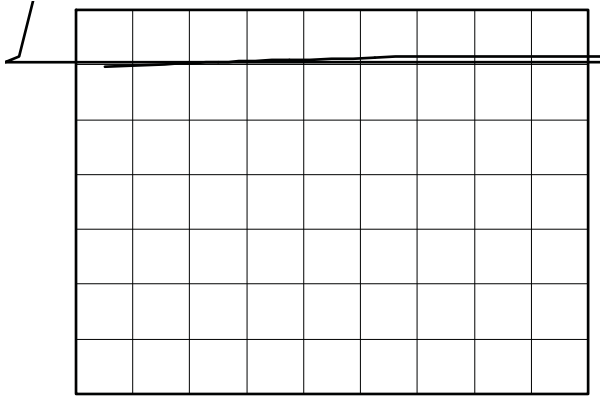


Figure 9. OCP, R_{OUT} Switches from 6.6Ω to 3.3





TEMPERATURE
vs
OVERLOAD PROTECTION

TEMPERATURE
vs
OVERLOAD PROTECTION

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TYPICAL OPERATING PERFORMANCE (continued)

LEAKAGE CURRENT (VBAT Pin)
vs
FREE-AIR TEMPERATURE

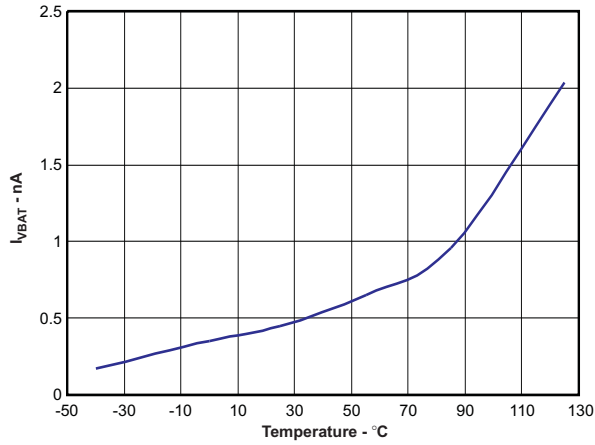


Figure 18.

SUPPLY CURRENT
vs
INPUT VOLTAGE

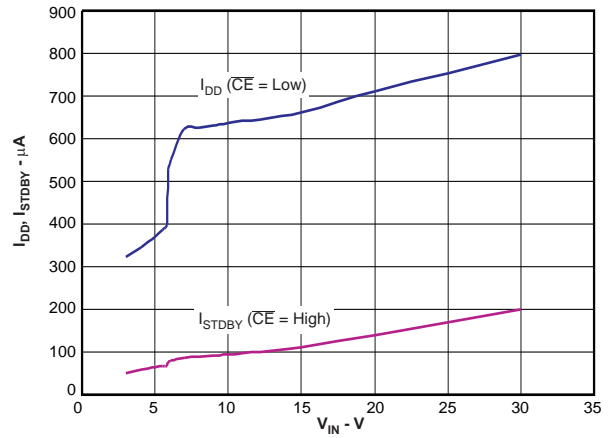


Figure 19.

TYPICAL APPLICATION CIRCUIT

$V_{OVP} = 5.85V$, $I_{OCP} = 1000mA$, $BV_{OVP} = 4.35V$ (Terminal numbers shown are for the 2x2 DSG package)

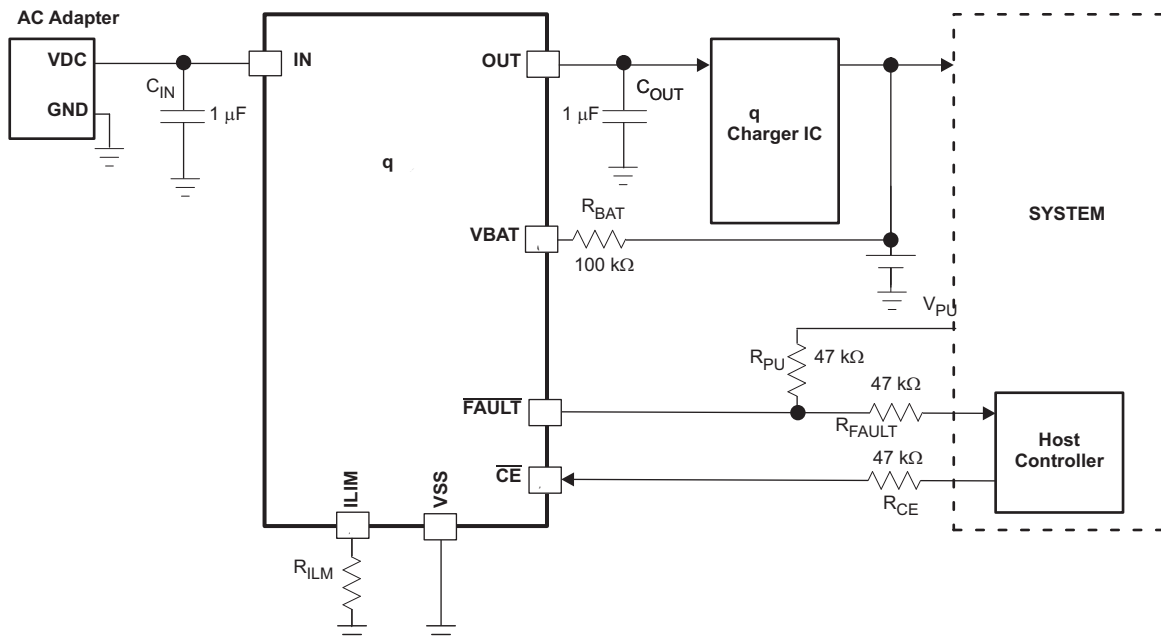


Figure 20.

DETAILED FUNCTIONAL DESCRIPTION

The bq24312 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. In case of an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. If the battery voltage rises to an unsafe level, the IC disconnects power from the charging circuit until the battery voltage returns to an acceptable value. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold UVLO. The FET Q1 connected between IN and OUT pins is off, and the status output, \overline{FAULT} , is set to Hi-Z.

POWER-ON RESET

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal

OPERATION

The device continuously monitors the input voltage, the input current, and the battery voltage as described in detail in the following sections.

Input Overvoltage Protection

As long as the input voltage is less than $V_{O(REG)}$, the output voltage tracks the input voltage (less the drop caused by $R_{DS(ON)}$ of Q1). If the input voltage is greater than $V_{O(REG)}$ (plus the $R_{DS(ON)}$ drop) and less than V_{OVP} , the device acts like a series linear regulator, with the output voltage regulated to $V_{O(REG)}$. If the input voltage rises above V_{OVP} , the output voltage is clamped to $V_{O(REG)}$ for a blanking duration $t_{BLANK(OVP)}$. If the input voltage returns below V_{OVP} within $t_{BLANK(OVP)}$, the device continues normal operation (See Figure 4). This provides protection against turning power off due to transient overvoltage spikes while still protecting the system. However, if the input voltage remains above V_{OVP} for more than $t_{BLANK(OVP)}$, the internal FET is turned off, removing power from the circuit (see Figure 5). When the input voltage comes back to a safe value the device waits for $t_{ON(OVP)}$, then switches on Q1 and goes through the soft-start routine (see Figure 6).

Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor R_{ILIM} connected from the ILIM pin to VSS. Figure 15 shows the OCP threshold as a function of R_{ILIM} , and may be approximated by the following equation: $I_{OCP} = 25 \div R_{ILIM}$ (current in A, resistance in k Ω), where R_{ILIM} must be between 15 k Ω and 90 k Ω .

If the load current tries to exceed the I_{OCP} threshold, the device limits the current for a blanking duration of $t_{BLANK(OCP)}$. If the load current returns to less than I_{OCP} before $t_{BLANK(OCP)}$ times out, the device continues to operate. However, if the overcurrent situation persists for $t_{BLANK(OCP)}$, the FET Q1 is turned off for a duration of $t_{REC(OCP)}$, and the FAULT pin is driven low. The FET is then turned on again after $t_{REC(OCP)}$ and the current is monitored all over again. Each time an OCP event occurs, the FAULT pin is driven low for a duration of $t_{REC(OCP)}$.

Battery Overvoltage Protection

Thermal Protection

Enable Function

Fault Indication

The $\overline{\text{FAULT}}$ pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting CE high. With CE low, the $\overline{\text{FAULT}}$ pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Battery overvoltage
- IC Overtemperature

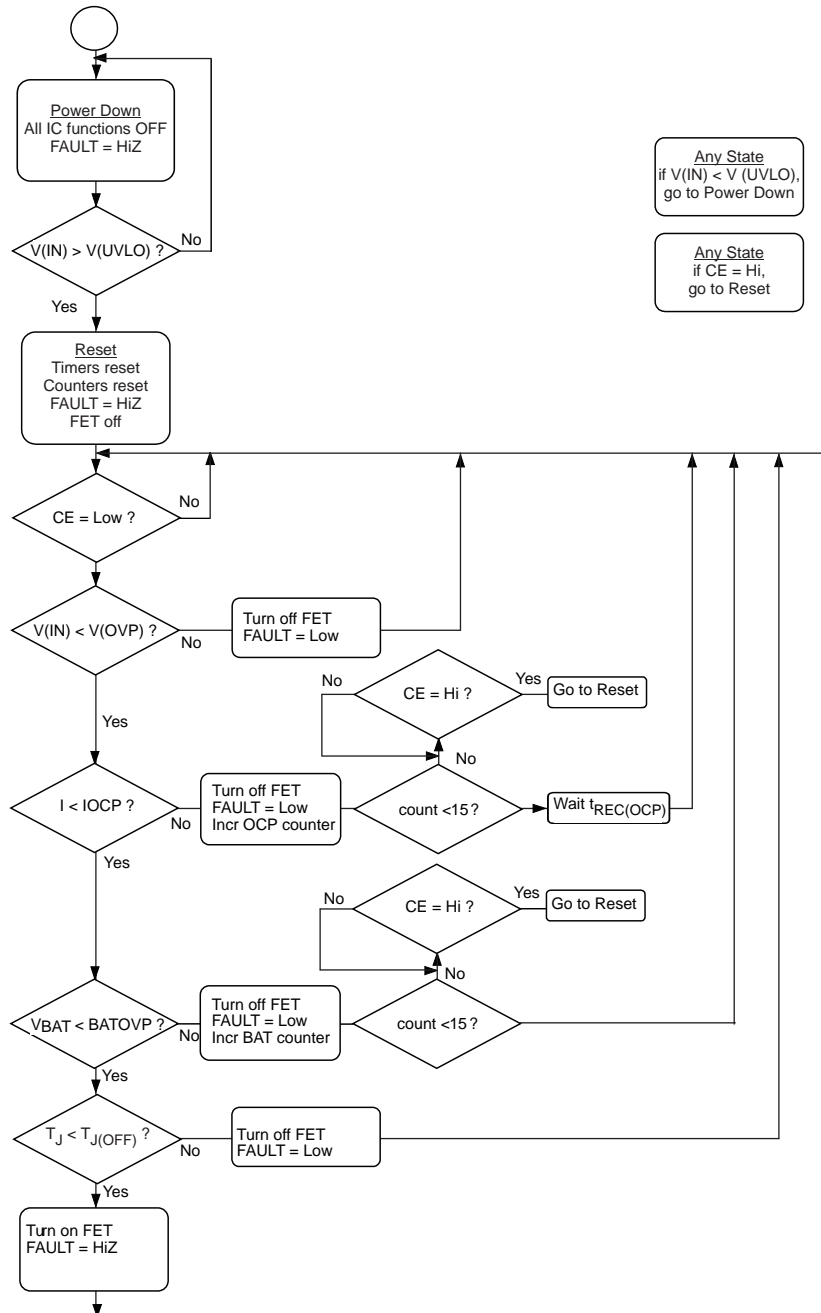


Figure 21. Flow Diagram

APPLICATION INFORMATION (WITH REFERENCE TO FIGURE 20)

Selection of R_{BAT}

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the bq24312 can be hazardous. Connecting the VBAT pin through R_{BAT} prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety, R_{BAT} should have a very high value. The problem with a large R_{BAT} is that the voltage drop across this resistor because of the VBAT bias current I_{VBAT} causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35V BV_{OVP} threshold.

Choosing R_{BAT} in the range 100k to 470k is a good compromise. In the case of an IC failure, with R_{BAT} equal to 100k, the maximum current flowing into the battery would be $(30V - 3V) \div 100k = 246\mu A$, which is low enough to be absorbed by the bias currents of the system components. R_{BAT} equal to 100k would result in a worst-case voltage drop of $R_{BAT} \times I_{VBAT} = 1mV$. This is negligible to compared to the internal tolerance of 50mV on BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

Selection of R_{CE} , R_{FAULT} , and R_{PU}

The \overline{CE} pin can be used to enable and disable the IC. If host control is not required, the \overline{CE} pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the \overline{CE} pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the \overline{CE} pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor should be greater than V_{IH} of the bq24312 \overline{CE} pin. The drop across the resistor is given by $R_{CE} \times I_{IH}$.

The \overline{FAULT} pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the \overline{FAULT} pin, it can be left unconnected. But if the \overline{FAULT} pin has to be monitored, it should be pulled high externally through R_{PU} , and connected to the host through R_{FAULT} . R_{FAULT} prevents damage to the host controller if the bq24312 fails (see above). The resistors should be of high value, in practice values between 22k and 100k should be sufficient.

Selection of Input and Output Bypass Capacitors

The input capacitor

Powering Accessories

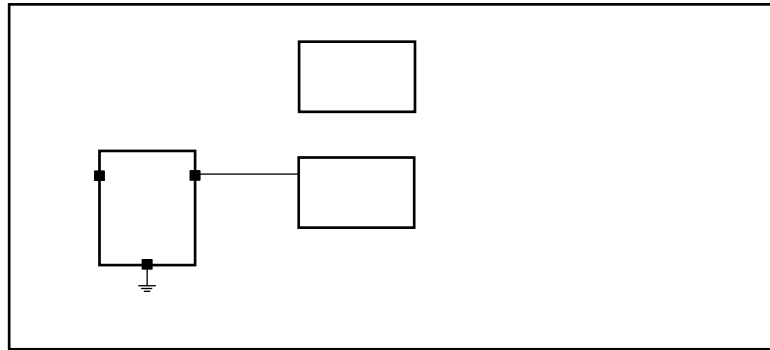


Figure 22. Charging - The Red Arrows Show the Direction of Current Flow

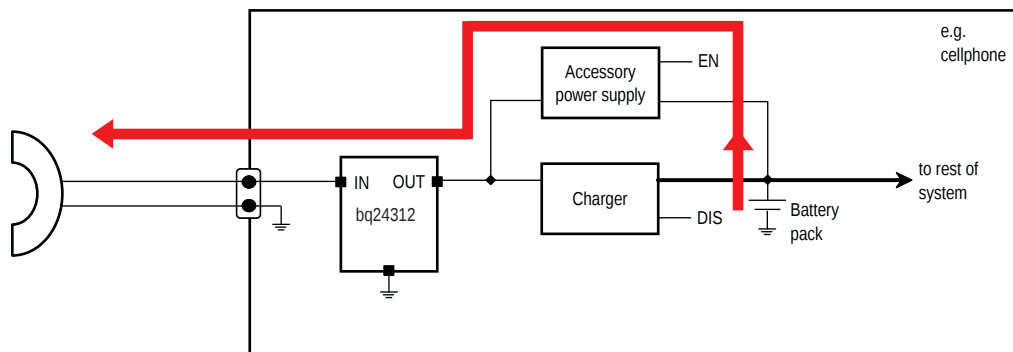


Figure 23. Powering an Accessory - The Red Arrows Show the Direction of Current Flow

In the second case, when power is being delivered to an accessory, the bq24312 device is required to support current flow from the OUT pin to the IN pin.

If $V_{OUT} > UVLO + 0.7V$, FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 will then remain ON as long as $V_{OUT} > UVLO - V_{hys}(UVLO) + R_{DS(on)} \times I_{ACCESSORY}$. Within this voltage range, the reverse current capability is the same as the forward capability, 1.5A. It should be noted that there is no overcurrent protection in this direction.

PCB Layout Guidelines:

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages.
- The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
- C_{IN} and C_{OUT} should be located close to the IC. Other components like R_{ILIM} and R_{BAT} should also be located close to the IC.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
BQ24312DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	

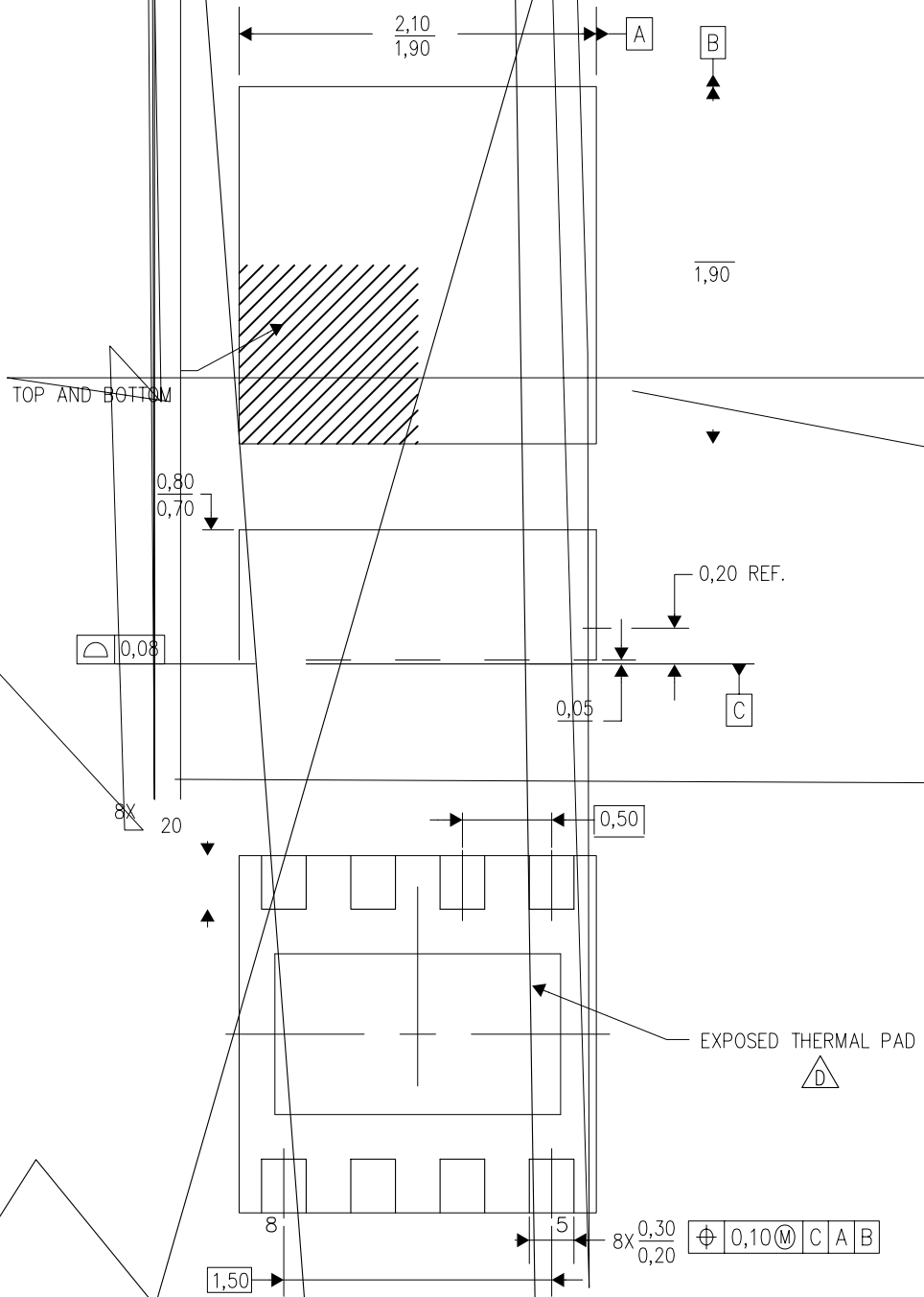
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24312DSGR	WSON	DSG	8	3000	195.0	200.0	45.0
BQ24312DSGT	WSON	DSG	8	250	195.0	200.0	45.0

STIC SMALL OUTLINE NO-LEAD



- B. This drawing is sufficient for manufacturing.
- C. Quad Flatpack, No-Leads (QFN) package configuration.
- The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details.
- E. Falls within JEDEC MO-229.

THERMAL PAD MECHANICAL DATA

DSG (S-PWSON-N8)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the thermal pad can be attached to an external heatsink. In addition, through the use of thermal vias, the thermal pad can be attached to a copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design is an integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SOP PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad is shown in the following illustration.

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