Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC With LDO Mode

FEATURES

- Input Overvoltage Protection
- Accurate Battery Overvoltage Protection
- Output Short-Circuit Protection
- Soft-Start to Prevent Inrush Currents
- Soft-Stop to Prevent Voltage Spikes
- 30-V Maximum Input Voltage
- Supports up to 1.7-A Load Current
- Thermal Shutdown
- Enable Function
- Fault Status Indication
- Small 2 mm × 2 mm 8-Pin SON Package

APPLICATIONS

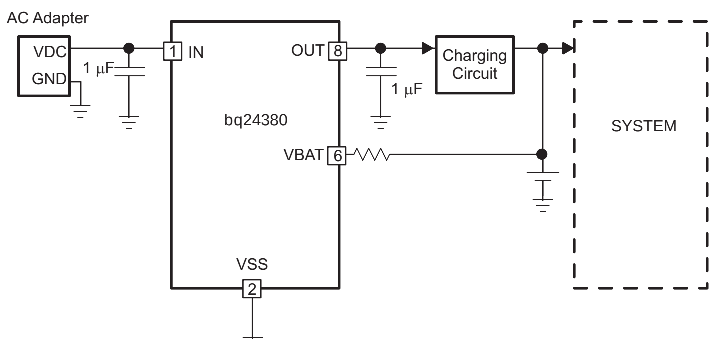
- Smart Phones, Mobile Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices

DESCRIPTION

The bq2438x family are charger front-end integrated circuits designed to provide protection to Li-ion batteries from failures of the charging circuitry. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.5-V (bq24380) or 5-V (bq24381, bq24382) output with input voltages up to the Input overvoltage threshold. During input overvoltage conditions, the IC immediately turns off the internal pass FET disconnecting the charging circuitry from the damaging input source. Additionally, if the battery voltage rises to unsafe levels while charging, power is removed from the system. The IC checks for short-circuit or overload conditions at its output when turning the pass FET on, and if it finds unsafe conditions, it switches off, and then rechecks the conditions. Additionally, the IC also monitors its die temperature and switches off if it exceeds 140°C.

When the IC is controlled by a processor, the IC provides status information about fault conditions to the host.

APPLICATION SCHEMATIC



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

DEVICE	V_{OVP}	$V_{O(REG)}$	PACKAGE (1)	MARKING
bq24380	6.3 V	5.5 V	2mm x 2mm SON	CFE
bq24381	7.1 V	5 V	2mm x 2mm SON	CFW
bq24382	10.5 V	5 V	2mm x 2mm SON	OBE

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI Web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

over operating free-air temperature range (unless otherwise noted)

			VALUE	UNIT
V_I	Input voltage	IN (with respect to VSS)	–0.3 to 30	V
		OUT (with respect to VSS)	–0.3 to 12	V
		$\overline{\text{FAULT}}$, $\overline{\text{CE}}$, VBAT (with respect to VSS)	–0.3 to 7	V
I_{OUT}max	Output source current	OUT	2	A
	Output sink current	$\overline{\text{FAULT}}$	15	mA
T_J	Junction temperature		–40 to 150	°C
T_{stg}	Storage temperature		–65 to 150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.

DISSIPATION RATINGS

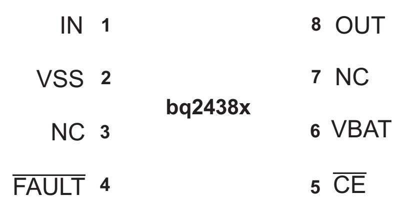
PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$
DSG	5°C/W	75°C/W

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
V_I	IN voltage range	3.3	30	V
I_O	Current, OUT pin		1.7	A
T_J	Junction temperature	-40	125	°C

ELECTRICAL CHARACTERISTICS

DEVICE INFORMATION

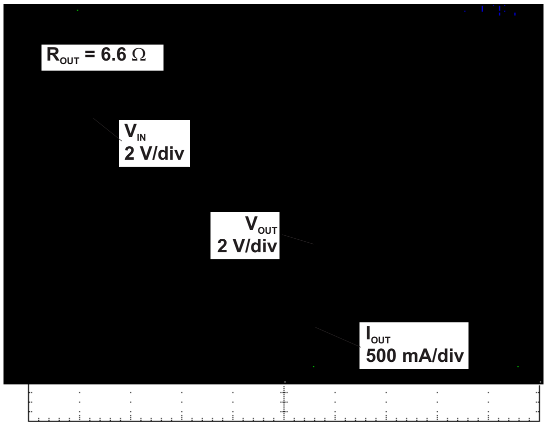


TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
IN	1	I	Input power, connected to external DC supply. Bypass IN to VSS with a ceramic capacitor (1 μF minimum)
VSS	2	–	Ground terminal. Connect to the thermal pad and to the ground rail of the circuit.
NC	3, 7		Do not connect to any external circuits. These pins may have internal connections used for test purposes.
$\overline{\text{FAULT}}$	4	O	Open-drain device status output. $\overline{\text{FAULT}}$ is pulled to VSS internally when the input pass FET has been turned off due to input overvoltage or output short-circuit conditions, an overtemperature condition, or because the battery voltage is outside safe limits. $\overline{\text{FAULT}}$ is high impedance during normal operation.
$\overline{\text{CE}}$	5	I	Active-low chip enable input. Connect $\overline{\text{CE}}$ = HI to turn the input pass FET off. Connect $\overline{\text{CE}}$ = LOW to turn the internal pass FET on and connect the input to the charging circuitry. $\overline{\text{CE}}$ is Internally pulled down, ~200 k .
VBAT	6	I	Battery voltage sense input. Connected to pack positive terminal through a 100-k resistor.
OUT	8	O	Output terminal to the charging system. Bypass OUT to VSS with a ceramic capacitor (1 μF minimum)
Thermal PAD			The thermal pad is electrically connected to VSS internally. The thermal pad must be connected to the same potential as the VSS pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. VSS pin must be connected to ground at all times.

TYPICAL CHARACTERISTICS

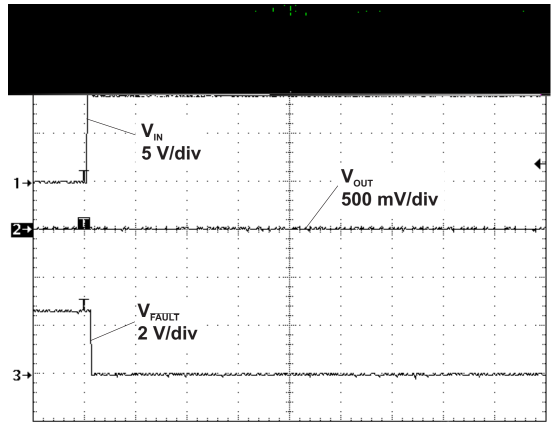
NORMAL POWER-ON SHOWING SOFT-START (bq24380)



t - Time - 2 ms/div

Figure 1.

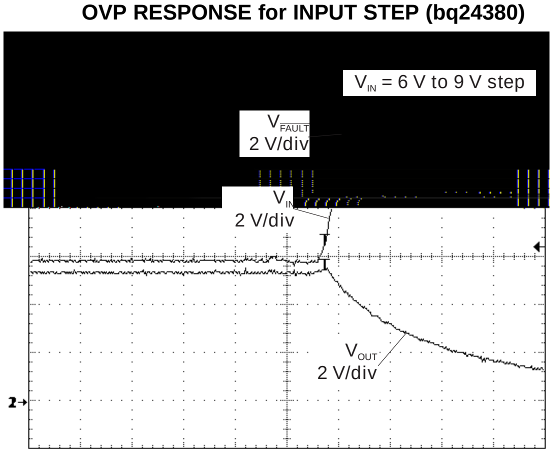
OVP at POWER-ON



t - Time - 2 ms/div

Figure 2.

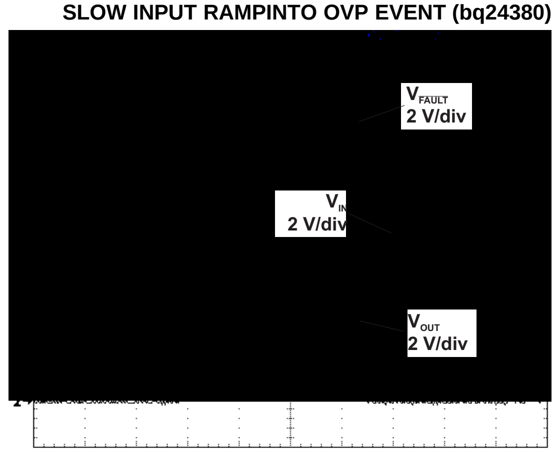
OVP RESPONSE for INPUT STEP (bq24380)



t - Time - 5 μs/div

Figure 3.

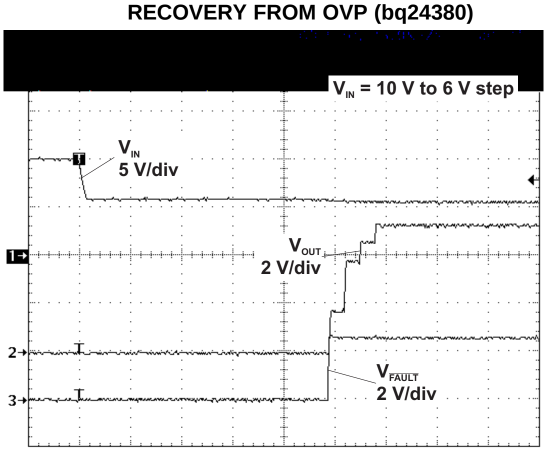
SLOW INPUT RAMPINTO OVP EVENT (bq24380)



t - Time - 200 ms/div

Figure 4.

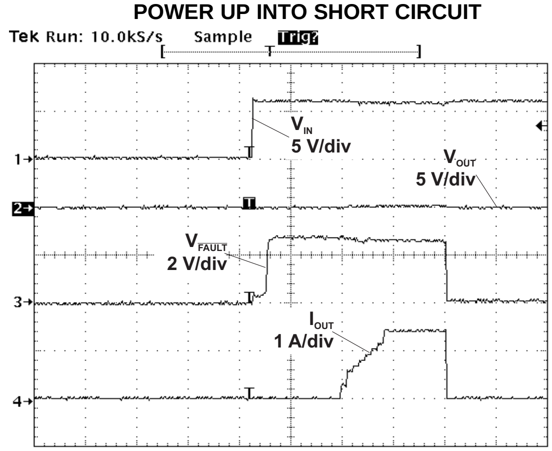
RECOVERY FROM OVP (bq24380)



t - Time - 2 ms/div

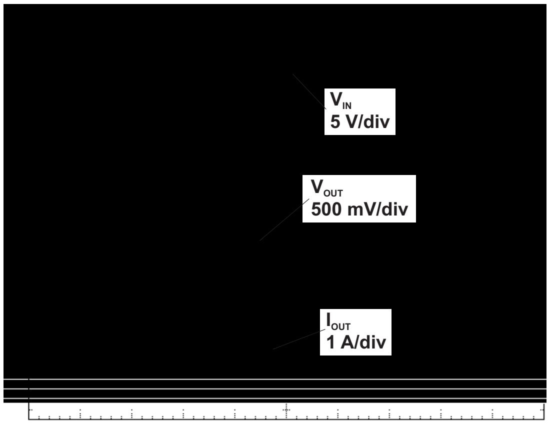
Figure 5.

POWER UP INTO SHORT CIRCUIT

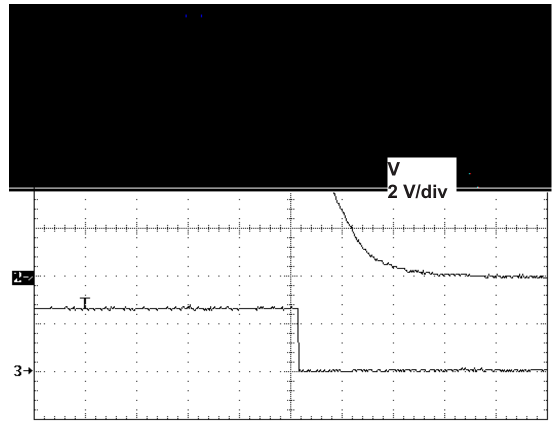


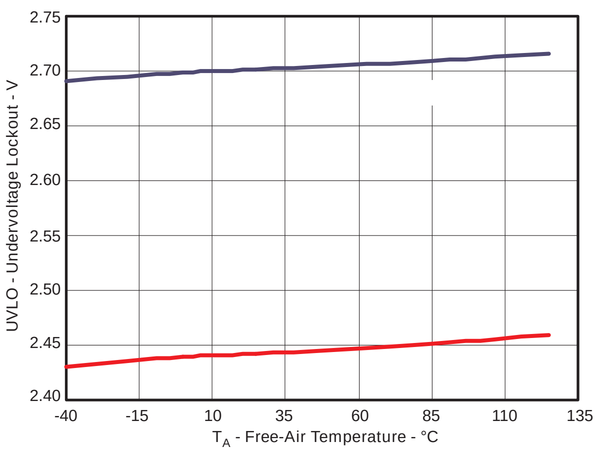
t - Time - 5 ms/div

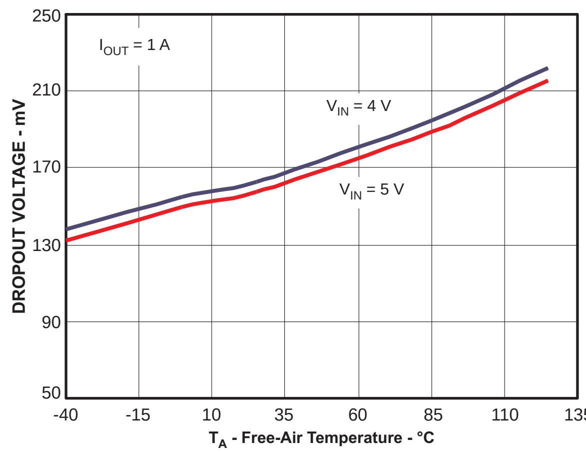
Figure 6.

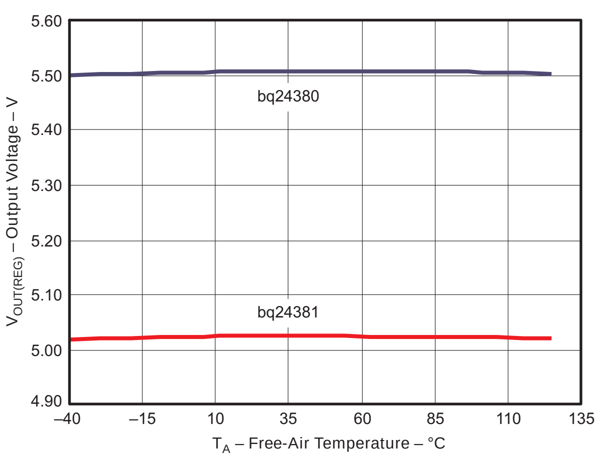


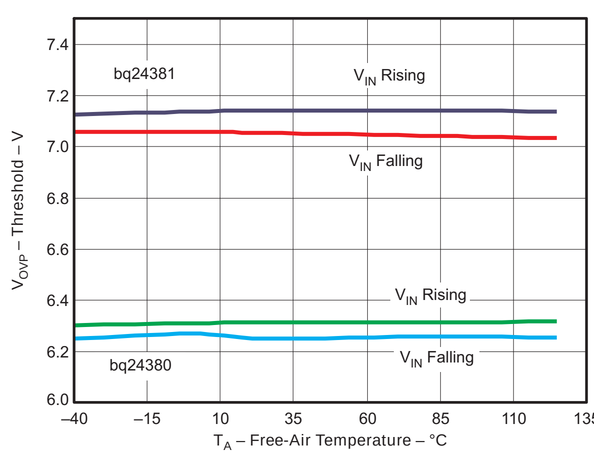
t - Time - 20 µs/div











TYPICAL CHARACTERISTICS (continued)

OVP THRESHOLD, V_{BOVP} vs FREE-AIR TEMPERATURE

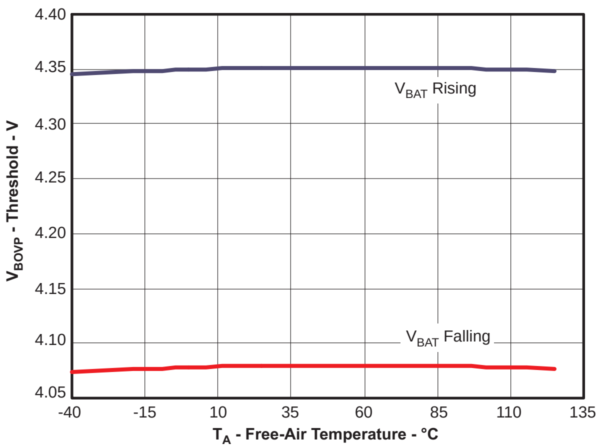


Figure 13.

LEAKAGE CURRENT (VBAT PIN) vs FREE-AIR TEMPERATURE

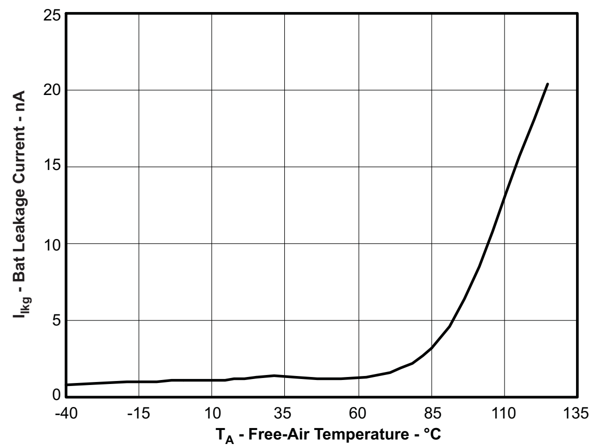


Figure 14.

SUPPLY CURRENT vs INPUT VOLTAGE (bq24380)

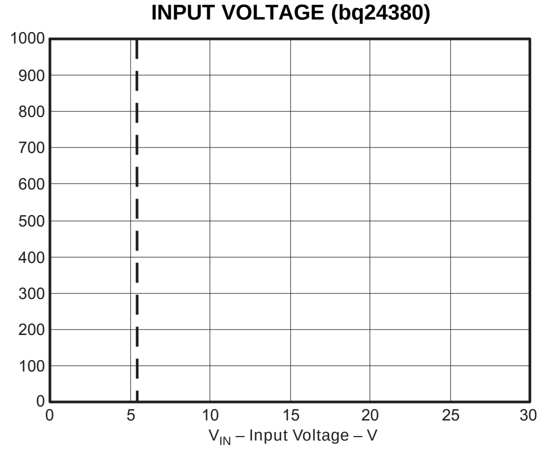


Figure 15.

SUPPLY CURRENT vs INPUT VOLTAGE (bq24381)

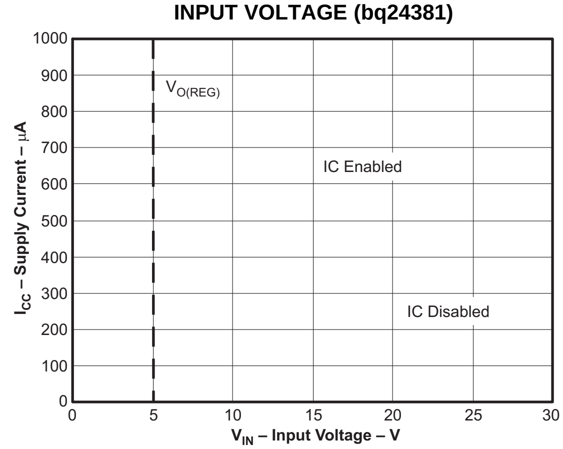
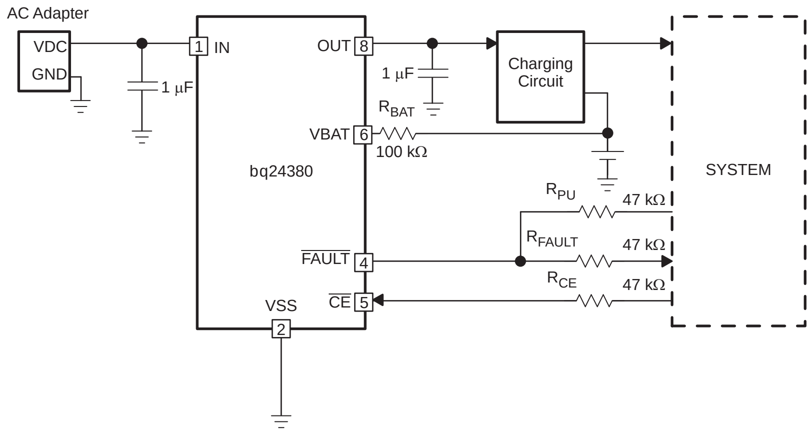
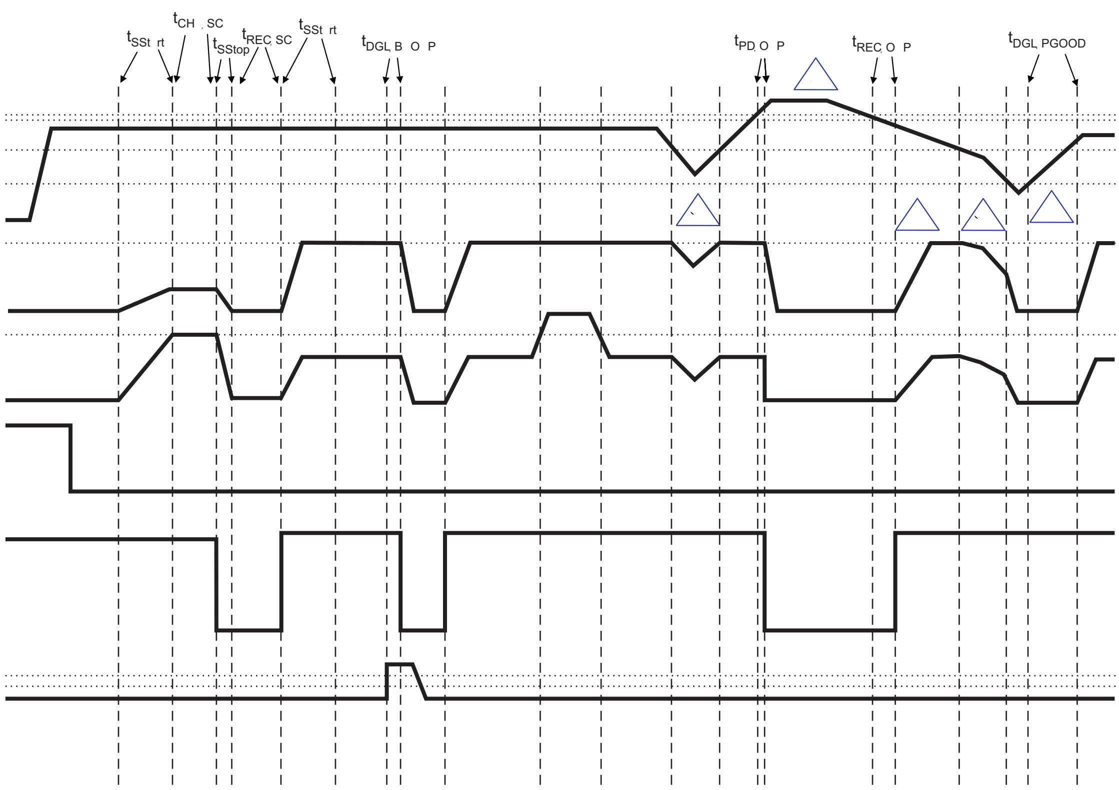


Figure 16.





Short circuit during st rt up
Nor st rt up condition
B ttery overvo t ge event
U LO IN OREG OUT tr cks IN
Input overvo t ge event
Input e o U LO
High current event during nor oper tion

DETAILED FUNCTIONAL DESCRIPTION

The bq2438x is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit and the input source. The IC continuously monitors the input voltage and the battery voltage. The device operates like a linear regulator, maintaining a 5.5-V (bq24380) or 5-V (bq24381, bq24382) output with input voltages up to the input overvoltage threshold (V_{OVP}). If the input voltage exceeds V_{OVP}, the IC shuts off the pass FET and disconnects the system from input power. Additionally, if the battery voltage rises above 4.35 V, the IC switches off the pass FET, removing the power from the system until the battery voltage falls to safe levels. The IC also monitors its die temperature and switches the pass FET off if it exceeds 140°C.

The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

POWER DOWN

The device remains in power-down mode when the input voltage at the IN pin is below the undervoltage threshold (UVLO) of 2.8 V. The FET connected between the IN and OUT pins is off, and the status output, FAULT, is set to HI-Z.

6(set)Tj 1 0 0 19 118.01 249.2 Tm /F2 -10 Tf (6(set)Tj 1 0 0 19 118 /F2 -10 Tf (6(set)Tj 1)Tj 1 0 0 1 1

POWER ON RESET

DETAILED FUNCTIONAL DESCRIPTION

Input Overvoltage Protection

Battery Overvoltage Protection

Thermal Protection

Start-Up Short-Circuit Protection

The bq2438x features overload current protection during start-up. The *condition 1* in Figure 18 illustrates start-up into an overload condition. If after the eight soft-start steps are complete, and the current limit is exceeded, the IC initiates a short-circuit check timer ($t_{CHK(SC)}$). During this check, the current is clamped to $I_{O(SC)}$. If the 5-ms $t_{CHK(SC)}$ timer expires and the current remains clamped by the current limit, the internal pass FET is turned off using the soft-stop method, $\overline{\text{FAULT}}$ is pulled low and the $t_{REC(SC)}$ timer begins. Once the $t_{REC(SC)}$ timer expires, $\overline{\text{FAULT}}$ becomes high impedance and the soft-start sequence restarts. The device repeats the start/fail sequence until the overload condition is removed. Once the overload condition is removed, the current limit circuitry is disabled and the device enters normal operation. Additionally, if the current is not limited after the completion of the soft-start sequence, the $t_{CHK(SC)}$ timer does not start and the current limit circuitry is disabled for normal operation.

Enable Function

The IC has an enable pin which is used to enable and disable the device. Connect the $\overline{\text{CE}}$ pin high to turn off the internal pass FET. Connect the $\overline{\text{CE}}$ pin low to turn on the internal pass FET and enter the start-up routine. The $\overline{\text{CE}}$ pin has an internal pulldown resistor and can be left unconnected. The $\overline{\text{FAULT}}$ pin is high impedance when the $\overline{\text{CE}}$ pin is high.

Fault Indication

The $\overline{\text{FAULT}}$ pin is an active-low, open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting $\overline{\text{CE}}$ high. With $\overline{\text{CE}}$ low, the $\overline{\text{FAULT}}$ pin goes low whenever any of these events occurs:

1. Output short-circuit at power-on
2. Input overvoltage
3. Battery overvoltage
4. IC overtemperature

See Figure 18 for an example of $\overline{\text{FAULT}}$ conditions during these events. Connect the $\overline{\text{FAULT}}$ pin to the desired logic level voltage rail through a resistor between 1 k and 50 k .

APPLICATION INFORMATION

Selection of $R_{(BAT)}$

It is recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30 V, and applying 30 V to the battery may cause failure of the device and can be hazardous. Connecting the VBAT pin through $R_{(BAT)}$ prevents a large current from flowing into the battery in the event of failure. For safety, $R_{(BAT)}$ must have a high value. The problem with a large $R_{(BAT)}$ is that the voltage drop across the resistor because of the VBAT bias current, $I_{(VBAT)}$, which causes an error in the BV_{OVP} threshold. This error is over and above the tolerance on the nominal 4.35-V BV_{OVP} threshold.

Choosing $R_{(BAT)}$ in the range of 100 k to 470 k is a good compromise. If the IC fails with $R_{(BAT)}$ equal to 100 k, the maximum current flowing into the battery would be (30 V – 3 V) ÷ 100 k = 246 µA, which is low enough to be absorbed by the bias currents of the system components. $R_{(BAT)}$ equal to 100 k results in a worst-case voltage drop of $R_{(BAT)} \times I_{(VBAT)} \approx 1$ mV. This is negligible compared to the internal tolerance of 50 mV on the BV_{OVP} threshold.

If the Bat-OVP function is not required, the VBAT pin must be connected to VSS.

Selection of $R_{(CE)}$

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left unconnected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As with the VBAT pin (see previous discussion), the $\overline{CE}$ pin must be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum V_{OH} of the host GPIO pin less the drop across the resistor must be greater than V_{IH} of the bq2430x $\overline{CE}$ pin. The drop across the resistor is given by $R_{(CE)} \times I_{IH}$.

Selection of Input and Output Bypass Capacitors

The input capacitor C_{IN} in Figure 17 is for decoupling and serves an important purpose. Whenever a step change downwards in the system load current occurs, the inductance of the input cable causes the input voltage to spike up. C_{IN} prevents the input voltage from overshooting to dangerous levels. It is recommended that a ceramic capacitor of at least 1 µF be used at the input of the device. It must be located in close proximity to the IN pin.

C_{OUT} in Figure 17 is also important. During an overvoltage transient, this capacitance limits the output overshoot until the power FET is turned off by the overvoltage protection circuitry. C_{OUT} must be a ceramic capacitor of at least 1 µF, located close to the OUT pin. C_{OUT} also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

PCB Layout Guidelines

1. This device is a protection device and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected

PACKAGING INFORMATION

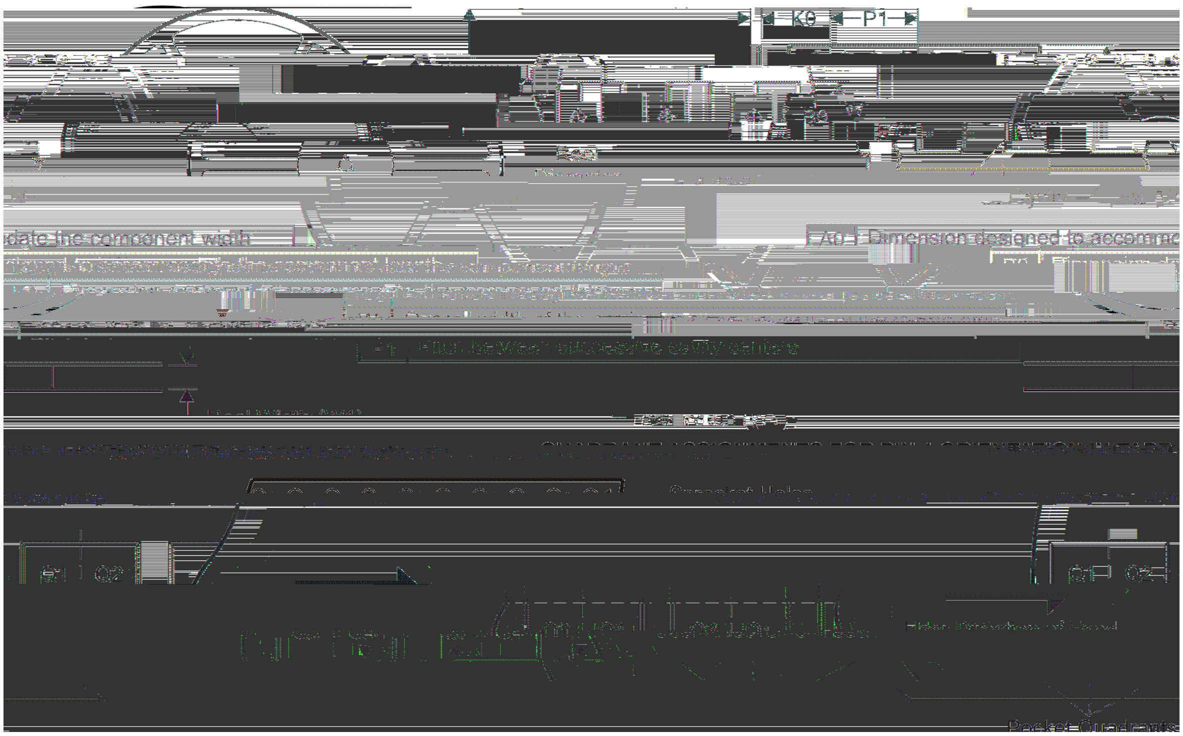
Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ24380DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24380DSGRG4	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24380DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24380DSGTG4	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24381DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24381DSGRG4	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24381DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24381DSGTG4	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24382DSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24382DSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and

TAPE AND REEL INFORMATION

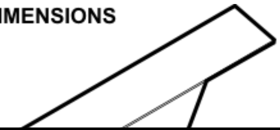
REEL DIMENSIONS **TAPE DIMENSIONS**



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24380DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24380DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24381DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24381DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24382DSGR	WSON	DSG	8	3000	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2
BQ24382DSGT	WSON	DSG	8	250	179.0	8.4	2.2	2.2	1.2	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

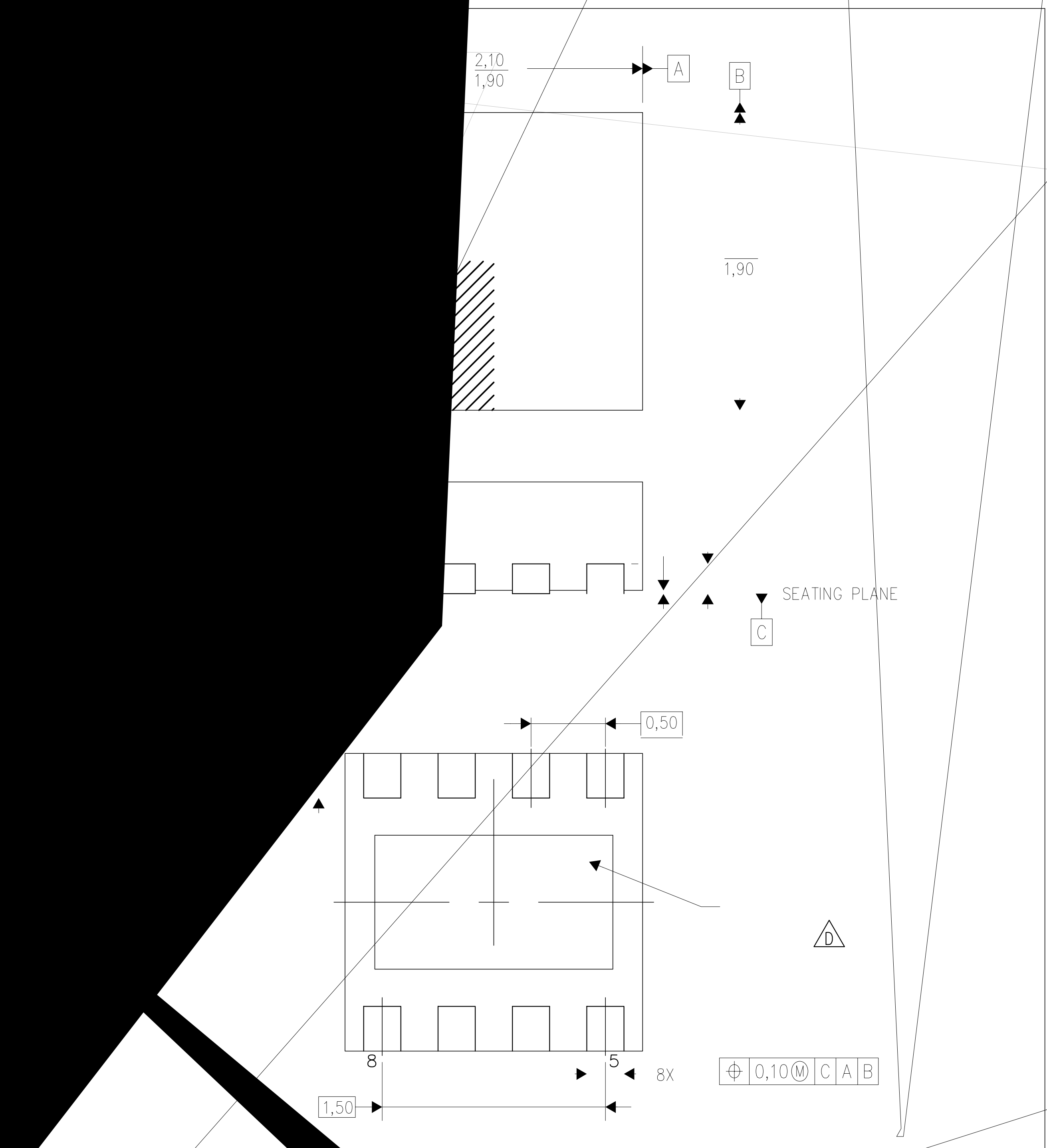


[redacted]

[redacted]	Length (mm)	Width (mm)	Height (mm)

[redacted]

PLASTIC SMALL OUTLINE NO-LEAD



[redacted]OTES: A. All linear dimensions are [redacted]eters. Dimensioning and tolerancing per ASME Y14.5M–1994.

B. This drawing is subject to c[redacted]ithout notice.

C. Quad Flatpack, No–Leads (QFN) [redacted]e configuration.

D. The package thermal pad must be [redacted]d to the board for thermal and mechanical performance. See the Product Data Sheet for deta[redacted]ling the exposed thermal pad dimensions.


CALD

[redacted] AND PATT[redacted]A

PL[redacted]UTL[redacted]—LEAD[redacted]

[redacted]5

[redacted]0.[redacted]

[redacted]08774/E 11/10

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IMPORTANT NOTICE