PROCESSOR SUPERVISORY CIRCUITS WITH WINDOW-WATCHDOG

FEATURES

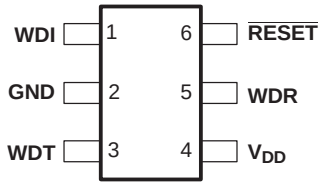
- **Controlled Baseline**
  - **One Assembly/Test Site, One Fabrication Site**
- **Extended Temperature Performance of -55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree** (1)
- **Window-Watchdog With Programmable Delay and Window Ratio**
- **6-Pin SOT-23 Package**
- **Supply Current of 9 μA (Typ)**
- **Power On Reset Generator With a Fixed Delay Time of 25 ms**
- **Precision Supply Voltage Monitor 2.5 V, 3 V, 3.3 V, 5 V**
- **Open-Drain Reset Output**

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

APPLICATIONS

- **Applications Using DSPs, Microcontrollers, or Microprocessors**
- **Safety Critical Systems**
- **Automotive Systems**
- **Healing Systems**

TPS3813
DBV PACKAGE
(TOP VIEW)



ACTUAL SIZE
3,00 mm x 3,00 mm

DESCRIPTION

The TPS3813 family of supervisory circuits provides circuit initialization and timing supervision, primarily for DSPs and processor-based systems.

During power on, $\overline{\text{RESET}}$ is asserted when supply voltage (V_{DD}) becomes higher than 1.1 V. Thereafter, the supervisory circuit monitors V_{DD} and keeps $\overline{\text{RESET}}$ active as long as V_{DD} remains below the threshold voltage (V_{IT}). An internal timer delays the return of the output to the inactive state (high) to ensure proper system reset. The delay time, t_d = 25 ms typical, starts after V_{DD} has risen above the threshold voltage (V_{IT}). When the supply voltage drops below the threshold voltage (V_{IT}), the output becomes active (low) again. No external components are required. All the devices of this family have a fixed-sense threshold voltage (V_{IT}) set by an internal voltage divider.

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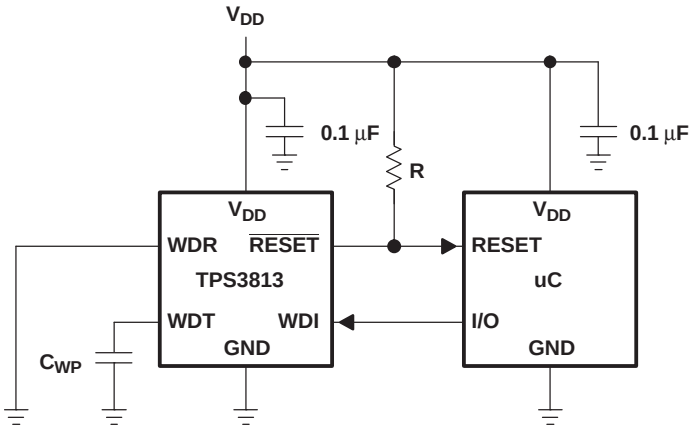
TYPICAL OPERATING CIRCUIT



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

For safety critical applications the TPS3813 family incorporates a so-called window-watchdog with programmable delay and window ratio. The upper limit of the watchdog time-out can be set by either connecting WDT to GND, V_{DD}, or using an external capacitor. The lower limit and thus the window ratio is set by connecting WDR to GND or V_{DD}. The supervised processor now needs to trigger the TPS3813 within this window not to assert a $\overline{\text{RESET}}$.

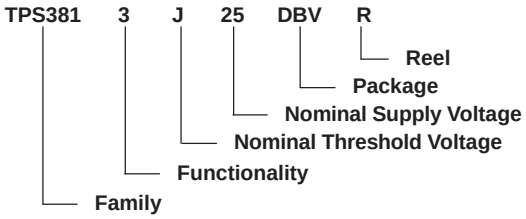
The product spectrum is designed for supply voltages of 2.5 V, 3 V, 3.3 V, and 5 V. The circuits are available in a 6-pin SOT-23 package.

The TPS3813 devices are characterized for operation over a temperature range of –55°C to 125°C.

PACKAGE INFORMATION

T_A	DEVICE NAME	THRESHOLD VOLTAGE	MARKING
–55°C to 125°C	TPS3813J25MDBVREP	2.25 V	PLEM
	TPS3813L30MDBVREP	2.64 V	PLFM
	TPS3813K33MDBVREP	2.93 V	PLGM
	TPS3813I50MDBVREP	4.55 V	PLHM

ORDERING INFORMATION



TPS3813 FUNCTION/TRUTH TABLE

$V_{DD} > V_{IT}$	$\overline{\text{RESET}}$
0	L
1	H

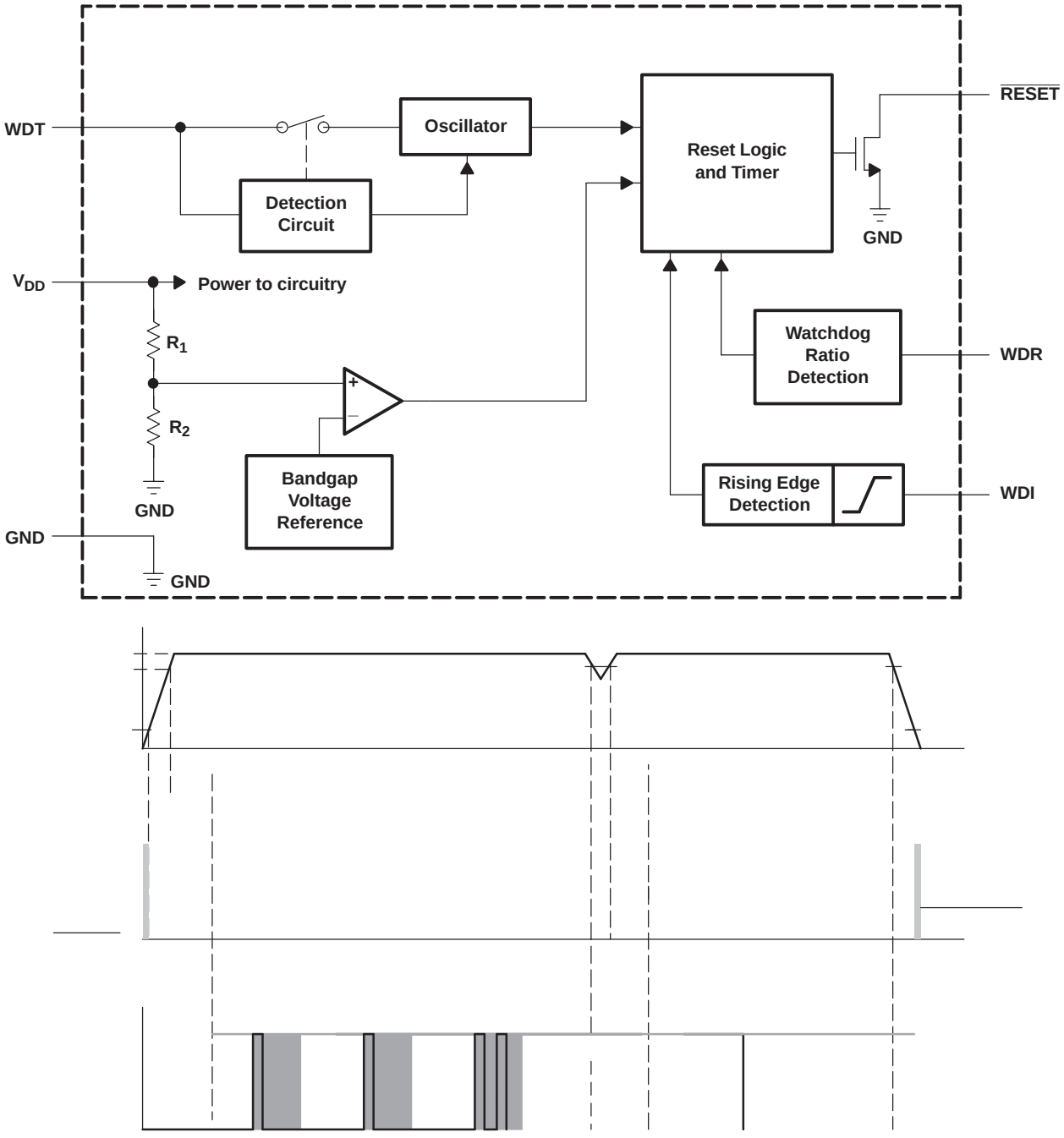


Figure 1. Timing Diagram

The lower boundary of the watchdog window starts with the rising edge of the WDI trigger pulse. At the same time, all internal timers will be reset. If an external capacitor is used, the lower boundary is impacted due to the different oscillator frequency. This is described in more detail in the following section. The timing diagram and especially the shaded boundary is prepared in a nonreal ratio scale to better visualize the description.

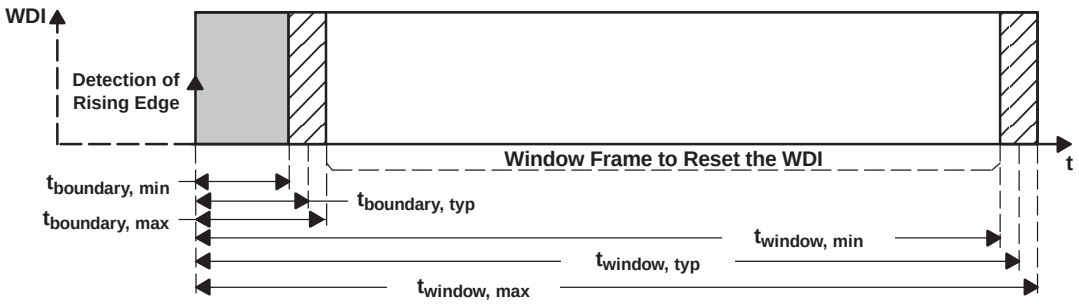
Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
GND	2	I	Ground
$\overline{\text{RESET}}$	6	O	Open-drain reset output
V_{DD}	4	I	Supply voltage and supervising input
WDI	1	I	Watchdog timer input
WDR	5	I	Selectable watchdog window ratio input
WDT	3	I	Programmable watchdog delay input

DETAILED DESCRIPTION

IMPLEMENTED WINDOW-WATCHDOG SETTINGS

There are two different ways to set up the watchdog window. The first way is to use the implemented timing which is a default setting. Or, the default settings can be activated by wiring the WDT and



TIMING RULES OF WINDOW-WATCHDOG

After the reset of the supervisor is released, the lower boundary of the first WDI window is disabled. However, after the first WDI pulse low-to-high transition is detected, the lower boundary function of the window is enabled. All further WDI pulses will need to fit into the configured window frame.

PROGRAMMABLE WINDOW-WATCHDOG BY USING AN EXTERNAL CAPACITOR

The upper boundary of the watchdog timer can be set by an external capacitor connected between the

$$t_{window,typ} = \left(\frac{C_{(ext)}}{15.55\ pF} + 1 \right) \times 6.25\ ms \quad (1)$$

LOWER BOUNDARY CALCULATION

WATCHDOG SOFTWARE CONSIDERATIONS

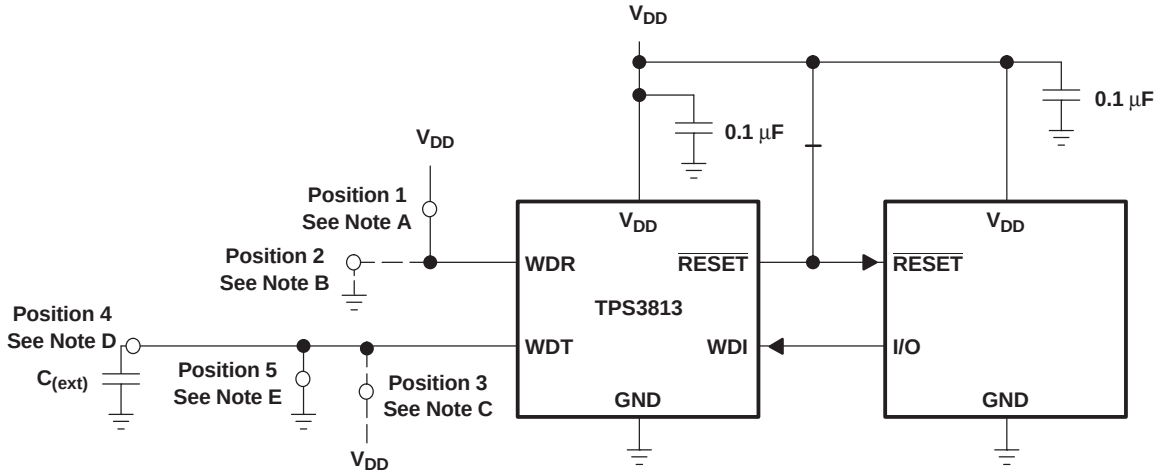
APPLICATION EXAMPLE

If the window watchdog ratio pin (WDR) is set to V_{DD}, Position 1 in Figure 3, then the lower window frame is a value based on a ratio calculation of the overall window timeout size: For the watchdog timeout pin (WDT) connected to GND, it is a ratio of 1:124.9, for WDT connected to V_{DD}, it is a ratio of 1:127.7, and for an external capacitor connected to WDT, it is a ratio of 1:64.5.

If the window watchdog ratio pin (WDR) is set to GND, Position 2, the lower window frame will be a value based on a ratio calculation of the overall window timeout size: For the watchdog timeout pin (WDT) connected to GND, it will be a ratio of 1:31.8, for WDT connected to V_{DD} it will be 1:32, and for an external capacitor connected to WDT it will be 1:25.8.

The watchdog timeout can be set in two fixed timings of 0.25 seconds and 2.5 seconds for the window or can by programmed by connecting a external capacitor with a low leakage current at WDT.

Example: If the watchdog timeout pin (WDT) is connected to V_{DD}, the timeout will be 2.5 seconds. If the window watchdog ratio pin (WDR) is set in this configuration to a ratio of 1:127.7 by connecting the pin to V_{DD}, the lower boundary is 19.6 ms.



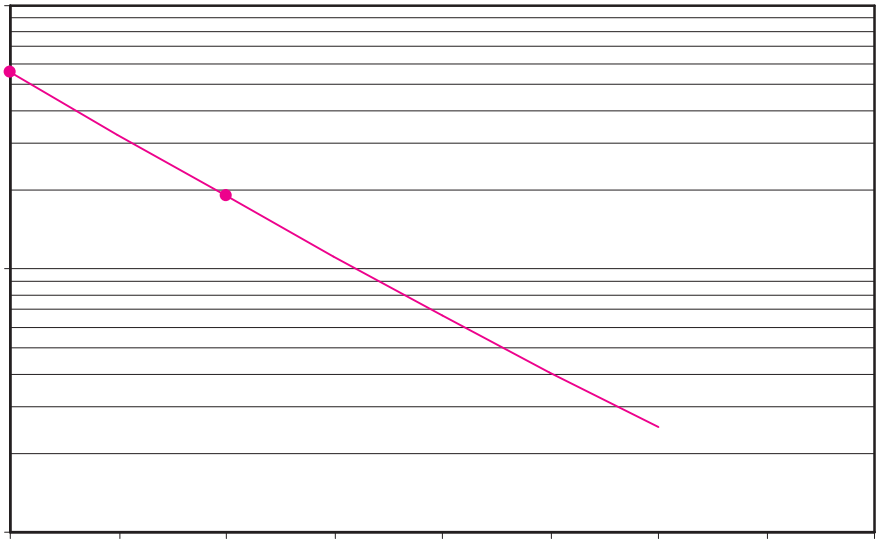
A. Watchdog window ratio
B. Watchdog timeout set to typical 2.5 sec
C. Watchdog timeout programmed by external capacitor
D. Watchdog timeout set to typical 0.25 sec

Figure 3. Application Example

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

		UNIT
V_{DD}	Supply voltage(2)	7 V
	RESET	–0.3 V to V_{DD} + 0.3 V
	All other pins7	



SWITCHING CHARACTERISTICS

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENT vs INPUT VOLTAGE AT WDT

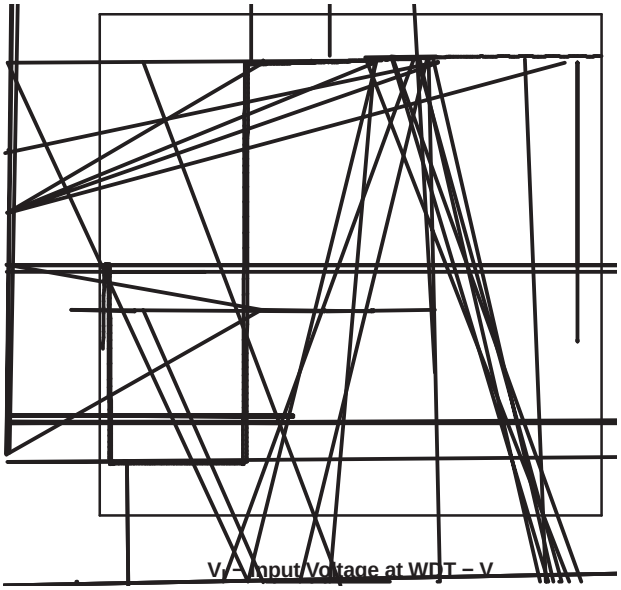


Figure 7.

NORMALIZED INPUT THRESHOLD VOLTAGE vs FREE-AIR TEMPERATURE AT V_{DD}

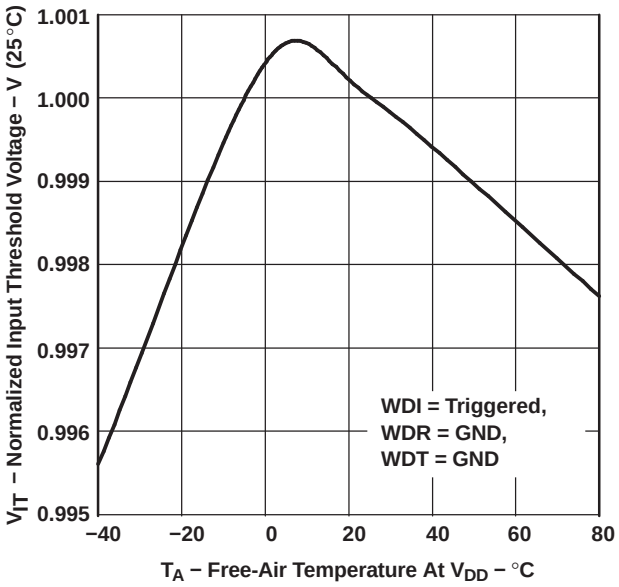


Figure 8.

MINIMUM PULSE DURATION AT V_{DD} vs V_{DD} THRESHOLD OVERDRIVE VOLTAGE

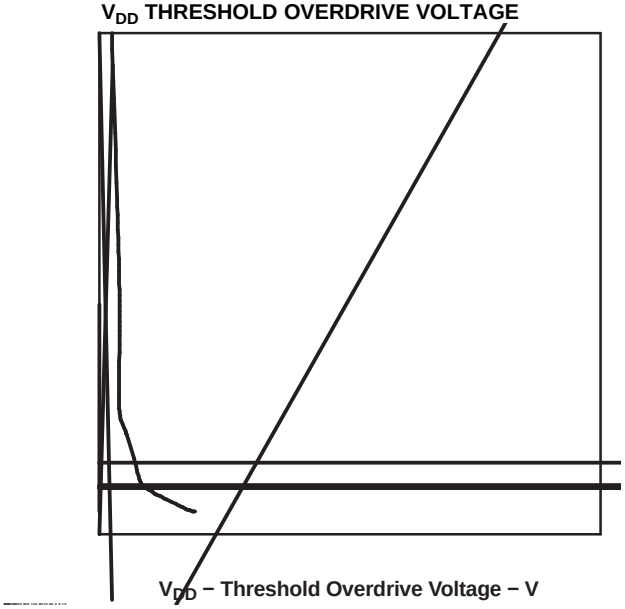


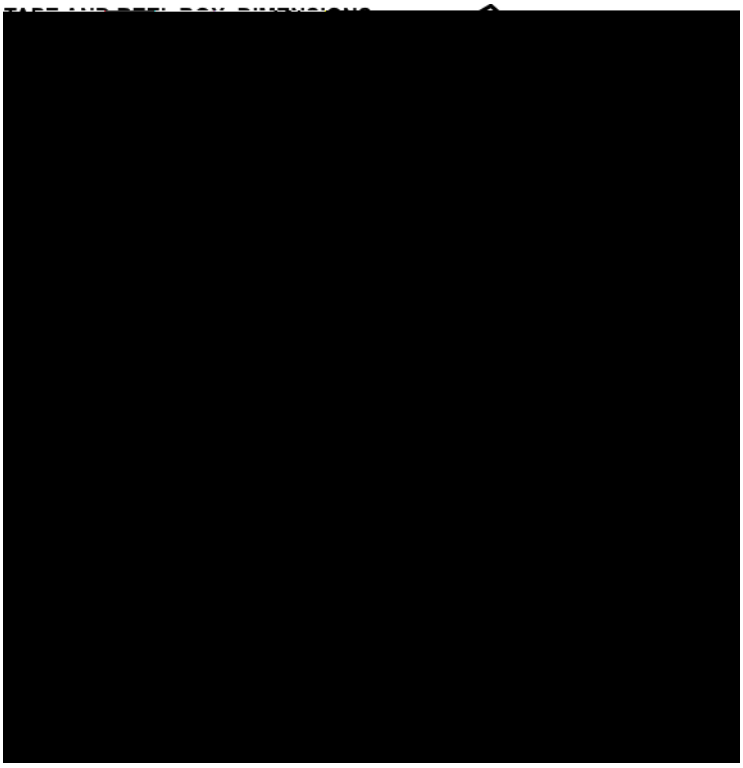
Figure 9.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
2T13K33MDBVREPG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TPS3813K33MDBVREP	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
V62/06627-01XE	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

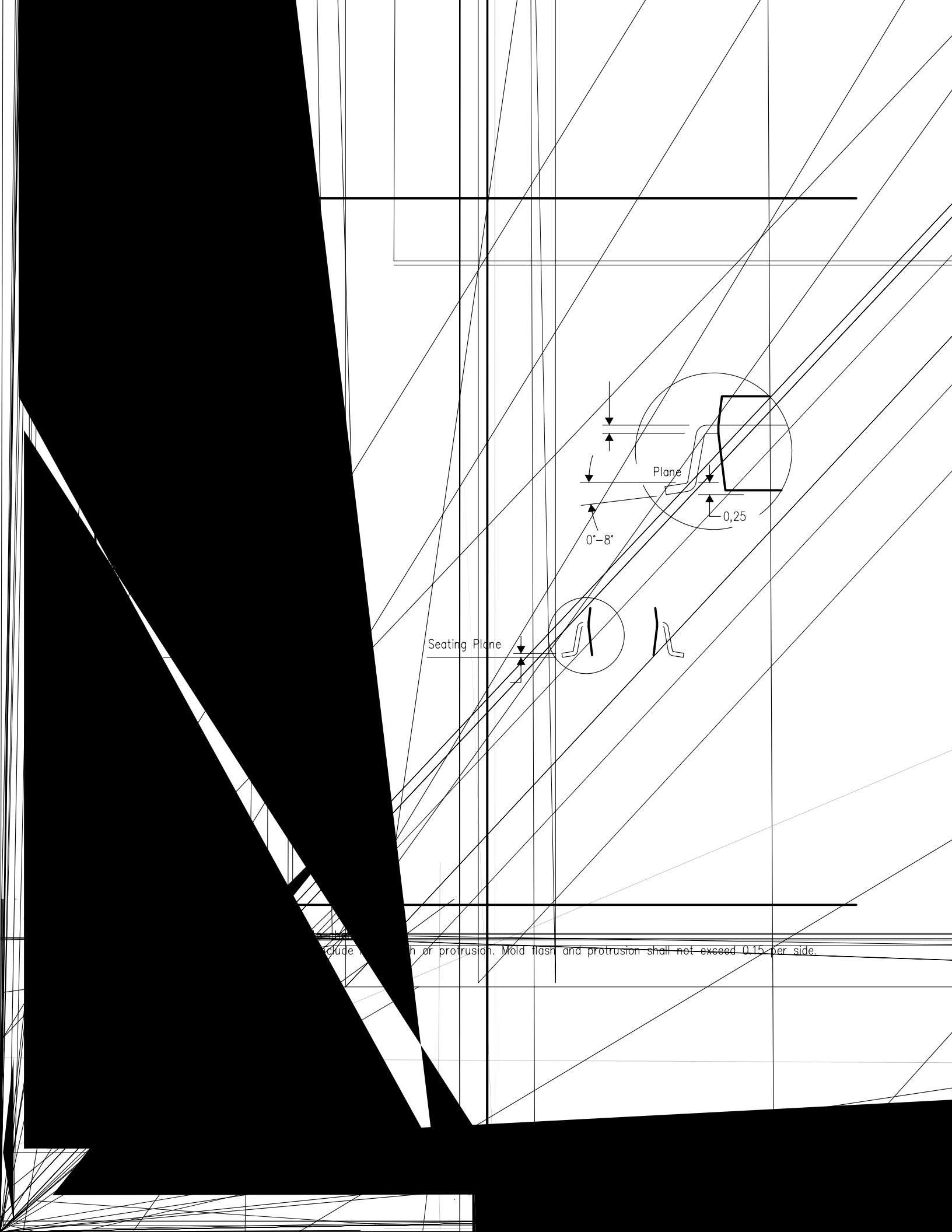
[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and



*All dimensions are nominal

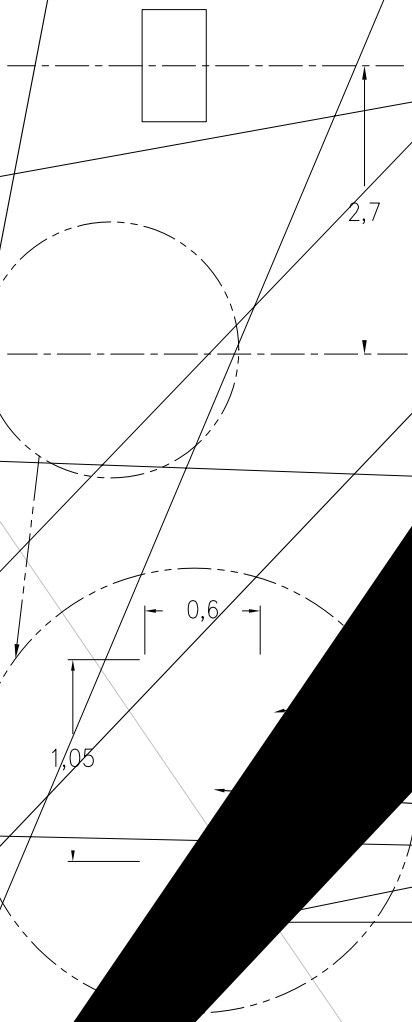
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3813K33MDBVREP	SOT-23	DBV	6	3000	182.0	182.0	20.0



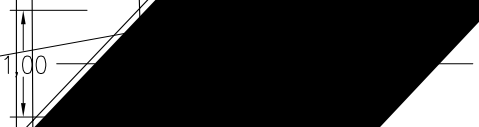
clude mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.

DBV (R-PDSO-G6) PLASTIC SMALL

Example Board Layout



Stencil Op
Based on a s
of .127m



der Mask Opening

Pad Geometry

4209593-4/C 08/11

NOTES: A. mensions are in millimeters.
B. ng is subject to change without notice.
C. ers should place a note on the circuit board fabricatic ~~er mask defined pad.~~
ication IPC-7351 is recommended for alternate designs.

~~contact their board assembly site for stencil design recommendations.~~ vill offer better paste release. Customers should
metal load solder paste. Example stencil design based on a 50% volumetric

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