

SBS 1.1-COMPLIANT GAS GAUGE AND PROTECTION-ENABLED IC WITH IMPEDANCE TRACK™

Check for Samples: [bq20z75-V180](#)

FEATURES

- **Next Generation Patented Impedance Track™ Technology accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries**
 - Better than 1% Error Over Lifetime of the Battery
 - Instant Accuracy – No Learning Cycle Required
- **Supports the Smart Battery Specification SBS V1.1**
- **Flexible Configuration for 2 to 4 Series Li-Ion and Li-Polymer Cells**
- **Powerful 8-Bit RISC CPU With Ultra-Low Power Modes**
- **Full Array of Programmable Protection Features**
 - Voltage, Current and Temperature
- **Supports SHA-1 Authentication**
- **small 38-Pin TSSOP (DBT) Package**

APPLICATIONS

- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq20z75-V180 SBS-compliant gas gauge and protection IC is a single IC solution designed for battery-pack or in-system installation. The bq20z75-V180 measures and maintains an accurate record of available charge in Li-ion or Li-polymer batteries using its integrated high-performance analog peripherals, monitors capacity change, battery impedance, open-circuit voltage, and other critical parameters of the battery pack as well and reports the information to the system host controller over a serial-communication bus. Together with the integrated analog front-end (AFE) short-circuit and overload protection the bq20z75-V180 maximizes functionality, safety and minimize external component count, cost and size in smart battery circuits.

The implemented Impedance Track™ gas gauging technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables remaining capacity to be calculated with discharge rate, temperature, and cell aging all accounted for during each stage of every cycle with high accuracy.

Table 1. AVAILABLE OPTIONS

T _A	PACKAGE	
	38-PIN TSSOP (DBT) Tube ⁽¹⁾	38-PIN TSSOP (DBT) Tape and Reel ⁽²⁾
–40°C to 85°C	bq20z75DBT	bq20z75DBTR
	bq20z75DBT-V160	bq20z75DBTR-v160
	bq20z75DBT-v180	bq20z75DBTR-v180

(1) A single tube quantity is 50 units.

(2) A single reel quantity is 2000 units

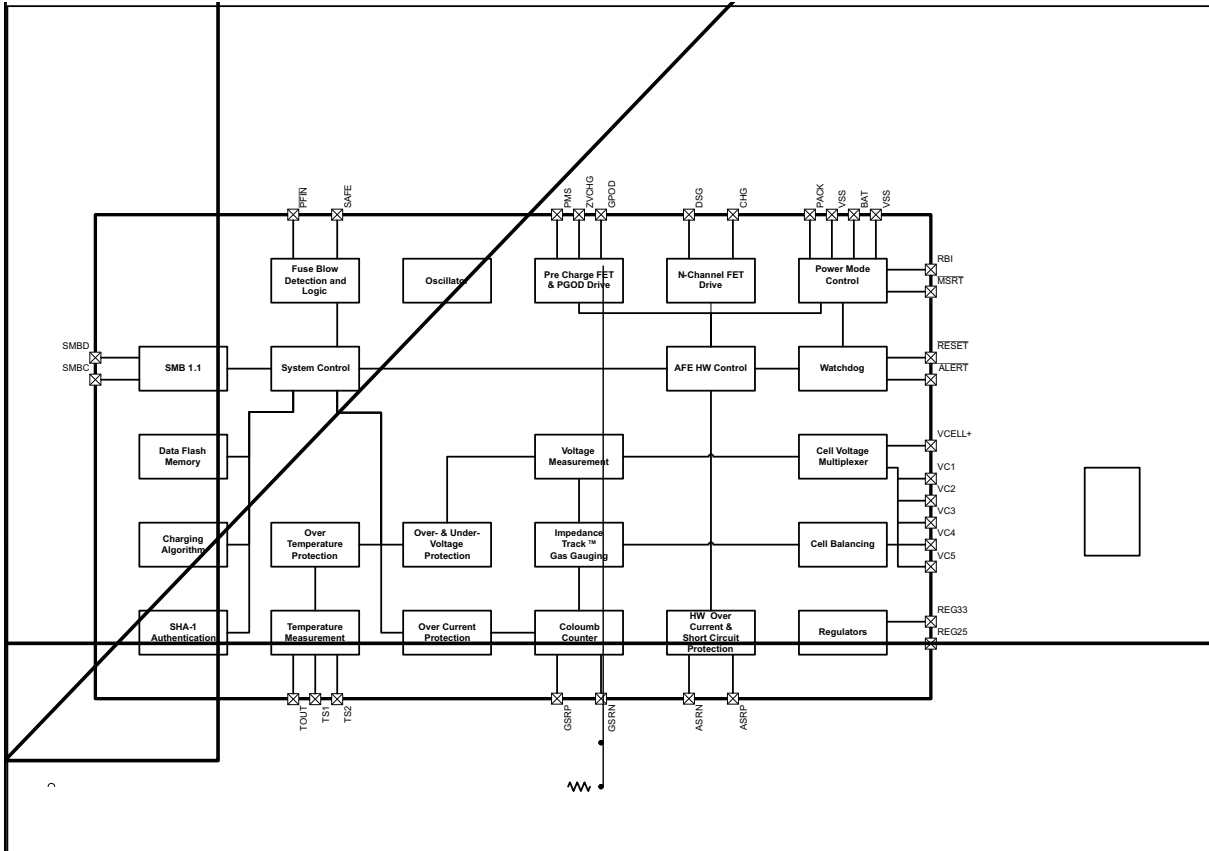


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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

SYSTEM PARTITIONING DIAGRAM



TSSOP (PW)
(TOP VIEW)

DSG	1	38	CHG
PACK	2	37	BAT
VCC	3	36	VC1
ZVCHG	4	35	VC2
GPOD	5	34	VC3
PMS	6	33	VC4
VSS	7	32	VC5
REG33	8	31	ASRP
TOUT	9	30	ASRN
VCELL+	10	29	RESET
ALERT	11	28	VSS
PRES	12	27	RBI
TS1	13	26	REG25
TS2	14	25	VSS
PFIN	15	24	MRST
SAFE	16	23	GSRN
SMBD	17	22	GSRP
SMBC	18	21	VSS
NC	19	20	VSS

TERMINAL FUNCTIONS

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	DSG	O	High side N-channel discharge FET gate drive
2	PACK	IA, P	Battery pack input voltage sense input. It also serves as device wake up when device is in shutdown mode.
3	VCC	P	Positive device supply input. Connect to the center connection of the CHG FET and DSG FET to ensure device supply either from battery stack or battery pack input
4	ZVCHG	O	P-channel pre-charge FET gate drive
5	GPOD	OD	High voltage general purpose open drain output. Can be configured to be used in pre-charge condition
6	PMS	I	Pre-charge mode setting input. Connect to PACK to enable 0v pre-charge using charge FET connected at CHG pin. Connect to VSS to disable 0V pre-charge using charge FET connected at CHG pin.
7	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device
8	REG33	P	3.3V regulator output. Connect at least a 2.2µF capacitor to REG33 and VSS
9	TOUT	P	Termistor bias supply output
10	VCELL+	-	Internal cell voltage multiplexer and amplifier output. Connect a 0.1µF capacitor to VCELL+ and VSS
11	$\overline{\text{ALERT}}$	I/OD	Alert output. In case of short circuit condition, overload condition and watchdog time out this pin will be triggered.
12	$\overline{\text{PRES}}$	I/OD	System / Host present input. Pull up to TOUT
13	TS1	IA	Temperature sensor 1 input
14	TS2	IA	Temperature sensor 2 input
15	$\overline{\text{PFIN}}$	I/OD	Fuse blow detection input
16	SAFE	I/OD	blow fuse signal output
17	SMBD	I/OD	SMBus data line
18	SMBC	I/OD	SMBus clock line
19	NC	-	Not Connected
20	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device.
21	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device.
22	GSRP	IA	Coulomb counter differential input. Connect to one side of the sense resistor
23	GSRN	IA	Coulomb counter differential input. Connect to one side of the sense resistor
24	$\overline{\text{MRST}}$	I	Reset input for internal CPU core. connect to $\overline{\text{RESET}}$ for correct operation of device.
25	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device.
26	REG25	P	2.5V regulator output. Connect at least a 1µF capacitor to REG25 and VSS
27	RBI	P	RAM backup input. Connect a capacitor to this pin and VSS to protect loss of RAM data in case of short-circuit condition
28	VSS	P	Negative device power supply input. Connect all VSS pins together for operation of device
29	$\overline{\text{RESET}}$	O	Reset output. Connect to $\overline{\text{MRST}}$.
30	ASRN	IA	Short-circuit and overload detection differential input
31	ASRP	IA	Short-circuit and overload detection differential input
32	VC5	IA,P	Cell voltage sense input and cell balancing input for the negative voltage of the bottom cell in cell stack.
33	VC4	IA,P	Cell voltage sense input and cell balancing input for the positive voltage of the bottom cell and the negative voltage of the second lowest cell in cell stack.
34	VC3	IA,P	Cell voltage sense input and cell balancing input for the positive voltage of the second lowest cell in cell stack and the negative voltage of the second highest cell in 4 cell applications.
35	VC2	IA,P	Cell voltage sense input and cell balancing input for the positive voltage of the second highest cell and the negative voltage of the highest cell in 4 cell applications. Connect to VC3 in 2 cell stack applications
36	VC1	IA,P	Cell voltage sense input and cell balancing input for the positive voltage of the highest cell in cell stack in 4 cell applications. Connect to VC2 in 3 or 2 cell stack applications

(1) I = Input, IA = Analog input, I/O = Input/output, I/OD = Input/Open-drain output, O = Output, OA = Analog output, P = Power

TERMINAL FUNCTIONS (continued)

TERMINAL		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
37	BAT	O	Battery stack voltage sense input
38	CHG	O	High side N-channel charge FET gate drive

Absolute Maximum RatingsOver Operating Free-Air Temperature (unless otherwise noted) ⁽¹⁾

	DESCRIPTION	PIN	UNIT
V _{MAX}	Supply voltage range	VBAT, VCC	–0.3V to 34V
		PACK, PMS	–0.3V to 34V
		VC(n)-VC(n+1); n = 1, 2, 3, 4	–0.3V to 8.5V
		VC1, VC2, VC3, VC4	–0.3V to 34V
V _{IN}	Input voltage range	VC5	–0.3V to 1.0V
		$\overline{\text{PFIN}}$, SMBD, SMBC, DISP	–0.3V to 6.0V
		TS1, TS2, VCELL+, PRES; ALERT	–0.3 V to V _{REG25} + 0.3 V
		$\overline{\text{MRST}}$, GSRN, GSRP, RBI	–0.3 V to V _{REG25} + 0.3 V
		ASRN, ASRP	–1.0V to 1.0V
V _{OUT}	Output voltage range	DSG, CHG, GPOD	–0.3V to 34V
		ZVCHG	–0.3V to V _{BAT}
		TOUT, $\overline{\text{ALERT}}$, REG33,	–0.3 V to 6.0V
		$\overline{\text{RESET}}$	–0.3 V to 7.0V
		REG25, SAFE, TOUT	–0.3V to 2.75V
I _{SS}	Maximum combined sink current for input pins	$\overline{\text{PRES}}$, $\overline{\text{PFIN}}$, SMBD, SMBC	50mA
T _A	Operating free-air temperature range		–40°C to 85°C
T _F	Functional temperature		–40°C to 100°C
T _{stg}	Storage temperature range		–65°C to 150°C
T _{sld}	Lead temperature (soldering, 10s)		300°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		PIN	MIN	NOM	MAX	UNIT
V _{SUP}	Supply voltage	VCC, VBAT	4.5		25	V
V _{STARTUP}	Minimum startup voltage	VCC, BAT, PACK	5.5			V
V _{IN}	Input Voltage Range	VC(n)–VC(n+1); n = 1,2,3,4	0		5	V
		VC1, VC2, VC3, VC4	0		V _{SUP}	V
		VC5	0		0.5	V
		ASRN, ASRP	–0.5		0.5	V
		PACK, PMS	0		25	V
V _{GPOD}	Output Voltage Range	GPOD	0		25	V
A _{GPOD}	Drain Current ⁽¹⁾	GPOD			1	mA
C _{REG25}	2.5V LDO Capacitor	REG25	1			μF
C _{REG33}	3.3V LDO Capacitor	REG33	2.2			μF
C _{VCELL+}	Cell Voltage Output Capacitor	VCELL+	0.1			μF
C _{PACK}	PACK input block resistor ⁽²⁾	PACK	1			kΩ

(1) Use external resistor to limit current to GPOD to 1mA in high voltage application.

(2) External resistor to limit inrush current PACK pin required.

Electrical Characteristics

 over operating free-air temperature range (unless otherwise noted), T_A = –40°C to 85°C, V_{REG25} = 2.41 V to 2.59 V, V_{BAT} = 14V, C_{REG25} = 1μF, C_{REG33} = 2.2μF; typical values at T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I _{NORMAL}	Firmware running			550		μA
I _{SLEEP}	Sleep Mode	CHG FET on; DSG FET on		124		μA
		CHG FET off; DSG FET on		90		μA
		CHG FET off; DSG FET off		52		μA
I _{SHUTDOWN}	Shutdown Mode			0.1	1	μA
SHUTDOWN WAKE; T_A = 25°C (unless otherwise noted)						
I _{PACK}	Shutdown exit at V _{STARTUP} threshold				1	μA
SRx WAKE FROM SLEEP; T_A = 25°C (unless otherwise noted)						
V _{WAKE}	Positive or negative wake threshold with 1.00 mV, 2.25 mV, 4.5 mV and 9 mV programmable options		1.25		10	mV
V _{WAKE_ACR}	Accuracy of V _{WAKE}	V _{WAKE} = 1.0mV; IWAKE=0, RSNS1=0, RSNS0=1;	–0.7		0.7	mV
		V _{WAKE} = 2.25mV; IWAKE =1, RSNS1=0, RSNS0=1; IWAKE =0, RSNS1=1, RSNS0=0;	–0.8		0.8	
		V _{WAKE} = 4.5mV; IWAKE =1, RSNS1=1, RSNS0=1; IWAKE =0, RSNS1=1, RSNS0=0;	–1.0		1.0	
		V _{WAKE} = 9mV; IWAKE =1, RSNS1=1, RSNS0=1;	–1.4		1.4	
V _{WAKE_TCO}	Temperature drift of V _{WAKE} accuracy			0.5		%/°C
t _{WAKE}	Time from application of current and wake of bq20z75-V180			1	10	ms
POWER-ON RESET						
V _{IT–}	Negative-going voltage input	Voltage at REG25 pin	1.70	1.80	1.90	V

Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted), $T_A = -40^{\circ}\text{C}$ to 85°C , $V_{\text{REG25}} = 2.41\text{ V}$ to 2.59 V , $V_{\text{BAT}} = 14\text{ V}$, $C_{\text{REG25}} = 1\mu\text{F}$, $C_{\text{REG33}} = 2.2\mu\text{F}$; typical values at $T_A = 25^{\circ}\text{C}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
$f_{(\text{EIO})}$ Frequency error ⁽¹²⁾ (13)		-3%	0.25%	3%	
	$T_A = 20^{\circ}\text{C}$ to 70°C	-2%	0.25%	2%	
$t_{(\text{SXO})}$ Start-up time ⁽¹⁴⁾			2.5	5	ms
LOW FREQUENCY OSCILLATOR					
$f_{(\text{LOSC})}$ Operating frequency			32.768		kHz
$f_{(\text{LEIO})}$ Frequency error ⁽¹³⁾ (15)		-2.5%	0.25%	2.5%	
	$T_A = 20^{\circ}\text{C}$ to 70°C	-1.5%	0.25%	1.5%	
$t_{(\text{LSXO})}$ Start-up time ⁽¹⁴⁾				500	μs

(12) The frequency error is measured from 4.194 MHz.

(13) The frequency drift is included and measured from the trimmed frequency at $V_{\text{REG25}} = 2.5\text{ V}$, $T_A = 25^{\circ}\text{C}$

(14) The startup time is defined as the time it takes for the oscillator output frequency to be $\pm 3\%$

(15) The frequency error is measured from 32.768 kHz.

Data Flash Characteristics Over Recommended Operating Temperature and Supply Voltage

Typical Values at $T_A = 25^{\circ}\text{C}$ and $V_{\text{REG25}} = 2.5\text{ V}$ (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Data retention		10			Years
Flash programming write-cycles		20k			Cycles
$t_{(\text{ROWPROG})}$ Row programming time	See ⁽¹⁾			2	ms
$t_{(\text{MASSERASE})}$ Mass-erase time				200	ms
$t_{(\text{PAGEERASE})}$ Page-erase time				20	ms
$I_{(\text{DDPROG})}$ Flash-write supply current				5	10
$I_{(\text{DDERASE})}$ Flash-erase supply current			5	10	mA
RAM BACKUP					
$I_{(\text{RB})}$ RB data-retention input current	$V_{(\text{RBI})} > V_{(\text{RBI})\text{MIN}}$, $V_{\text{REG25}} < V_{\text{IT-}}$, $T_A = 85^{\circ}\text{C}$		1000	2500	nA
	$V_{(\text{RBI})} > V_{(\text{RBI})\text{MIN}}$, $V_{\text{REG25}} < V_{\text{IT-}}$, $T_A = 25^{\circ}\text{C}$		90	220	
$V_{(\text{RB})}$ RB data-retention input voltage ⁽¹⁾		1.7			V

(1) Assured by design. Not production tested.

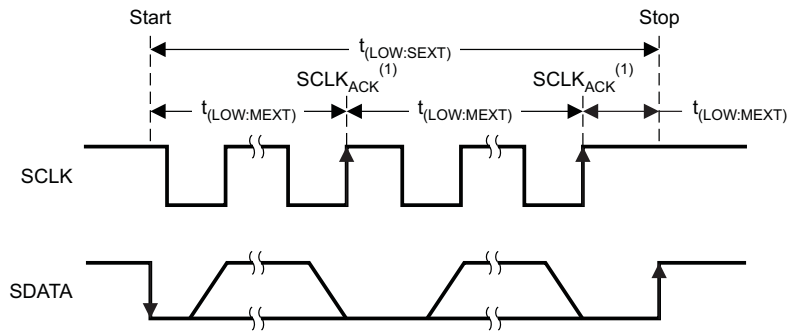
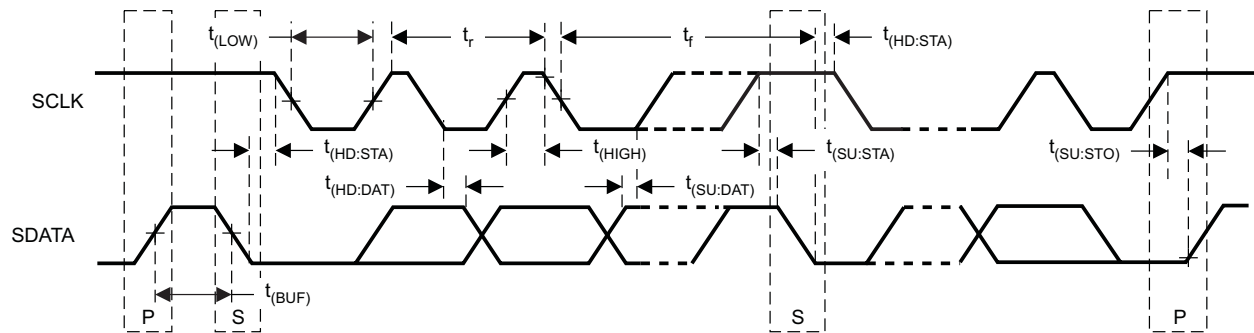
SMBus Timing Characteristics

$T_A = -40^{\circ}\text{C}$ to 85°C Typical Values at $T_A = 25^{\circ}\text{C}$ and $V_{(\text{REG25})} = 2.5\text{ V}$ (Unless Otherwise Noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SMB} SMBus operating frequency	Slave mode, SMBC 50% duty cycle	10		100	kHz
f_{MAS} SMBus master clock frequency	Master mode, No clock low slave extend		51.2		kHz
$t_{(\text{BUF})}$ Bus free time between start and stop (see Figure 1)		4.7			μs
$t_{(\text{HD:STA})}$ Hold time after (repeated) start (see Figure 1)		4.0			μs
$t_{(\text{SU:STA})}$ Repeated start setup time (see Figure 1)		4.7			μs
$t_{(\text{SU:STO})}$ Stop setup time (see Figure 1)		4.0			μs
$t_{(\text{HD:DAT})}$ Data hold time (see Figure 1)	Receive mode	0			ns
	Transmit mode	300			
$t_{(\text{SU:DAT})}$ Data setup time (see Figure 1)		250			ns

SMBus Timing Characteristics (continued)

$T_A = -40^\circ\text{C}$ to 85°C Typical $V_{DD} = 1.63\text{ V}$ $T_f = 3.6$ 0 $T_d(\text{C})$ $T_j = 9.251$ 0 0 $r_g(\text{Typical})$ $T_j = 31.2$ 0 T_d $T_j = 9.2$ 0 $T_d(\text{to})$ $T_j = 10.21$ 0 $T = 707.8$ $T_d(\text{SMBus})$ $T_j = 40.58$



FEATURE SET

Primary (1st Level) Safety Features

The bq20z75-V180 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/under voltage protection
 - Charge and Discharge over current
 - Short Circu
-

Power Modes

The bq20z75-V180 supports 3 different power modes to reduce power consumption:

- In Normal Mode, the bq20z75-V180 performs measurements, calculations, protection decisions and data updates in 1 second intervals. Between these intervals, the bq20z75-V180 is in a reduced power stage.
- In Sleep Mode, the bq20z75-V180 performs measurements, calculations, protection decisions and data update in adjustable time intervals. Between these intervals, the bq20z75-V180 is in a reduced power stage. The bq20z75-V180 has a wake function that enables exit from Sleep mode, when current flow or failure is detected.
- In Shutdown Mode the bq20z75-V180 is completely disabled.

CONFIGURATION

Oscillator Function

The bq20z75-V180 fully integrates the system oscillators. Therefore the bq20z75-V180 requires no external components for this feature.

System Present Operation

The bq20z75-V180 checks the $\overline{\text{PRES}}$ pin periodically (1 s). Connect the $\overline{\text{PRES}}$ pin to TOUT with a 100k Ω resistor. If $\overline{\text{PRES}}$ input is pulled to ground by external system host, the bq20z75-V180 detects this as system present.

BATTERY PARAMETER MEASUREMENTS

The bq20z75-V180 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage, and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The integrating ADC measures bipolar signals from -0.25 V to 0.25 V. The bq20z75-V180 detects charge activity when $V_{\text{SR}} = V_{(\text{SRP})} - V_{(\text{SRN})}$ is positive and discharge activity when $V_{\text{SR}} = V_{(\text{SRP})} - V_{(\text{SRN})}$ is negative. The bq20z75-V180 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh.

Voltage

The bq20z75-V180 updates the individual series cell voltages at one second intervals. The internal ADC of the bq20z75-V180 measures the voltage, scales and calibrates it appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track™ gas-gauging.

Current

The bq20z75-V180 uses the GSRP and GSRN inputs to measure and calculate the battery charge and discharge current using a 5 m Ω to 20 m Ω typ. sense resistor.

Auto Calibration

The bq20z75-V180 provides an auto-calibration feature to cancel the voltage offset error across GSRN and GSRP for maximum charge measurement accuracy. The bq20z75-V180 performs auto-calibration when the SMBus lines stay low continuously for a minimum of 5 s.

Temperature

The bq20z75-V180 has an internal temperature sensor and 2 external temperature sensor inputs TS1 and TS2 used in conjunction with two identical NTC thermistors (default are Semitec 103AT) to sense the battery environmental temperature. The bq20z75-V180 can be configured to use internal or external temperature sensors.

COMMUNICATIONS

The bq20z75-V180 uses SMBus v1.1 with Master Mode and package error checking (PEC) options per the SBS specification.

SMBus On and Off State

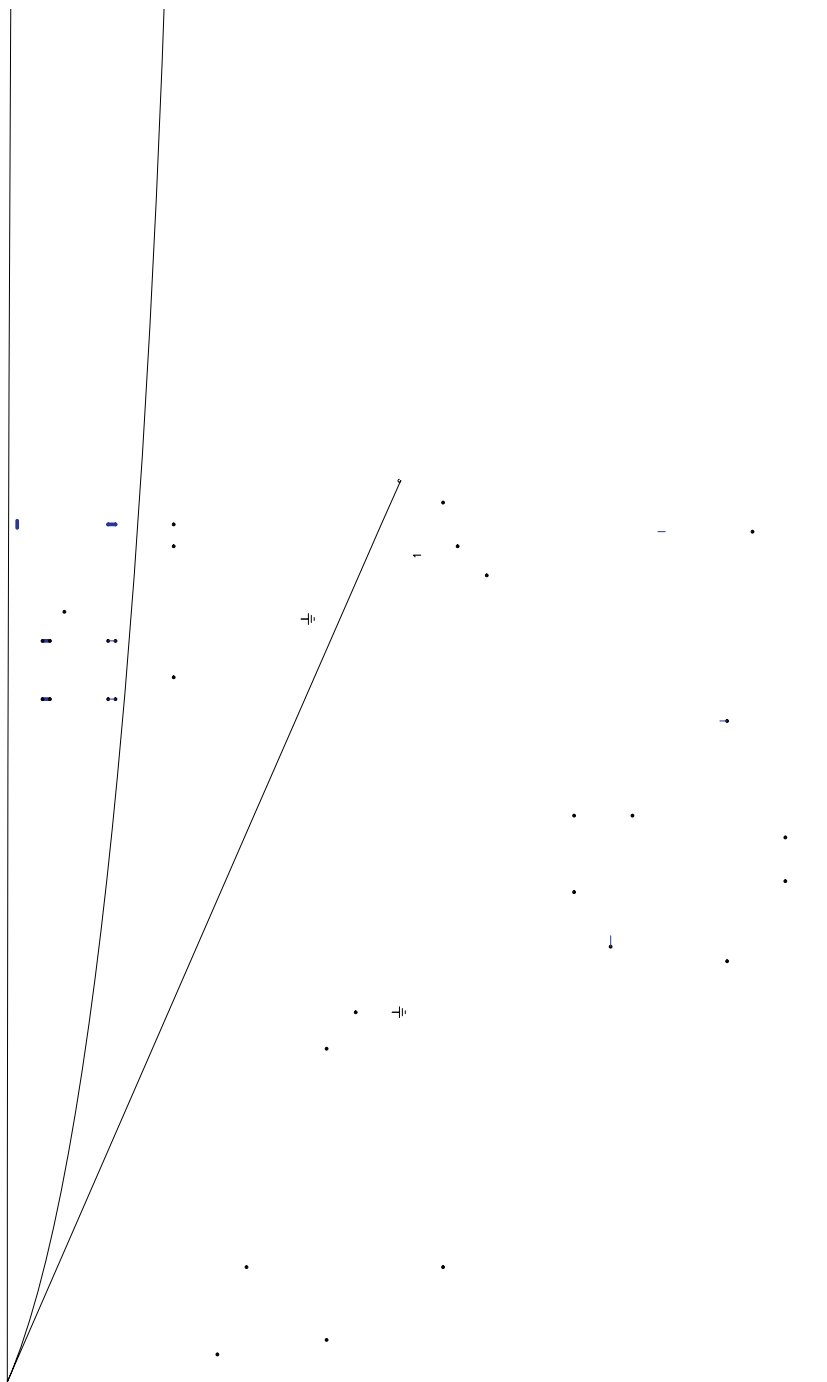
The bq20z75-V180 detects an SMBus off state when SMBC and SMBD are logic-low for ≥ 2 seconds. Clearing this state requires either SMBC or SMBD to transition high. Within 1 ms, the communication bus is available.

SBS and Dataflash Values

Table 2. SBS COMMANDS

SBS Cmd	Mode	Name	Format	Size in Bytes	Min Value	Max Value	Default Value	Unit
0x00	R/W	ManufacturerAccess	hex	2	0x0000	0xffff	—	
0x01	R/W	RemainingCapacityAlarm	unsigned int	2	0	65535	—	mAh or 10mWh
0x02	R/W	RemainingTimeAlarm	unsigned int	2	0	65535	—	min
0x03	R/W	BatteryMode	hex	2	0x0000	0xffff	—	
0x04	R/W	AtRate	signed int	2	-32768	32767	—	mA or 10mW
0x05	R	AtRateTimeToFull	unsigned int	2	0	65535	—	min
0x06	R	AtRateTimeToEmpty	unsigned int	2	0	65535	—	min
0x07	R	AtRateOK	unsigned int	2	0	65535	—	
0x08	R	Temperature	unsigned int	2	0	65535	—	0.1°K
0x09	R	Voltage	unsigned int	2	0	20000	—	mV
0x0a	R	Current	signed int	2	-32768	32767	—	mA
0x0b	R	AverageCurrent	signed int	2	-32768	32767	—	mA
0x0c	R	MaxError	unsigned int	1	0	100	—	%
0x0d	R	RelativeStateOfCharge	unsigned int	1	0	100	—	%
0x0e	R	AbsoluteStateOfCharge	unsigned int	1	0	100	—	%
0x0f	R/W	RemainingCapacity	unsigned int	2	0	65535	—	mAh or 10mWh
0x10	R	FullChargeCapacity	unsigned int	2	0	65535	—	mAh or 10mWh
0x11	R	RunTimeToEmpty	unsigned int	2	0	65535	—	min
0x12	R	AverageTimeToEmpty	unsigned int	2	0	65535	—	min
0x13	R	AverageTimeToFull	unsigned int	2	0	65535	—	min
0x14	R	ChargingCurrent	unsigned int	2	0	65535	—	mA
0x15	R	ChargingVoltage	unsigned int	2	0	65535	—	mV
0x16	R	BatteryStatus	unsigned int	2	0x0000	0xffff	—	
0x17	R/W	CycleCount	unsigned int	2	0	65535	—	
0x18	R/W	DesignCapacity	unsigned int	2	0	65535	—	mAh or 10mWh
0x19	R/W	DesignVoltage	unsigned int	2	7000	16000	14400	mV
0x1a	R/W	SpecificationInfo	unsigned int	2	0x0000	0xffff	0x0031	
0x1b	R/W	ManufactureDate	unsigned int	2	0	65535	0	
0x1c	R/W	SerialNumber	hex	2	0x0000	0xffff	-	
0x20	R/W	ManufacturerName	String	11+1	—	—	Texas Instruments	ASCII
0x21	R/W	DeviceName	String	7+1	—	—	bq20z75-V180	ASCII
0x22	R/W	DeviceChemistry	String	4+1	—	—	LION	ASCII
0x23	R	ManufacturerData	String	14+1	—	—	—	ASCII
0x2f	R/W	Authenticate	String	20+1	—	—	—	ASCII
0x3c	R	CellVoltage4	unsigned int	2	0	65535	—	mV
0x3d	R	CellVoltage3	unsigned int	2	0	65535	—	mV
0x3e	R	CellVoltage2	unsigned int	2	0	65535	—	mV
0x3f	R	CellVoltage1	unsigned int	2	0	65535	—	mV

Application Schematics





PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ20Z75DBT-V180	ACTIVE	TSSOP	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	20Z75	Samples
BQ20Z75DBTR-V180	ACTIVE	TSSOP	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	20Z75	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

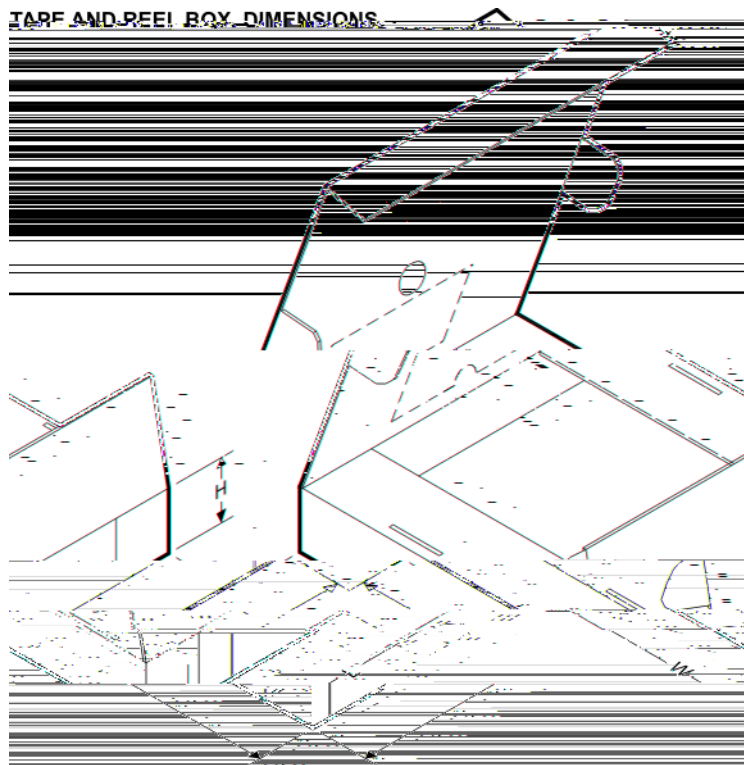
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TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)



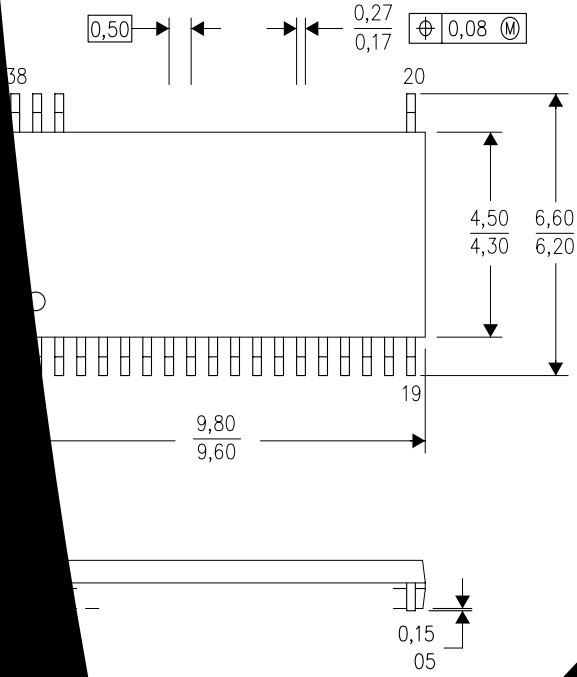
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ20Z75DBTR-V180	TSSOP	DBT	38	2000	367.0	367.0	38.0

MECHANICAL DATA

(R-PDSO-G38)

PLASTIC SMALL OUTLINE



5 NOM

0,75
0,50

See

4073252-6/1 03/11

Dimensions
is sub
of
ED.

Y14.5M-1994.



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