# Dual, 300 mA Output, Low Noise, High PSRR Voltage Regulators

Data Sheet

# ADP222/ADP223/ADP224/ADP225

## FEATURES

- Input voltage range: 2.5 V to 5.5 V
- Small, 8-lead, 2 mm × 2 mm LFCSP package
- Initial accuracy: ±1%
- High PSRR: 70 dB at 10 kHz, 60 dB at 100 kHz, 40 dB at 1 MHz
- Low noise: 27 µV rms at $V_{OUT}$ = 1.2 V, 50 µV rms at $V_{OUT}$ = 2.8 V
- Excellent transient response
- Low dropout voltage: 170 mV at 300 mA load
- 65 µA typical ground current at no load, both LDOs enabled
- Fixed output voltage from 0.8 V to 3.3 V (ADP222/ADP224)
- Adjustable output voltage range from 0.5 V to 5.0 V (ADP223/ADP225)
- Quick output discharge (QOD)—ADP224/ADP225
- Overcurrent and thermal protection

## APPLICATIONS

- Portable and battery-powered equipment
- Portable medical devices
- Post dc-to-dc regulation
- Point of sale terminals
- Credit card readers
- Automatic meter readers
- Wireless network equipment

## TYPICAL APPLICATION CIRCUITS

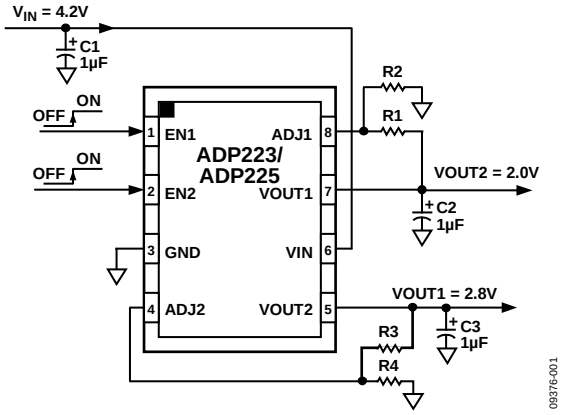


Figure 1. ADP223/ADP225

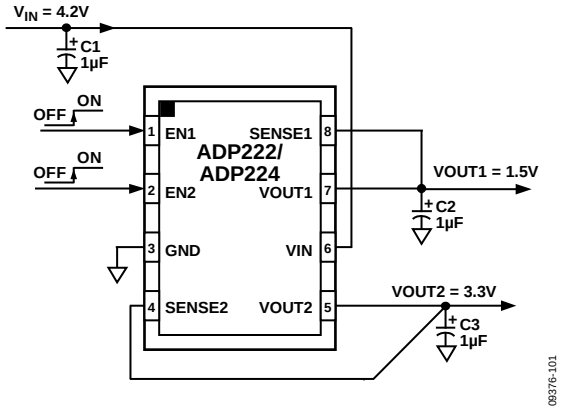


Figure 2. ADP222/ADP224

## GENERAL DESCRIPTION

The 300 mA, adjustable dual output ADP223/ADP225 and fixed dual output ADP222/ADP224 combine high PSRR, low noise, low quiescent current, and low dropout voltage in a voltage regulator that is ideally suited for wireless applications with demanding performance and board space requirements.

The ADP222/ADP224 are available with fixed outputs voltages from 0.8V to 3.3V. The adjustable output ADP223/ADP225 may be set to output voltages from 0.5 V to 5.0 V. The low quiescent current, low dropout voltage, and wide input voltage range of the ADP222/ADP223/ADP224/ADP225 extend the battery life of portable devices.

The ADP222/ADP223/ADP224/ADP225 maintain power supply rejection greater than 60 dB for frequencies as high as 100 kHz while operating with a low headroom voltage. The ADP222/ADP223/ADP224/ADP225 offer much lower noise performance than competing LDOs without the need for a noise bypass capacitor. Overcurrent and thermal protection circuitry prevent damage in adverse conditions.

The ADP224 and ADP225 are identical to the ADP222 and ADP223, respectively, but with the addition of a quick output discharge (QOD) feature.

The ADP222/ADP223/ADP224/ADP225 are available in a small 8-lead, 2 mm × 2 mm LFCSP package and are stable with tiny 1 µF, ±30% ceramic output capacitors, resulting in the smallest possible board area for a wide variety of portable power needs.

Rev. D
Document Feedback


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**2/11—Revision 0: Initial Version**

# SPECIFICATIONS

$V_{IN}$ = ($V_{OUT}$ + 0.5 V) or 2.5 V (whichever is greater), EN1 = EN2 = $V_{IN}$, $I_{OUT1}$ = $I_{OUT2}$ = 10 mA, $C_{IN}$ = $C_{OUT1}$ = $C_{OUT2}$ = 1 µF, $T_A$ = 25°C, unless otherwise noted.

**Table 1.**

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| INPUT VOLTAGE RANGE | $V_{IN}$ | $T_J$ = −40°C to +125°C | 2.5 | | 5.5 | V |
| OPERATING SUPPLY CURRENT WITH BOTH REGULATORS ON | $I_{GND}$ | $I_{OUT}$ = 0 µA | | 65 | | µA |
| | | $I_{OUT}$ = 0 µA, $T_J$ = −40°C to +125°C | | | 150 | µA |
| | | $I_{OUT}$ = 10 mA | | 100 | | µA |
| | | $I_{OUT}$ = 10 mA, $T_J$ = −40°C to +125°C | | | 200 | µA |
| | | $I_{OUT}$ = 300 mA | | 300 | | µA |
| | | $I_{OUT}$ = 300 mA, $T_J$ = −40°C to +125°C | | | 450 | µA |
| SHUTDOWN CURRENT | $I_{GND-SD}$ | EN1 = EN2 = GND | | 0.2 | 2 | µA |
| OUTPUT VOLTAGE ACCURACY[1] | $V_{OUT}$ | $T_J$ = −40°C to +125°C | | | | |
| | | $I_{OUT}$ = 10 mA | −1 | | +1 | % |
| | | 0 µA < $I_{OUT}$ < 300 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V | −2 | | +2 | % |
| ADJUSTABLE-OUTPUT VOLTAGE ACCURACY[1] | $V_{ADJ}$ | $T_J$ = −40°C to +125°C | | | | |
| | | $I_{OUT}$ = 10 mA | 0.495 | 0.500 | 0.505 | V |
| | | 0 µA < $I_{OUT}$ < 300 mA, $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V | 0.490 | | 0.510 | V |
| LINE REGULATION | $\Delta V_{OUT}/\Delta V_{IN}$ | $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V | | 0.01 | | %/V |
| | | $V_{IN}$ = ($V_{OUT}$ + 0.5 V) to 5.5 V, $T_J$ = −40°C to +125°C | −0.05 | | +0.05 | %/V |
| LOAD REGULATION[2] | $\Delta V_{OUT}/\Delta I_{OUT}$ | $I_{OUT}$ = 1 mA to 300 mA | | 0.001 | | %/mA |
| | | $I_{OUT}$ = 1 mA to 300 mA, $T_J$ = −40°C to +125°C | | | 0.002 | %/mA |
| DROPOUT VOLTAGE[3] | $V_{DROPOUT}$ | $V_{OUT}$ = 3.3 V | | | | |
| | | $I_{OUT}$ = 10 mA | | 6 | | mV |
| | | $I_{OUT}$ = 10 mA, $T_J$ = −40°C to +125°C | | | 9 | mV |
| | | $I_{OUT}$ = 300 mA | | 170 | | mV |
| | | $I_{OUT}$ = 300 mA, $T_J$ = −40°C to +125°C A | | | 260 | mV |
| SENSE INPUT BIAS CURRENT | $SENSE_{I-BIAS}$ | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V, SENSEx connected to VOUTx | | 10 | | nA |
| ADJx INPUT BIAS CURRENT | $ADJ_{I-BIAS}$ | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V, ADJx connected to VOUTx | | 10 | | nA |
| START-UP TIME[4] | $t_{START-UP}$ | $V_{OUT}$ = 3.3 V | | 240 | | µs |
| | | $V_{OUT}$ = 0.8 V | | 100 | | µs |
| CURRENT-LIMIT THRESHOLD[5] | $I_{LIMIT}$ | | 340 | 400 | | mA |
| THERMAL SHUTDOWN | | | | | | |
| Thermal Shutdown Threshold | $TS_{SD}$ | $T_J$ rising | | 155 | | °C |
| Thermal Shutdown Hysteresis | $TS_{SD-HYS}$ | | | 15 | | °C |
| EN INPUT | | | | | | |
| EN Input Logic High | $V_{IH}$ | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | 1.2 | | | V |
| EN Input Logic Low | $V_{IL}$ | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | | | 0.4 | V |
| EN Input Leakage Current | $V_{I-LEAKAGE}$ | EN1 = EN2 = $V_{IN}$ or GND | | 0.1 | | µA |
| | | EN1 = EN2 = $V_{IN}$ or GND, $T_J$ = −40°C to +125°C | | | 1 | µA |
| UNDERVOLTAGE LOCKOUT | UVLO | | | | | |
| Input Voltage Rising | $UVLO_{RISE}$ | | | | 2.45 | V |
| Input Voltage Falling | $UVLO_{FALL}$ | | 2.2 | | | V |
| Hysteresis | $UVLO_{HYS}$ | | | 120 | | mV |
| OUTPUT DISCHARGE TIME | $t_{DIS}$ | $V_{OUT}$ = 2.8 V | | 1000 | | µs |
| OUTPUT DISCHARGE RESISTANCE | $R_{QOD}$ | | | 140 | | Ω |

| Parameter | Symbol | Test Conditions/Comments | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| OUTPUT NOISE | $OUT_{NOISE}$ | 10 Hz to 100 kHz, $V_{IN}$ = 5 V, $V_{OUT}$ = 3.3 V | | 56 | | μV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 5 V, $V_{OUT}$ = 2.8 V | | 50 | | μV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 2.5 V | | 45 | | μV rms |
| | | 10 Hz to 100 kHz, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 1.2 V | | 27 | | μV rms |
| POWER SUPPLY REJECTION RATIO | PSRR | $V_{IN}$ = 2.5 V, $V_{OUT}$ = 0.8 V, $I_{OUT}$ = 100 mA | | | | |
| | | 100 Hz | | 76 | | dB |
| | | 1 kHz | | 76 | | dB |
| | | 10 kHz | | 70 | | dB |
| | | 100 kHz | | 60 | | dB |
| | | 1 MHz | | 40 | | dB |
| | | $V_{IN}$ = 3.8 V, $V_{OUT}$ = 2.8 V, $I_{OUT}$ = 100 mA | | | | |
| | | 100 Hz | | 68 | | dB |
| | | 1 kHz | | 68 | | dB |
| | | 10 kHz | | 68 | | dB |
| | | 100 kHz | | 60 | | dB |
| | | 1 MHz | | 40 | | dB |

[1] Accuracy when VOUTx is connected directly to ADJx or SENSEx. When the VOUTx voltage is set by external feedback resistors, the absolute accuracy in adjust mode depends on the tolerances of resistors used.
[2] Based on an end-point calculation using 1 mA and 300 mA loads.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.
[4] Start-up time is defined as the time between the rising edge of EN to $V_{OUT}$ being at 90% of its nominal value.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V or 2.7 V.

## INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

The minimum input and output capacitance should be greater than 0.70 μF over the full range of the operating conditions. The full range of the operating conditions in the application must be considered during device selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended for use with the LDOs, but Y5V and Z5U capacitors are not recommended for use with the LDOs.

**Table 2.**

| Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MINIMUM INPUT AND OUTPUT CAPACITANCE | $C_{MIN}$ | $T_A$ = −40°C to +125°C | 0.70 | | | μF |
| CAPACITOR ESR | $R_{ESR}$ | $T_A$ = −40°C to +125°C | 0.001 | | 1 | Ω |

# ABSOLUTE MAXIMUM RATINGS

**Table 3.**

| Parameter | Rating |
|---|---|
| VIN to GND | −0.3 V to +6 V |
| ADJ1, ADJ2, VOUT1, VOUT2 to GND | −0.3 V to VIN |
| EN1, EN2 to GND | −0.3 V to +6 V |
| Storage Temperature Range | −65°C to +150°C |
| Operating Junction Temperature Range | −40°C to +125°C |
| Soldering Conditions | JEDEC J-STD-020 |

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## THERMAL DATA

Absolute maximum ratings apply individually only, not in combination.

The ADP222/ADP223/ADP224/ADP225 can be damaged when the junction temperature limits are exceeded. Monitoring ambient temperature does not guarantee that $T_J$ is within the specified temperature limits. In applications with high power dissipation and poor thermal resistance, the maximum ambient temperature may have to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits. The junction temperature ($T_J$) of the device is dependent on the ambient temperature ($T_A$), the power dissipation of the device ($P_D$), and the junction-to-ambient thermal resistance of the package ($\theta_{JA}$). Maximum junction temperature ($T_J$) is calculated from the ambient temperature ($T_A$) and power dissipation ($P_D$) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

Junction-to-ambient thermal resistance ($\theta_{JA}$) of the package is based on modeling and calculation using a 4-layer board. $\theta_{JA}$ is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required. The value of $\theta_{JA}$ may vary, depending on PCB material, layout, and environmental conditions. The specified value of $\theta_{JA}$ is based on a 4-layer, 4 in × 3 in, 2½ oz copper board, as per JEDEC standards. For more information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

$\Psi_{JB}$ is the junction-to-board thermal characterization parameter with units of °C/W. $\Psi_{JB}$ of the package is based on modeling and calculation using a 4-layer board. The JESD51-12, *Guidelines for Reporting and Using Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. $\Psi_{JB}$ measures the component power flowing through multiple thermal paths rather than a single path as in thermal resistance, $\theta_{JB}$. Therefore, $\Psi_{JB}$ thermal paths include convection from the top of the package as well as radiation from the package, factors that make $\Psi_{JB}$ more useful in real-world applications. Maximum junction temperature ($T_J$) is calculated from the board temperature ($T_B$) and power dissipation ($P_D$) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to JESD51-8 and JESD51-12 for more detailed information about $\Psi_{JB}$.

## THERMAL RESISTANCE

$\theta_{JA}$ and $\Psi_{JB}$ are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

**Table 4. Thermal Resistance**

| Package Type | $\theta_{JA}$ | $\theta_{JC}$ | $\Psi_{JB}$ | Unit |
|---|---|---|---|---|
| 8-Lead 2 mm × 2 mm LFCSP | 50.2 | 31.7 | 18.2 | °C/W |

## ESD CAUTION

**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

# PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

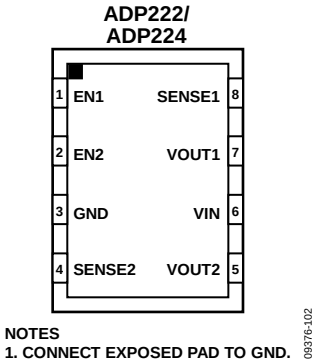


*Figure 3. ADP222/ADP224 Pin Configuration*

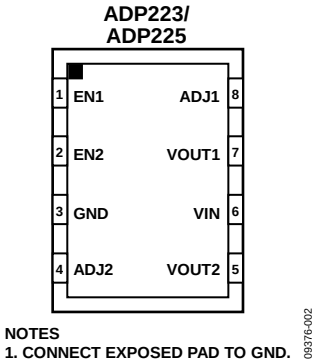


*Figure 4. ADP223/ADP225 Pin Configuration*

**Table 5. Pin Function Descriptions**

| Pin No. | | | |
|---|---|---|---|
| ADP222/ADP224 | ADP223/ADP225 | Mnemonic | Description |
| 1 | 1 | EN1 | Enable Input for the First Regulator. Drive EN1 high to turn on Regulator 1 and drive EN1 low to turn off Regulator 1. For automatic startup, connect EN1 to VIN. |
| 2 | 2 | EN2 | Enable Input for the Second Regulator. Drive EN2 high to turn on Regulator 2 and drive EN2 low to turn off Regulator 2. For automatic startup, connect EN2 to VIN. |
| 3 | 3 | GND | Ground Pin. |
| N/A[1] | 4 | ADJ2 | Adjust Pin for VOUT2. A resistor divider from VOUT2 to ADJ2 sets the output voltage. |
| 4 | N/A[1] | SENSE2 | Sense Pin for VOUT2. |
| 5 | 5 | VOUT2 | Regulated Output Voltage. Connect an 1 µF or greater output capacitor between VOUT2 and GND. |
| 6 | 6 | VIN | Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor. |
| 7 | 7 | VOUT1 | Regulated Output Voltage. Connect 1 µF or greater output capacitor between VOUT1 and GND. |
| N/A[1] | 8 | ADJ1 | Adjust Pin for VOUT1. A resistor divider from VOUT1 to ADJ1 sets the output voltage. |
| 8 | N/A[1] | SENSE1 | Sense Pin for VOUT1. |
| | | EPAD | The exposed paddle must be connected to ground. |

[1] N/A means not applicable.

# TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 5 V, $V_{OUT1}$ = 3.3 V, $V_{OUT2}$ = 2.8 V, $I_{OUT1}$ = $I_{OUT2}$ = 1 mA, $C_{IN}$ = $C_{OUT}$ = 1 µF, $T_A$ = 25°C, unless otherwise noted.

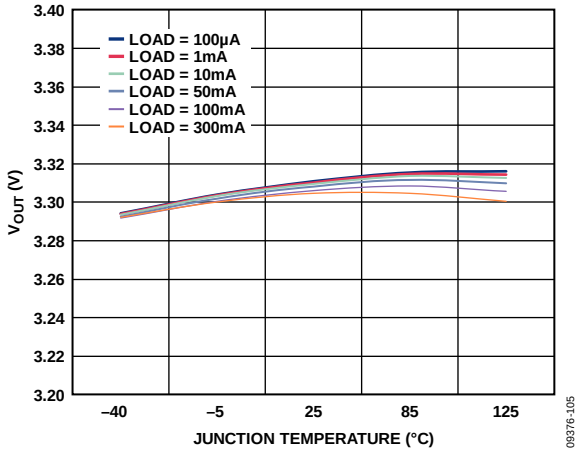


*Figure 5. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 3.3 V, ADP222/ADP224*

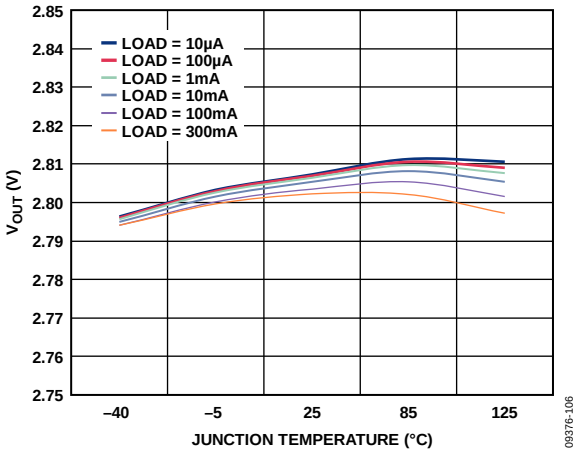


*Figure 6. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 2.8 V, ADP222/ADP224*

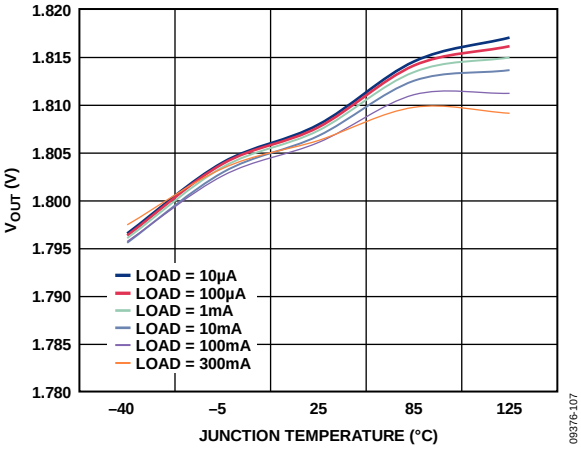


*Figure 7. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 1.8 V, ADP222/ADP224*

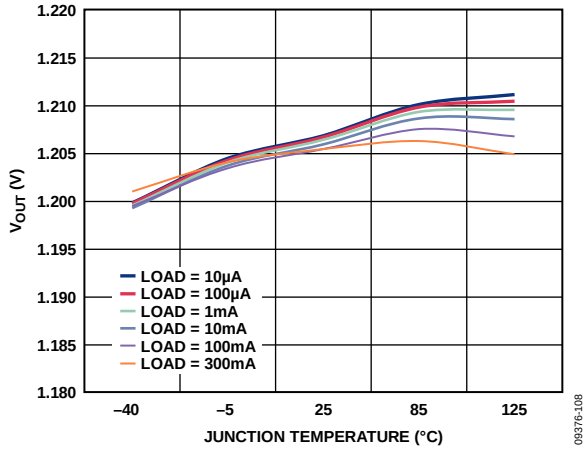


*Figure 8. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 1.2 V, ADP222/ADP224*

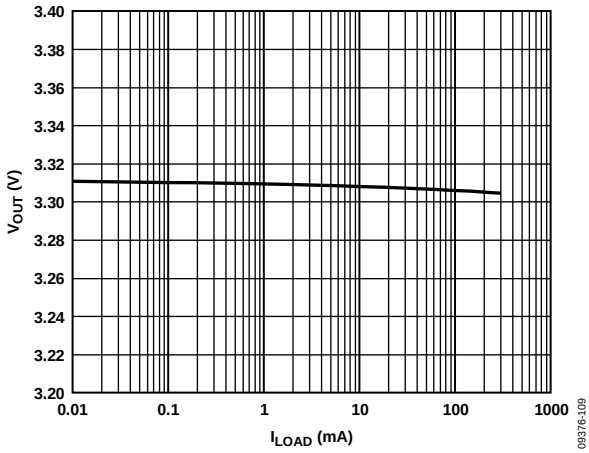


*Figure 9. Output Voltage vs. Load Current, $V_{OUTx}$ = 3.3 V, ADP222/ADP224*

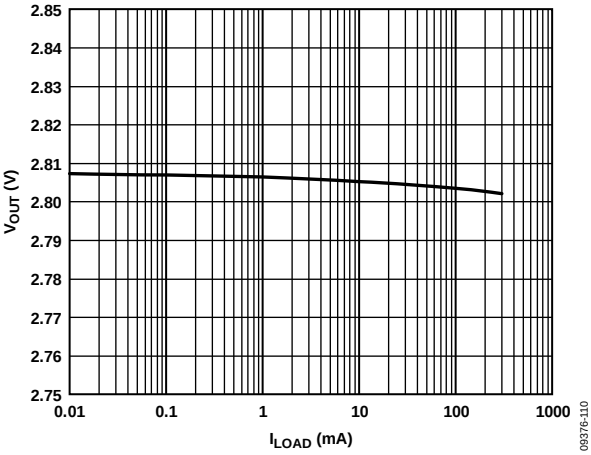


*Figure 10. Output Voltage vs. Load Current, $V_{OUTx}$ = 2.8 V, ADP222/ADP224*

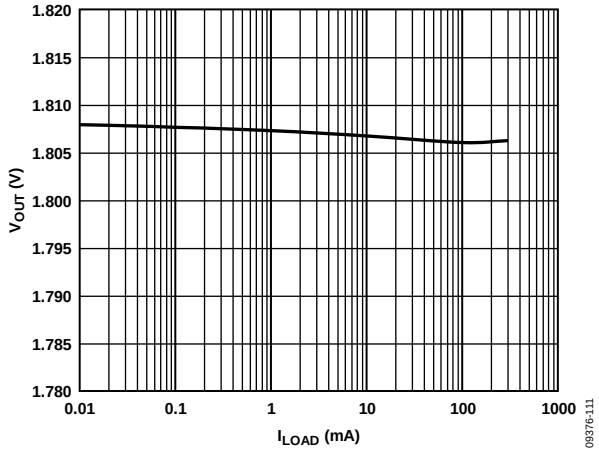


Figure 11. Output Voltage vs. Load Current, $V_{OUTx}$ = 1.8 V, ADP222/ADP224

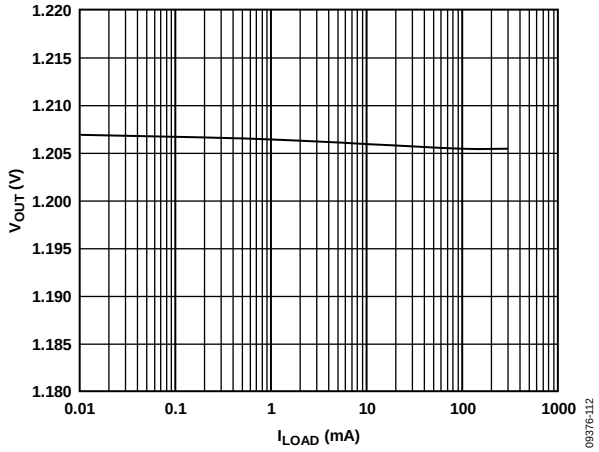


Figure 12. Output Voltage vs. Load Current, $V_{OUTx}$ = 1.2 V, ADP222/ADP224

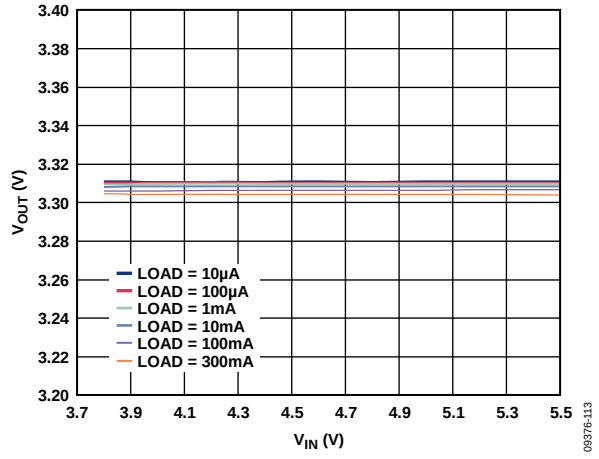


Figure 13. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 3.3 V, ADP222/ADP224

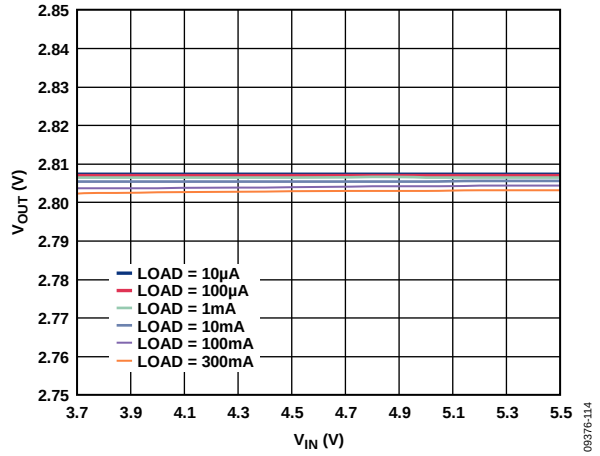


Figure 14. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 2.8 V, ADP222/ADP224

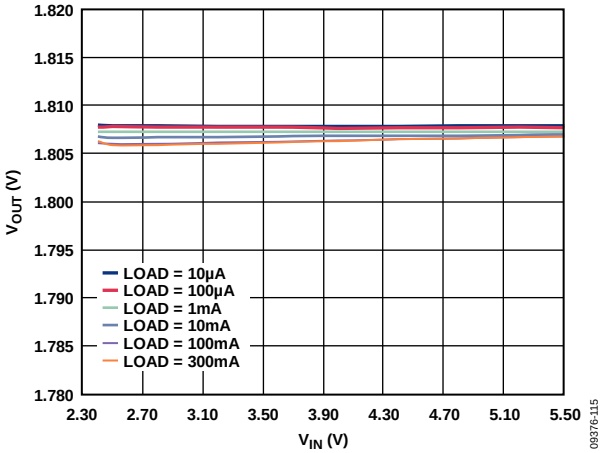


Figure 15. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 1.8 V, ADP222/ADP224

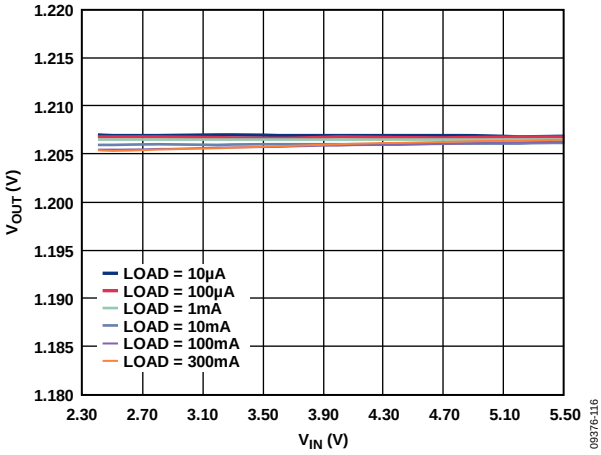


Figure 16. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 1.2 V, ADP222/ADP224

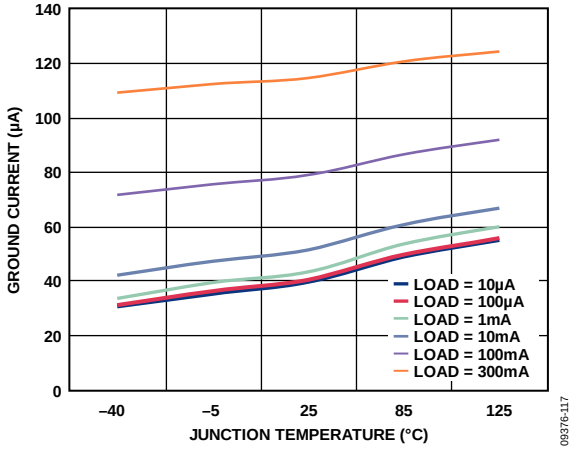


Figure 17. Ground Current vs. Junction Temperature, Single Output, ADP222/ADP224

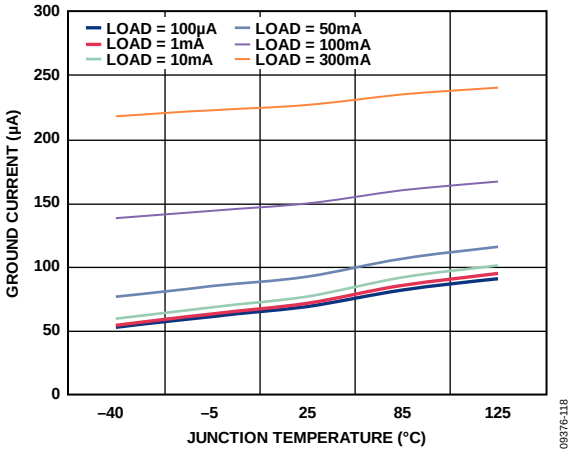


Figure 18. Ground Current vs. Junction Temperature, Dual Output, ADP222/ADP224

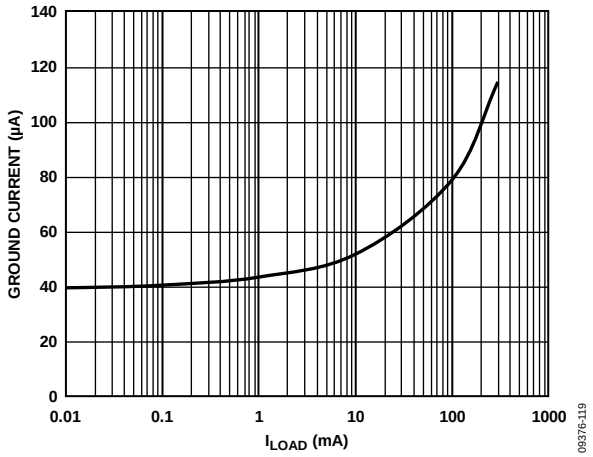


Figure 19. Ground Current vs. Load Current, Single Output, ADP222/ADP224

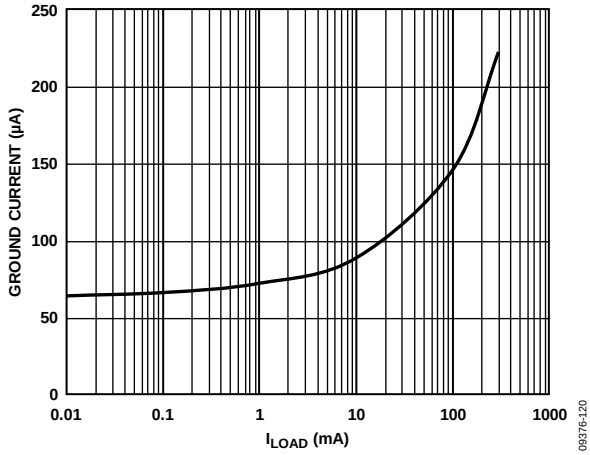


Figure 20. Ground Current vs. Load Current, Dual Output, ADP222/ADP224

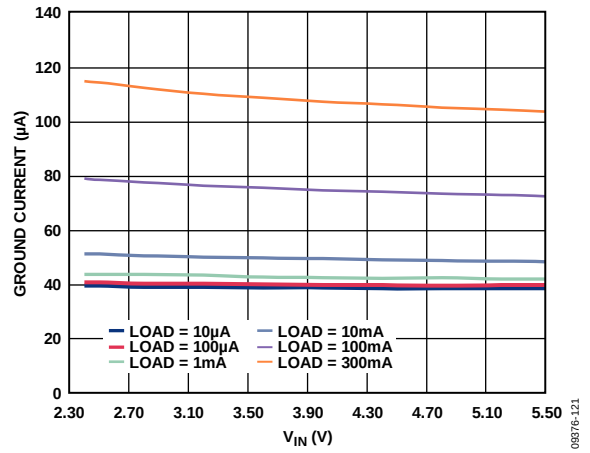


Figure 21. Ground Current vs. Input Voltage, $V_{OUTx}$ = 1.2 V, ADP222/ADP224

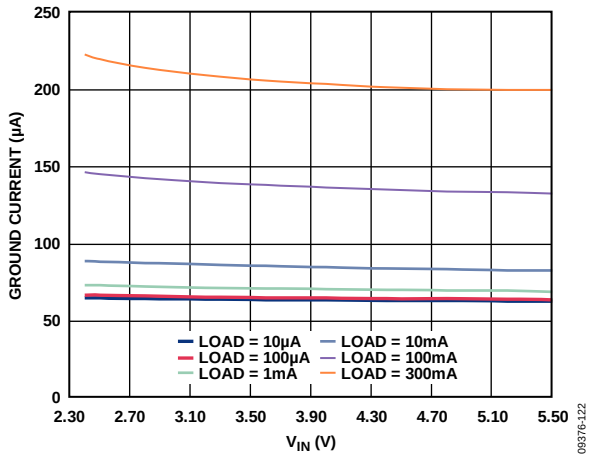


Figure 22. Ground Current vs. Input Voltage, $V_{OUTx}$ = 1.2 V and 1.8 V, ADP222/ADP224

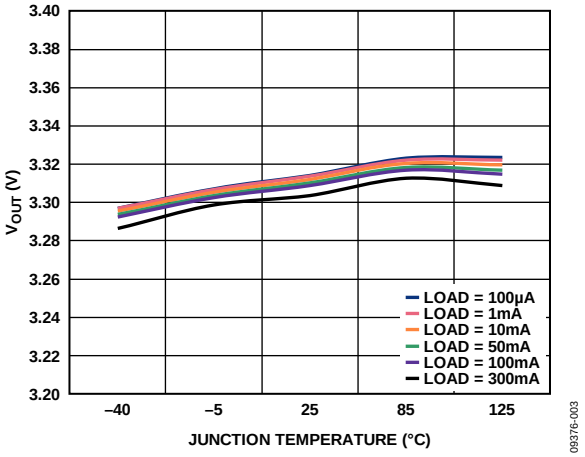


Figure 23. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 3.3 V, ADP223/ADP225

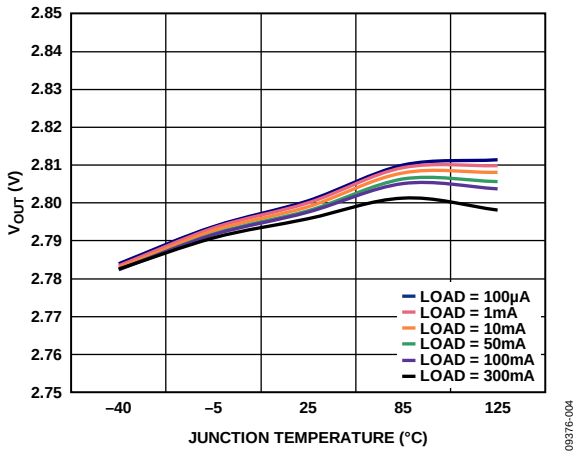


Figure 24. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 2.8 V, ADP223/ADP225

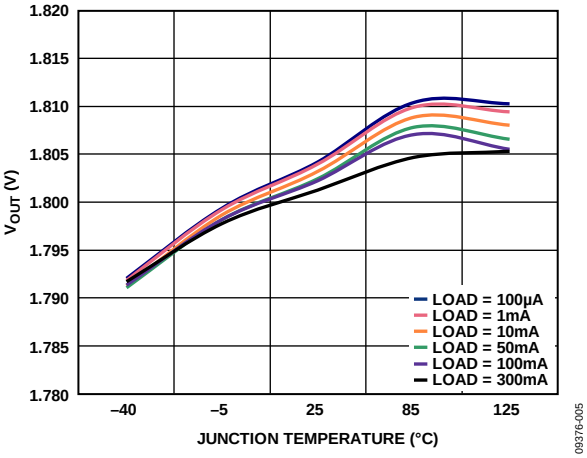


Figure 25. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 1.8 V, ADP223/ADP225

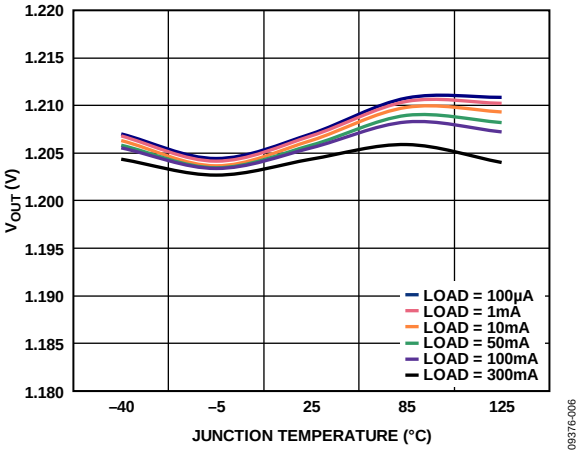


Figure 26. Output Voltage vs. Junction Temperature, $V_{OUTx}$ = 1.2 V, ADP223/ADP225

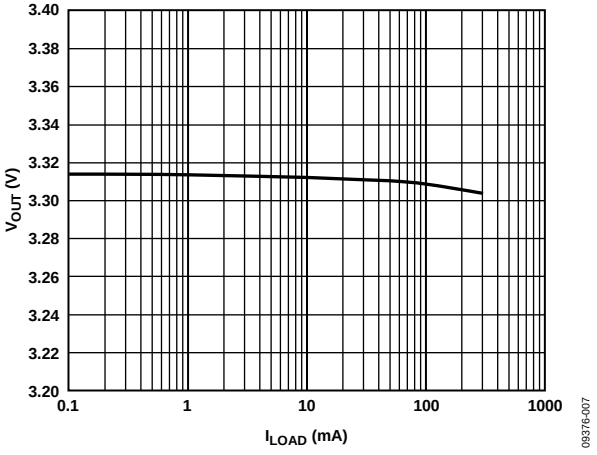


Figure 27. Output Voltage vs. Load Current, $V_{OUTx}$ = 3.3 V, ADP223/ADP225

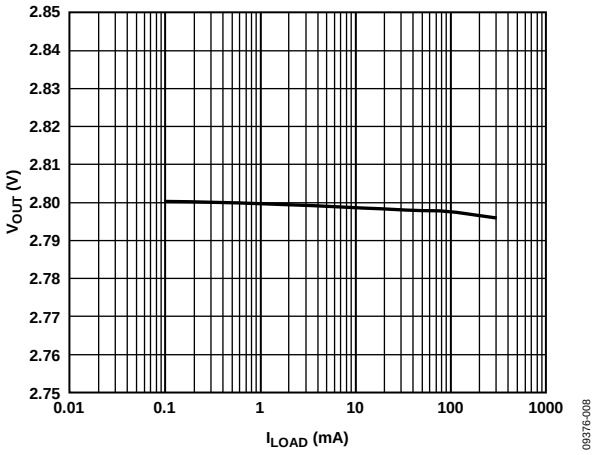


Figure 28. Output Voltage vs. Load Current, $V_{OUTx}$ = 2.8 V, ADP223/ADP225

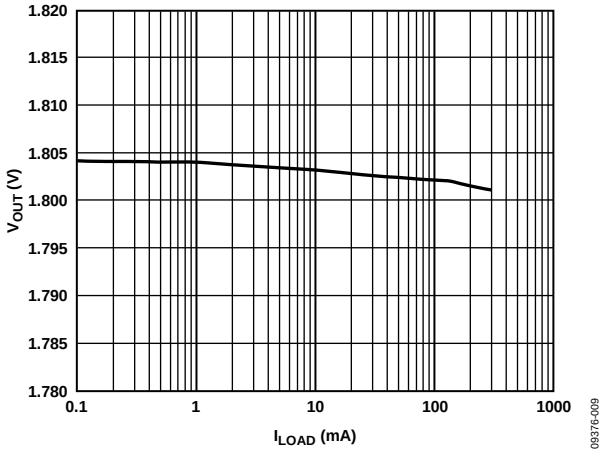


Figure 29. Output Voltage vs. Load Current, $V_{OUTx}$ = 1.8 V, ADP223/ADP225

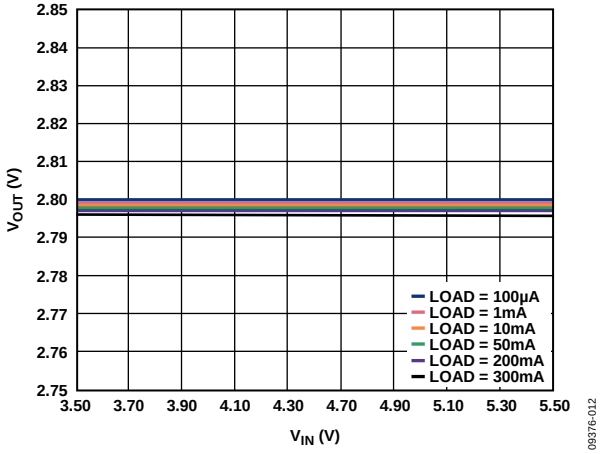


Figure 32. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 2.8 V, ADP223/ADP225

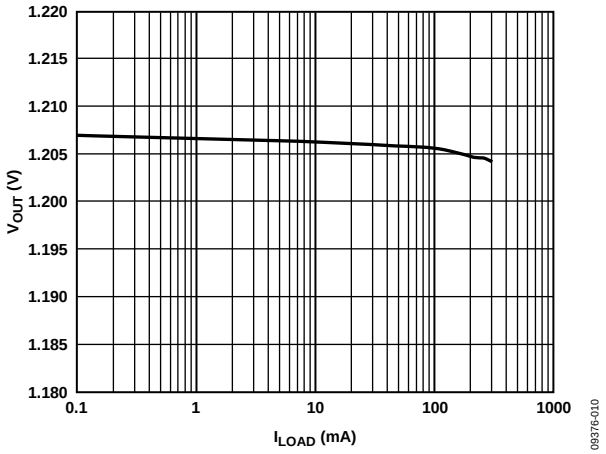


Figure 30. Output Voltage vs. Load Current, $V_{OUTx}$ = 1.2 V, ADP223/ADP225

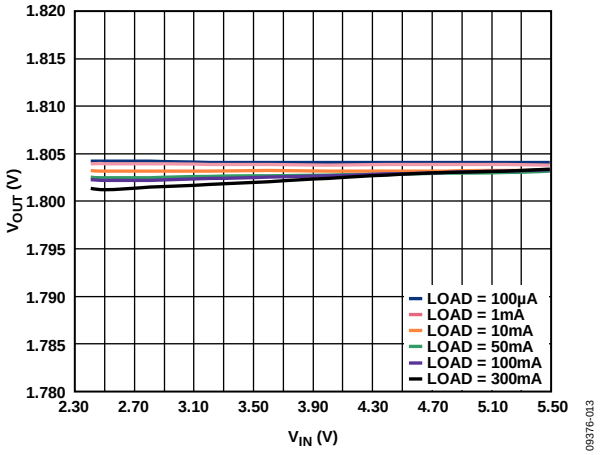


Figure 33. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 1.8 V, ADP223/ADP225

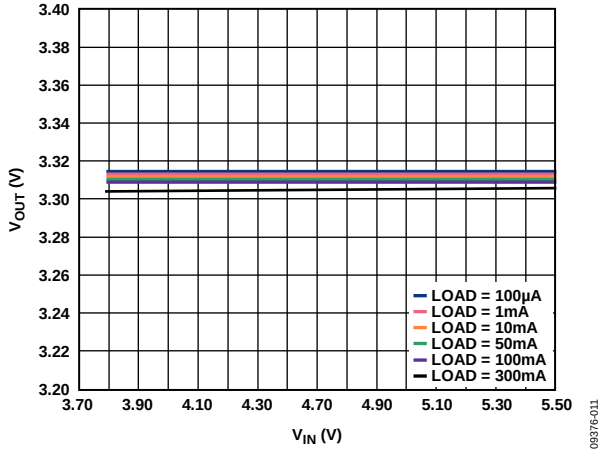


Figure 31. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 3.3 V, ADP223/ADP225

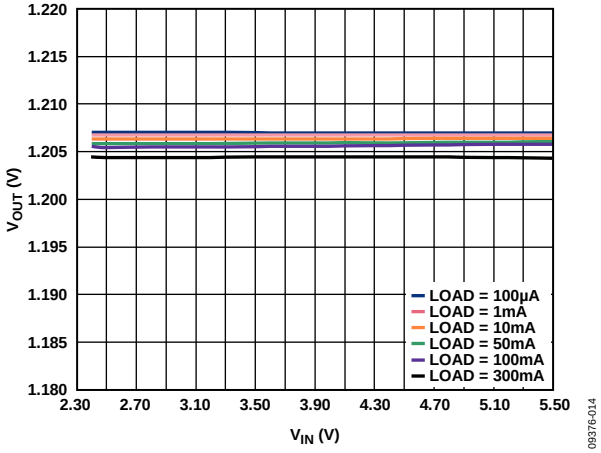


Figure 34. Output Voltage vs. Input Voltage, $V_{OUTx}$ = 1.2 V, ADP223/ADP225

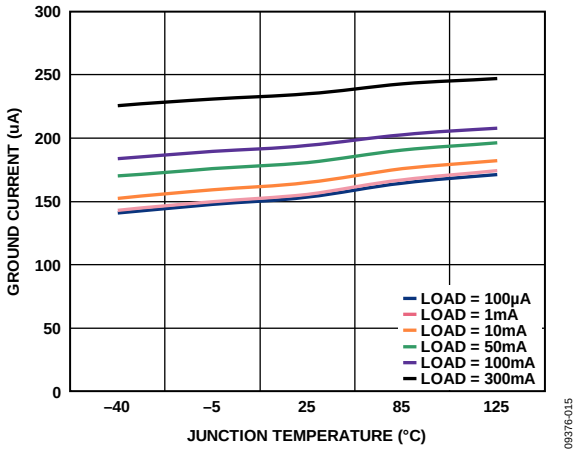


Figure 35. Ground Current vs. Junction Temperature, Single Output, Includes 100 µA for Output Divider, ADP223/ADP225

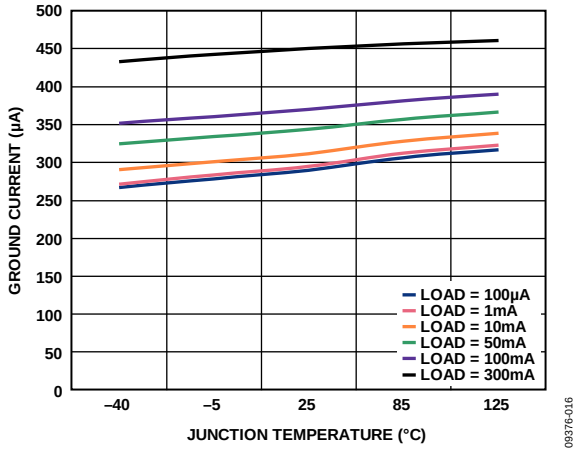


Figure 36. Ground Current vs. Junction Temperature, Dual Output, Includes 200 µA for Output Dividers, ADP223/ADP225

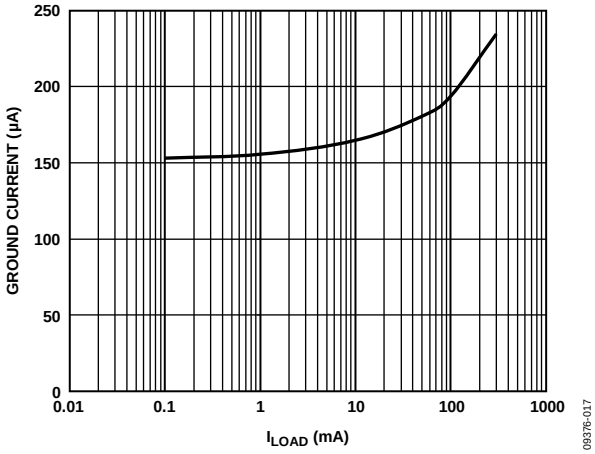


Figure 37. Ground Current vs. Load Current, Single Output, Includes 100 µA for Output Divider, ADP223/ADP225

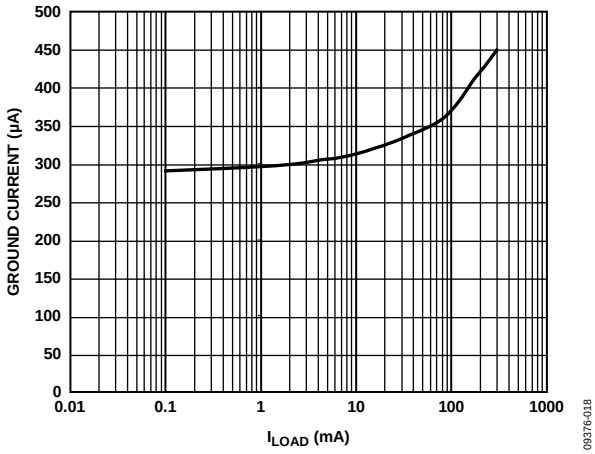


Figure 38. Ground Current vs. Load Current, Dual Output, Includes 200 µA for Output Dividers, ADP223/ADP225

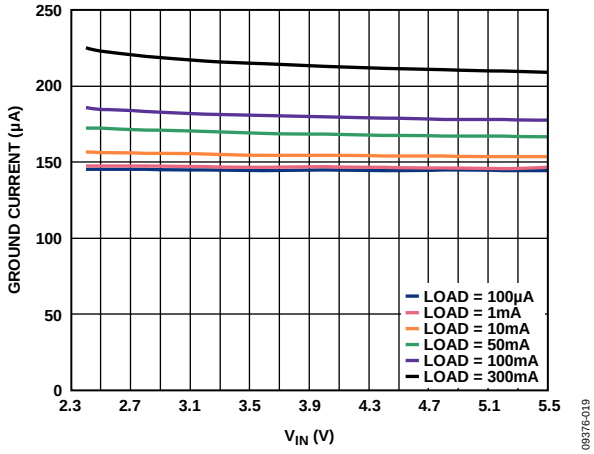


Figure 39. Ground Current vs. Input Voltage, $V_{OUTx}$ = 1.2 V, Single Output, Includes 100 µA for Output Divider, ADP223/ADP225

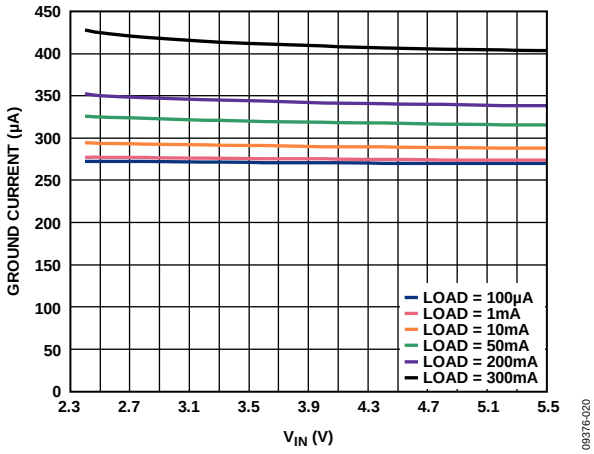


Figure 40. Ground Current vs. Input Voltage, $V_{OUTx}$ = 1.2 V and 1.8 V, Dual Output, Includes 200 µA for Output Dividers, ADP223/ADP225

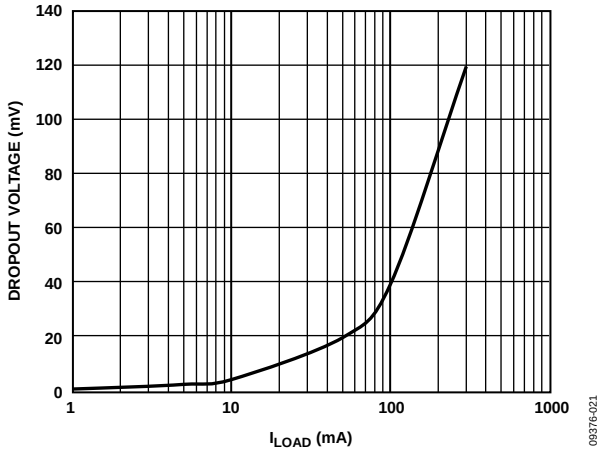


Figure 41. Dropout Voltage vs. Load Current, $V_{OUT}$ = 3.3 V

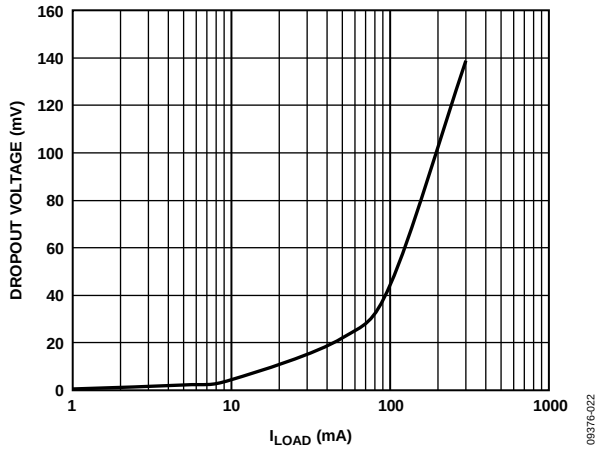


Figure 42. Dropout Voltage vs. Load Current, $V_{OUT}$ = 2.8 V

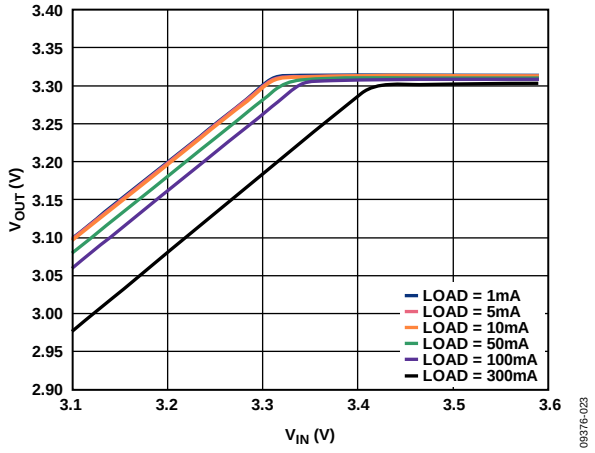


Figure 43. Output Voltage vs. Input Voltage in Dropout, $V_{OUTx}$ = 3.3 V

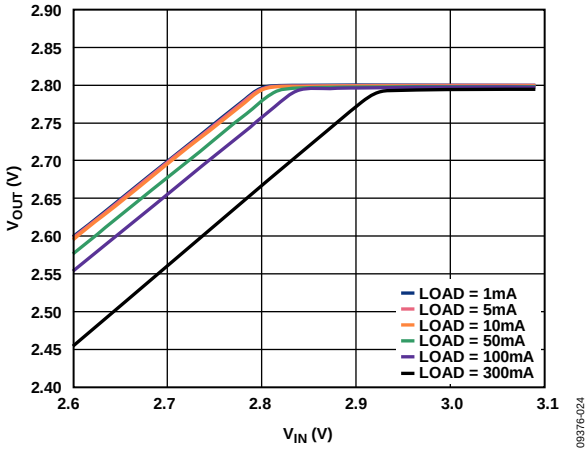


Figure 44. Output Voltage vs. Input Voltage in Dropout, $V_{OUTx}$ = 2.8 V

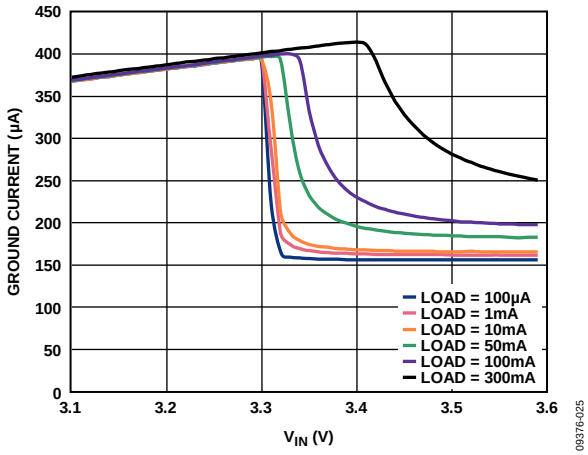


Figure 45. Ground Current vs. Input Voltage in Dropout, $V_{OUTx}$ = 3.3 V

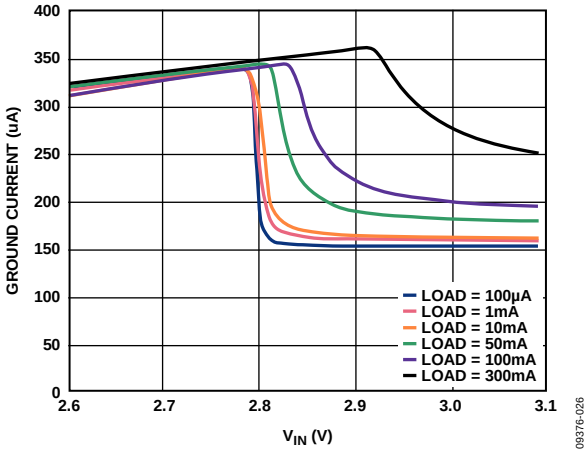


Figure 46. Ground Current vs. Input Voltage in Dropout, $V_{OUTx}$ = 2.8 V

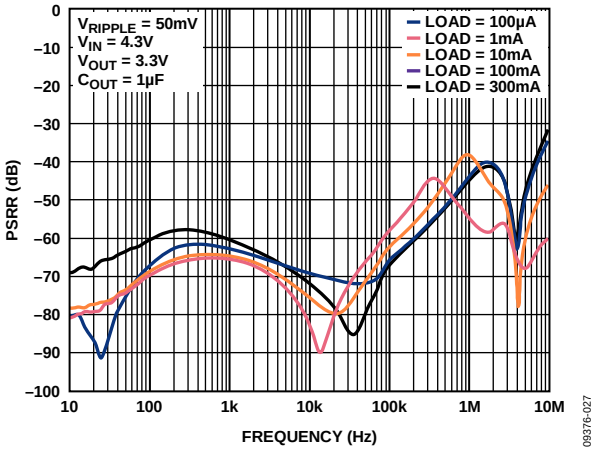


*Figure 47. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 4.3, V $V_{OUTx}$ = 3.3 V*

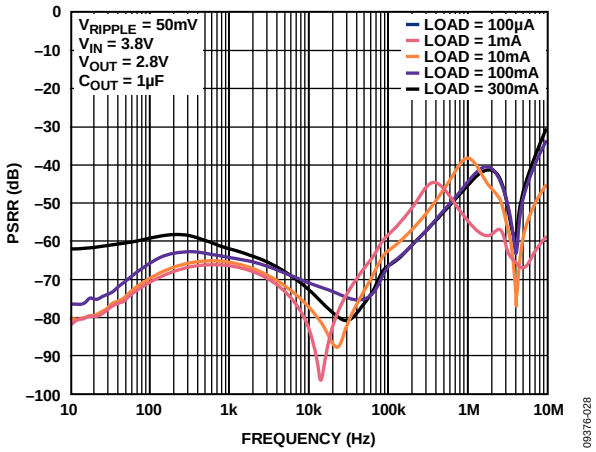


*Figure 48. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 3.8 V, $V_{OUTx}$ = 2.8 V*

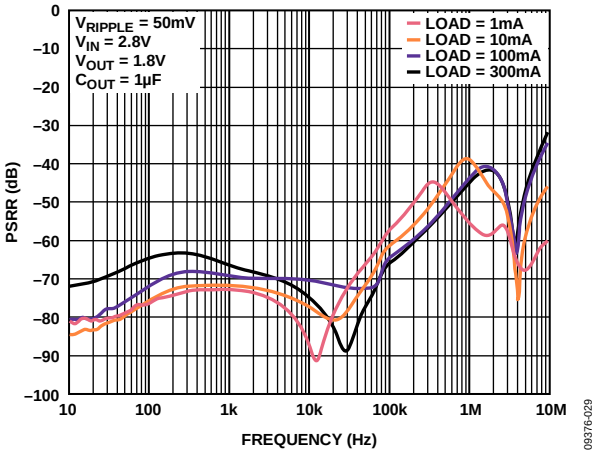


*Figure 49. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 2.8 V, $V_{OUTx}$ = 1.8 V*

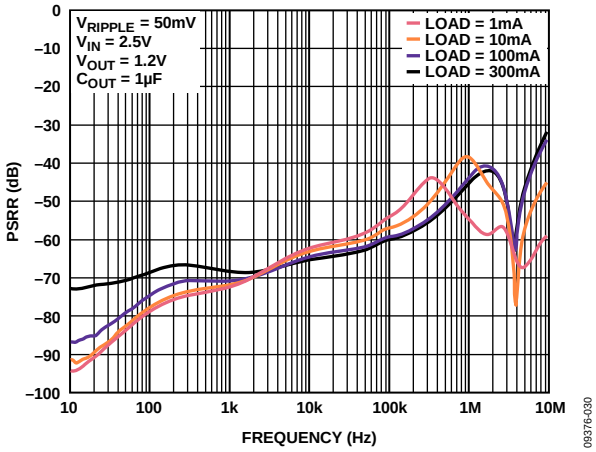


*Figure 50. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 2.5 V, $V_{OUTx}$ = 1.2 V*

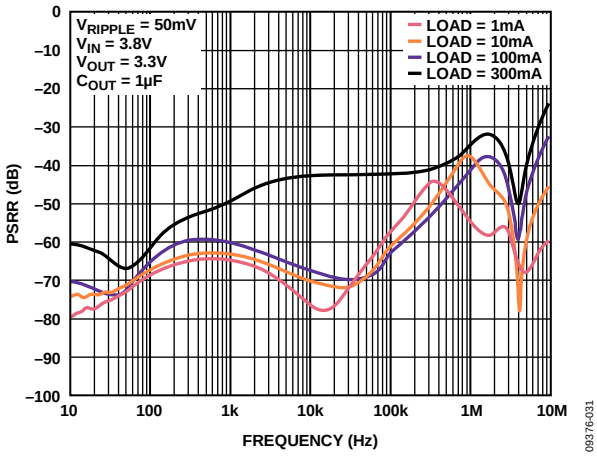


*Figure 51. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 3.8 V, $V_{OUTx}$ = 3.3 V*

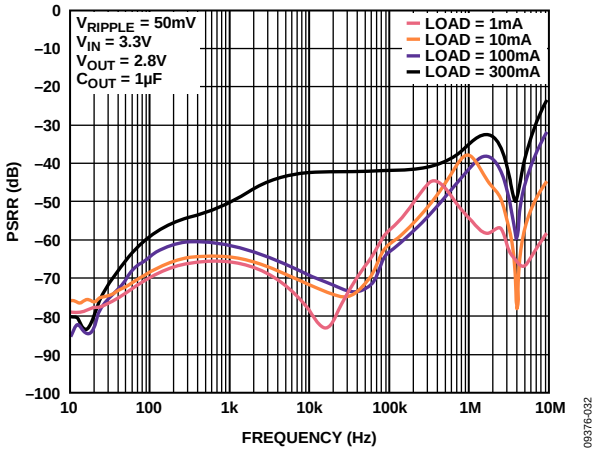


*Figure 52. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 3.3 V, $V_{OUTx}$ = 2.8 V*

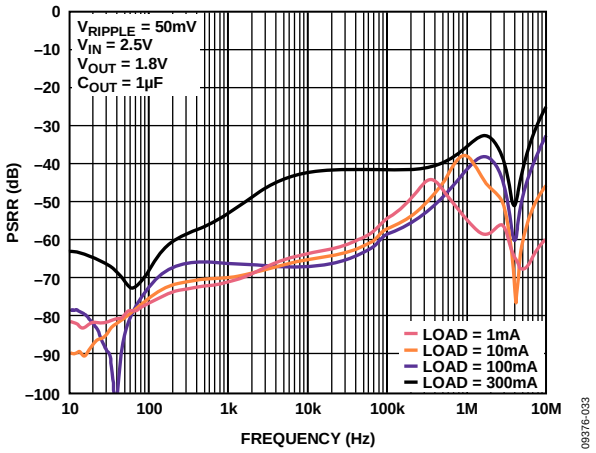


*Figure 53. Power Supply Rejection Ratio vs. Frequency, $V_{IN}$ = 2.5 V, $V_{OUTx}$ = 1.8 V*

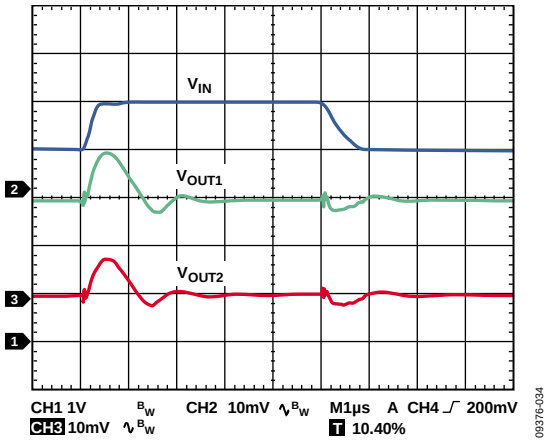


*Figure 54. Transient Line Response, $V_{OUTx}$ = 3.3 V and 2.8 V, $V_{IN}$ = 4 V to 5 V, $I_{LOAD}$ = 10 mA*

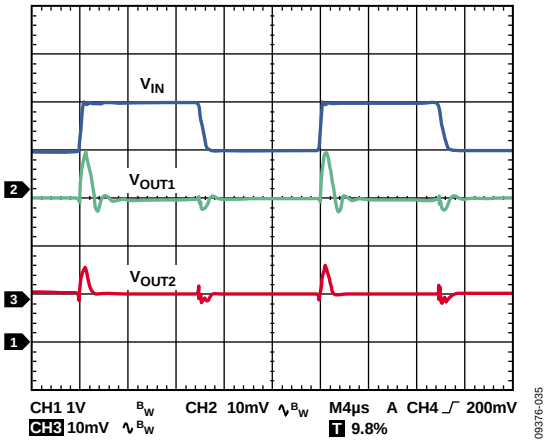


*Figure 55. Transient Line Response, $V_{OUTx}$ = 1.2 V and 1.8 V, $V_{IN}$ = 4 V to 5 V, $I_{LOAD}$ = 10 mA*

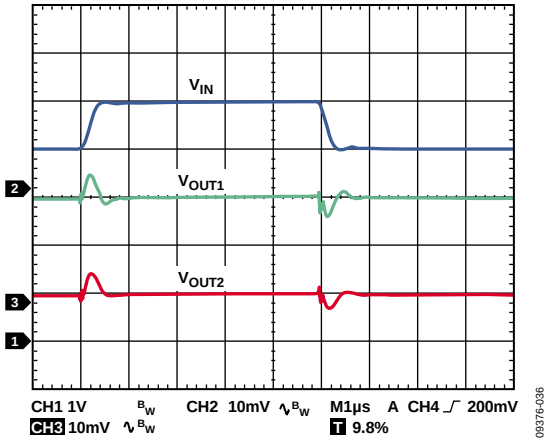


*Figure 56. Transient Line Response, $V_{OUTx}$ = 3.3 V and 2.8 V, $V_{IN}$ = 4 V to 5 V, $I_{LOAD}$ = 300 mA*

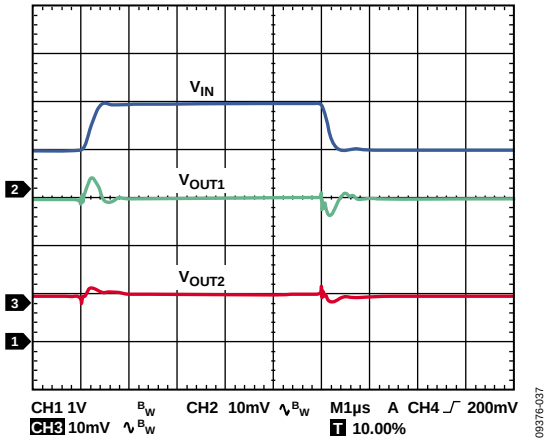


*Figure 57. Transient Line Response, $V_{OUTx}$ = 1.2 V and 1.8 V, $V_{IN}$ = 4 V to 5 V, $I_{LOAD}$ = 300 mA*

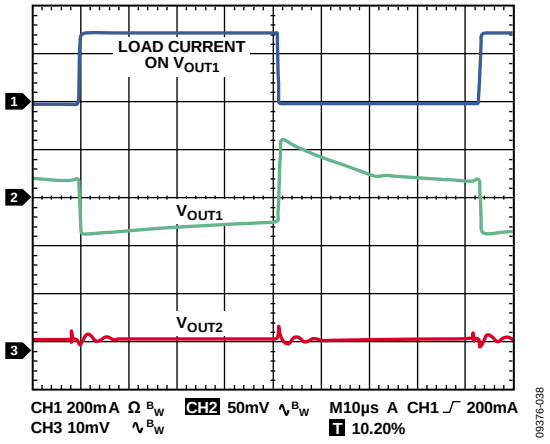


*Figure 58. Transient Load Response, $V_{OUTx}$ = 3.3 V, $I_{LOAD}$ = 1 mA to 300 mA; $V_{OUTx}$ = 2.8 V, $I_{LOAD}$ = 1 mA*

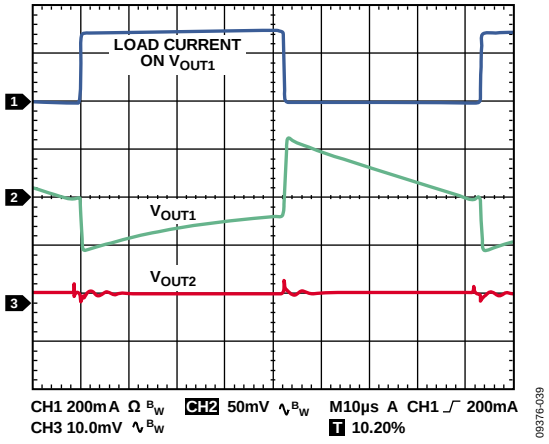


Figure 59. Transient Load Response, $V_{OUTx}$ = 1.2 V, $I_{LOAD}$ = 1 mA to 300 mA; $V_{OUTx}$ = 1.8 V, $I_{LOAD}$ = 1 mA

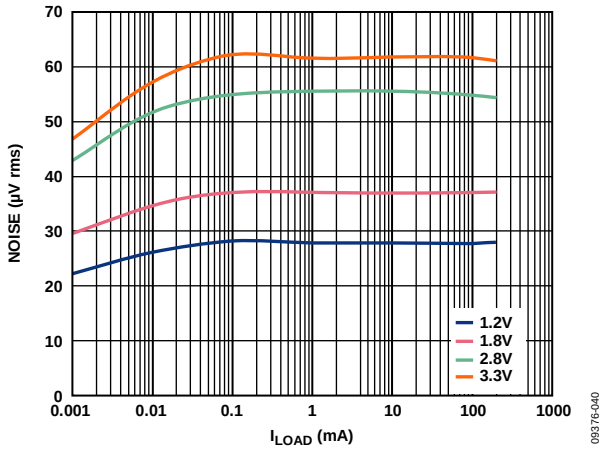


Figure 60. RMS Output Noise vs. Load Current and Output Voltage, $V_{IN}$ = 5 V, $C_{OUT}$ = 1 µF

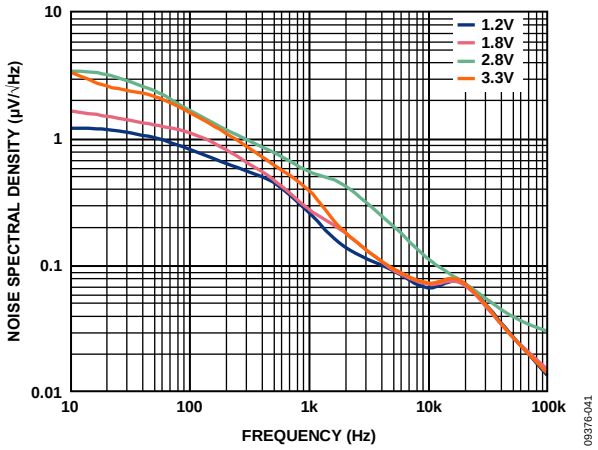


Figure 61. Output Noise Spectral Density, $V_{IN}$ = 5 V, $I_{LOAD}$ = 10 mA, $C_{OUT}$ = 1 µF

# THEORY OF OPERATION

The ADP222/ADP223/ADP224/ADP225 are low quiescent current, fixed and adjustable dual output, low dropout linear regulators that operate from 2.5 V to 5.5 V and provide up to 300 mA of current from each output. Drawing a low 300 µA quiescent current (typical) at full load make the ADP222/ADP223/ADP224/ADP225 ideal for battery-operated portable equipment. Shutdown current consumption is typically 200 nA.

Optimized for use with small 1 µF ceramic capacitors, the ADP222/ADP223/ADP224/ADP225 provide excellent transient performance.

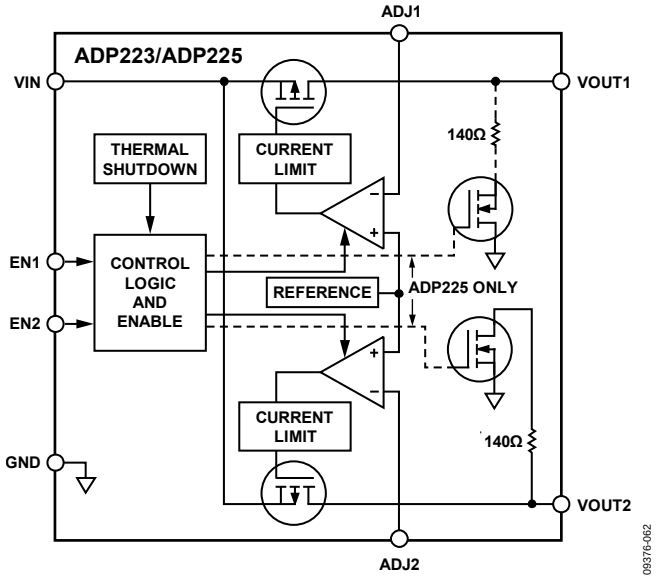


*Figure 62. Internal Block Diagram, ADP223/ADP225*

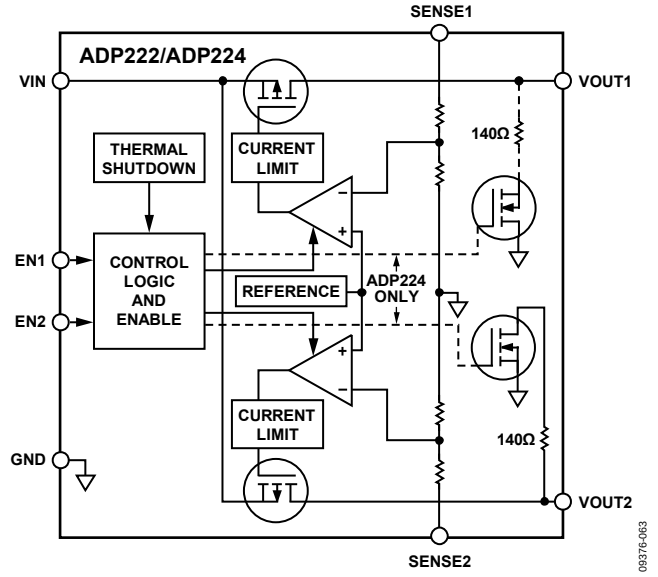


*Figure 63. Internal Block Diagram, ADP222/ADP224*

Internally, the ADP222/ADP223/ADP224/ADP225 consist of a reference, two error amplifiers, and two PMOS pass transistors. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

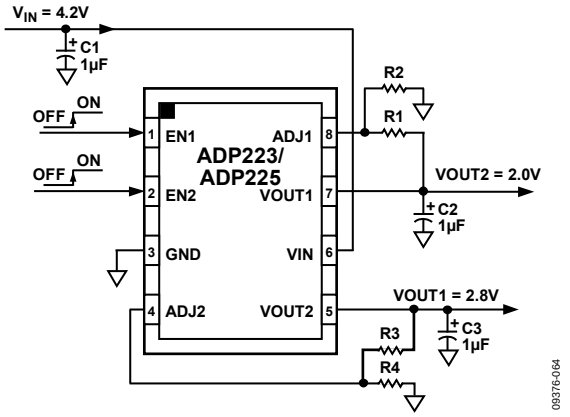


*Figure 64. Typical Application Circuit for Setting Output Voltages, ADP223/ADP225*

The ADP223/ADP225 are exactly the same as the ADP222/ADP224 except that the output voltage dividers are internally disconnected and the feedback input of the error amplifiers is brought out for each output. The output voltages can be set according to the following equations:

$$V_{OUT1} = 0.50\ V(1 + R1/R2)$$

$$V_{OUT2} = 0.50\ V(1 + R3/R4)$$

The value of R1 and R3 should be less than 200 kΩ to minimize errors in the output voltage caused by the ADJx pin input current. For example, when R1 and R2 each equal 200 kΩ, the output voltage is 1.0 V. The output voltage error introduced by the ADJx pin input current is 2 mV or 0.20%, assuming a typical ADJx pin input current of 10 nA at 25°C.

The output voltage of the ADP223/ADP225 may be set from 0.5 V to 5.0 V.

The ADP222/ADP224 are available in multiple output voltage options ranging from 0.8 V to 3.3 V.

The ADP224/ADP225 are identical to the ADP222/ADP223 with the addition of a quick output discharge (QOD) feature. This allows the output voltage to start up from a known state.

The ADP222/ADP223/ADP224/ADP225 use the EN1/EN2 pins to enable and disable the VOUT1/VOUT2 pins under normal operating conditions. When EN1/EN2 are high, VOUT1/VOUT2 turn on; when EN1/EN2 are low, VOUT1/VOUT2 turn off. For automatic startup, EN1/EN2 can be tied to VIN.

# APPLICATIONS INFORMATION

## CAPACITOR SELECTION

### Output Capacitor

The ADP222/ADP223/ADP224/ADP225 are designed for operation with small, space-saving ceramic capacitors but function with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 0.7 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP222/ADP223/ADP224/ADP225. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP222/ADP223/ADP224/ADP225 to large changes in load current. Figure 65 shows the transient responses for an output capacitance value of 1 µF.

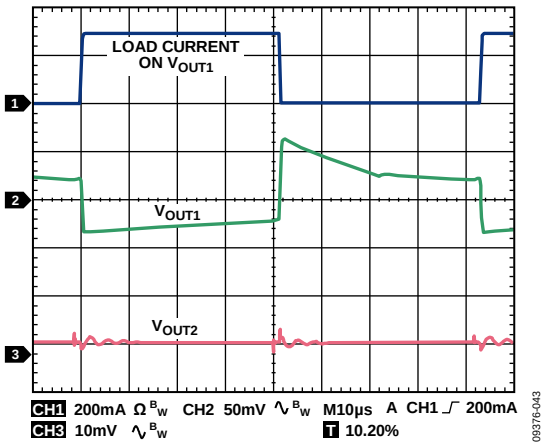


*Figure 65. Output Transient Response, $C_{OUT}$ = 1 µF*

### Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If greater than 1 µF of output capacitance is required, the input capacitor should be increased to match it.

### Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP222/ADP223/ADP224/ADP225, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended, but Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 66 depicts the capacitance vs. voltage bias characteristic of an 0402, 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is ~±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

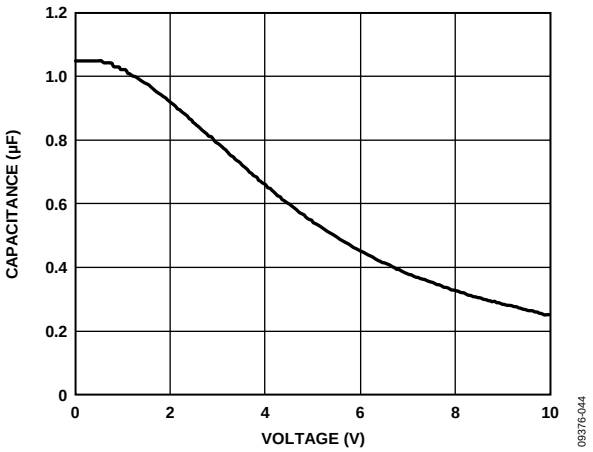


*Figure 66. Capacitance vs. Voltage Bias Characteristic*

Use Equation 1 to determine the worst-case capacitance accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
$C_{BIAS}$ is the effective capacitance at the operating voltage.
*TEMPCO* is the worst-case capacitor temperature coefficient.
*TOL* is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and $C_{BIAS}$ is 0.94 µF at 1.8 V, as shown in Figure 66.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP222/ADP223/ADP224/ADP225, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

## ENABLE FEATURE

The ADP222/ADP223/ADP224/ADP225 use the ENx pins to enable and disable the VOUTx pins under normal operating conditions. Figure 67 shows a rising voltage on ENx crossing the active threshold, where $V_{OUTx}$ turns on. When a falling voltage on ENx crosses the inactive threshold, $V_{OUTx}$ turns off.

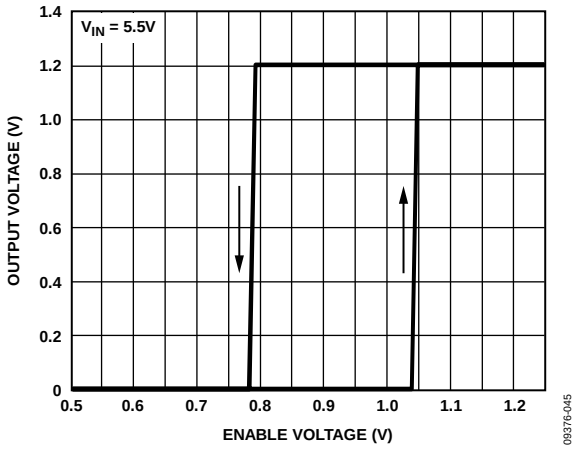


*Figure 67. Typical ENx Pin Operation, $V_{IN}$ = 5.5 V*

As shown in Figure 67, the ENx pins have built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the ENx pins as it passes through the threshold points.

The active/inactive thresholds of the ENx pins are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 68 shows typical ENx active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

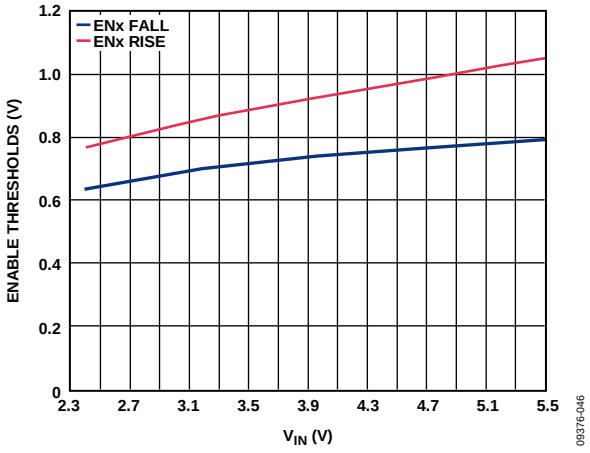


*Figure 68. Typical Enable Thresholds vs. Input Voltage*

The ADP222/ADP223/ADP224/ADP225 use an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 2.8 V option is approximately 240 µs from the time the ENx active threshold is crossed to when the output reaches 90% of its final value. The start-up time is somewhat dependent on the output voltage setting and increases slightly as the output voltage increases.

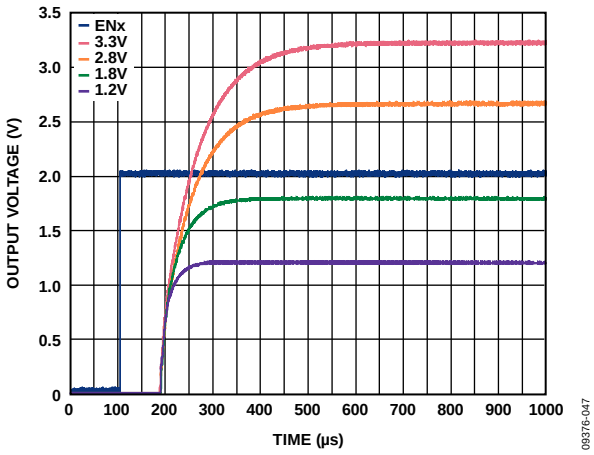


*Figure 69. Typical Start-Up Time*

## PARALLELING OUTPUTS TO INCREASE OUTPUT CURRENT

The ADP223/ADP225 use a single band gap to generate the reference voltage for each LDO. The reference voltages are trimmed to plus or minus a couple of millivolts of each other. This allows paralleling of the LDOs to increase the output current to 600 mA. The adjust pins of each LDO are tied together and a single output voltage divider sets the output voltage. Even though the output voltage of each LDO is slightly different, at high load currents, the resistance of the package and the board layout absorbs the difference. Figure 70 shows the schematic of a typical application where the LDO outputs are paralleled.

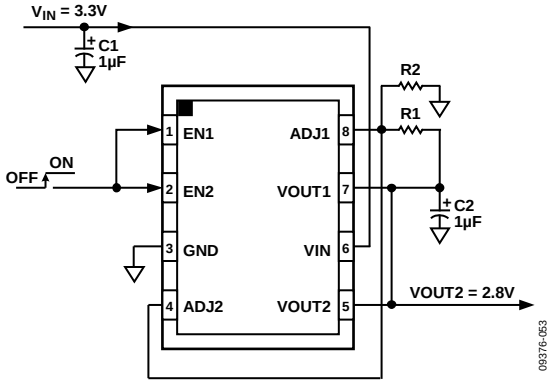


*Figure 70. Paralleling Outputs for Higher Output Current*

## QUICK OUTPUT DISCHARGE (QOD) FUNCTION

The ADP224/ADP225 include an output discharge resistor to force the voltage on each output to zero when the respective LDO is disabled. This ensures that the outputs of the LDOs are always in a well-defined state, regardless if it is enabled or not. The ADP222/ADP223 do not include the output discharge function. Figure 71 compares the turn-off time of a 3.3 V output LDO with and without the QOD function. Both LDOs have a 1 kΩ resistor connected to each output. The LDO with the QOD function discharges the output to 0 V in less than 1 ms, whereas the 1 kΩ load takes over 5 ms to do the same.

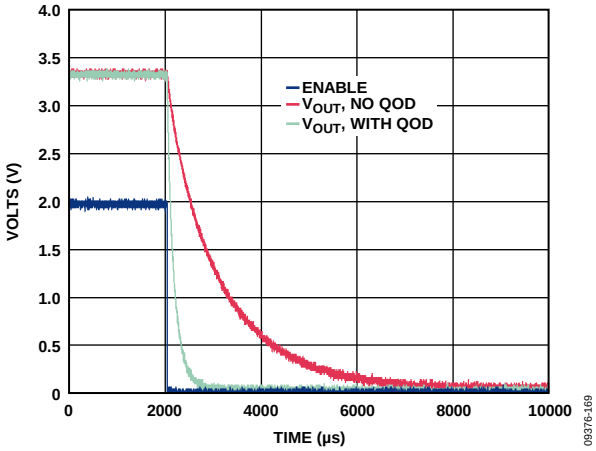


*Figure 71. Typical Turn-Off Time with and Without QOD Function*

## CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP222/ADP223/ADP224/ADP225 are protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP222/ADP223/ADP224/ADP225 are designed to current limit when the output load reaches 300 mA (typical). When the output load exceeds 300 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 155°C (typical). Under extreme conditions (that is, high ambient temperature and power dissipation) when the junction temperature starts to rise above 155°C, the output is turned off, reducing the output current to 0. When the junction temperature drops below 140°C, the output is turned on again, and output current is restored to its nominal value.

Consider the case where a hard short from VOUTx to ground occurs. At first, the ADP222/ADP223/ADP224/ADP225 current limits, so that only 300 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 155°C, thermal shutdown activates, turning off the output and reducing the output current to 0 mA. As the junction temperature cools and drops below 140°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 155°C. This thermal oscillation between 140°C and 155°C causes a current oscillation between 300 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that junction temperatures do not exceed 125°C.

## THERMAL CONSIDERATIONS

In most applications, the ADP222/ADP223/ADP224/ADP225 do not dissipate much heat due to its high efficiency. However, in applications with high ambient temperature, and high supply voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 155°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 140°C to prevent any permanent damage. Therefore, thermal analysis for the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to the power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP222/ADP223/ADP224/ADP225 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the power device, and thermal resistances between the junction and ambient air ($\theta_{JA}$). The $\theta_{JA}$ number is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pin to the PCB.

Table 6 shows typical $\theta_{JA}$ values of the 8-lead LFCSP package for various PCB copper sizes, and Table 7 shows the typical $\Psi_{JB}$ value of the 8-lead LFCSP.

**Table 6. Typical $\theta_{JA}$ Values**

| Copper Size (mm²) | $\theta_{JA}$ (°C/W) |
|---|---|
| 25[1] | 175.1 |
| 100 | 135.6 |
| 500 | 77.3 |
| 1000 | 65.2 |
| 6400 | 51 |

[1] Device soldered to minimum size pin traces.

**Table 7. Typical $\Psi_{JB}$ Value**

| Model | $\Psi_{JB}$ (°C/W) |
|---|---|
| 8-Lead LFCSP | 18.2 |

The junction temperature of the ADP222/ADP223/ADP224/ADP225 can be calculated by

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
$T_A$ is the ambient temperature.
$P_D$ is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND})$$

where:
$I_{LOAD}$ is the load current.
$I_{GND}$ is the ground current.
$V_{IN}$ and $V_{OUT}$ are input and output voltages, respectively.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\}$$

As shown in the simplified equation, for a given ambient temperature, input- to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 72 to Figure 75 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

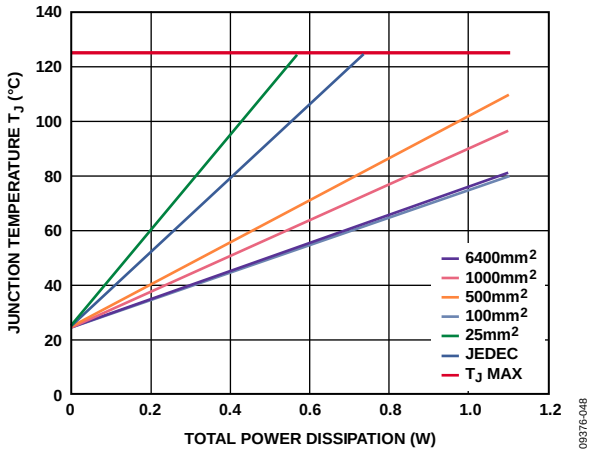


*Figure 72. 8-Lead LFCSP, $T_A$ = 25°C*

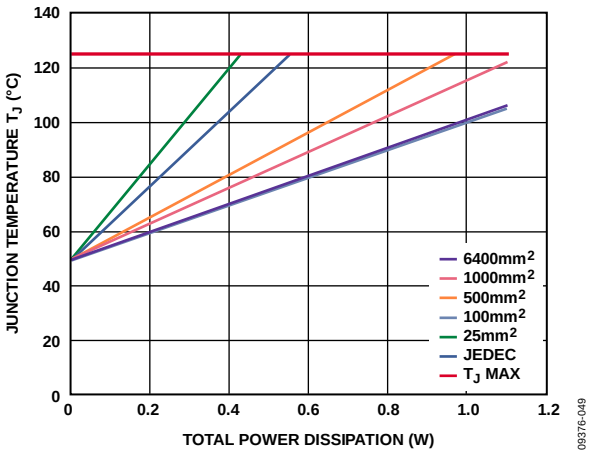


*Figure 73. 8-Lead LFCSP, $T_A$ = 50°C*

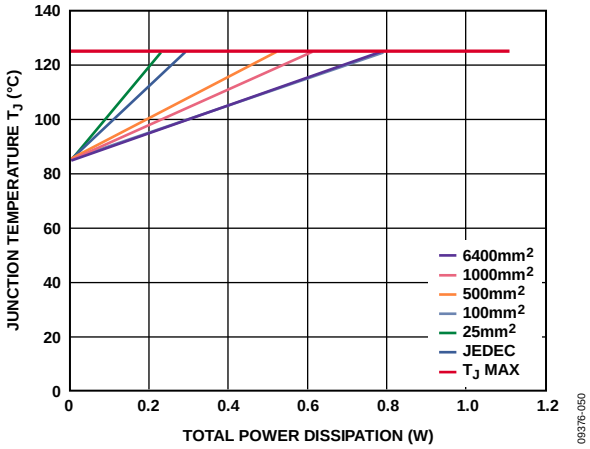


*Figure 74. 8-Lead LFCSP, $T_A$ = 85°C*

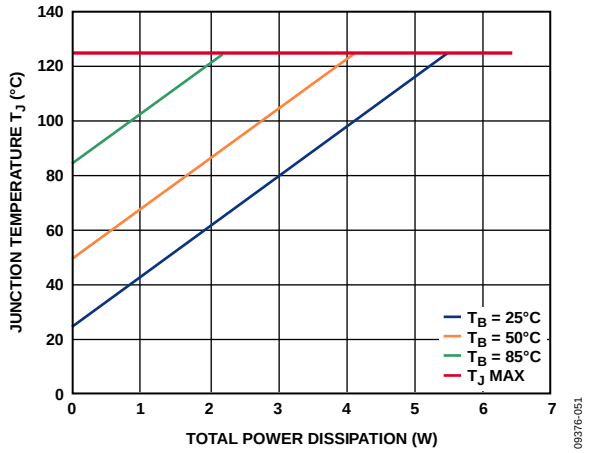


*Figure 75. 8-Lead LFCSP, $T_A$ = 85°C*

In the case where the board temperature is known, use the thermal characterization parameter, $\Psi_{JB}$, to estimate the junction temperature rise (see Figure 75). Maximum junction temperature ($T_J$) is calculated from the board temperature ($T_B$) and power dissipation ($P_D$) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (3)$$

The typical value of $\Psi_{JB}$ is 18.2°C/W for the 8-lead LFCSP package.

## PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP222/ADP223/ADP224/ADP225. However, as listed in Table 6, a point of diminishing returns is eventually reached beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUTx and GND pins. Use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

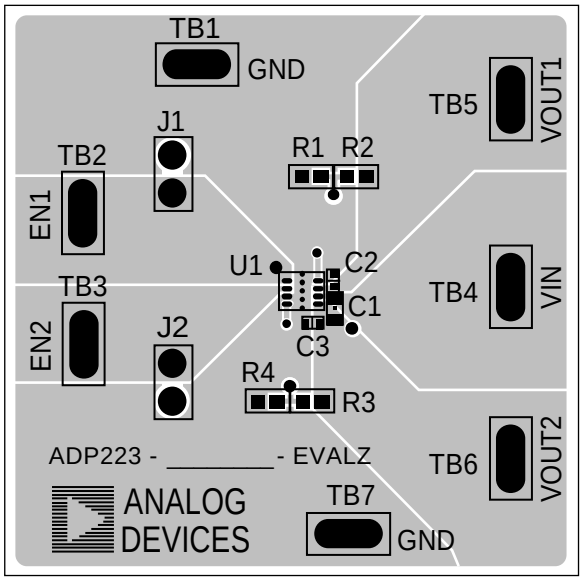


*Figure 76. Example 8-Lead LFCSP PCB Layout*

# OUTLINE DIMENSIONS

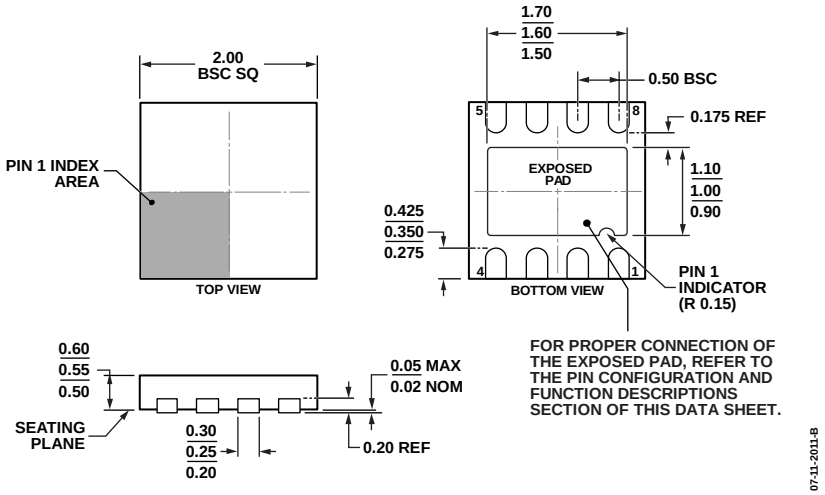


*Figure 77. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]*
*2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead*
*(CP-8-10)*
*Dimensions shown in millimeters*

## ORDERING GUIDE

| Model[1] | Temperature Range | Output Voltage (V) | | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| | | VOUT1 | VOUT2 | | | |
| ADP222ACPZ-1218-R7 | −40°C to +125°C | 1.2 | 1.8 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | L16 |
| ADP222ACPZ-1228-R7 | −40°C to +125°C | 1.2 | 2.8 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | L17 |
| ADP222ACPZ-1233-R7 | −40°C to +125°C | 1.2 | 3.3 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | L18 |
| ADP222ACPZ-1528-R7 | −40°C to +125°C | 1.5 | 2.8 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKR |
| ADP222ACPZ-1533-R7 | −40°C to +125°C | 1.5 | 3.3 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKS |
| ADP222ACPZ-1815-R7 | −40°C to +125°C | 1.8 | 1.5 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LL0 |
| ADP222ACPZ-1825-R7 | −40°C to +125°C | 1.8 | 2.5 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LL1 |
| ADP222ACPZ-1827-R7 | −40°C to +125°C | 1.8 | 2.7 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | L3A |
| ADP222ACPZ-1833-R7 | −40°C to +125°C | 1.8 | 3.3 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LL2 |
| ADP222ACPZ-2725-R7 | −40°C to +125°C | 2.7 | 2.5 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LN8 |
| ADP222ACPZ-2818-R7 | −40°C to +125°C | 2.8 | 1.8 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LL3 |
| ADP222ACPZ-2827-R7 | −40°C to +125°C | 2.8 | 2.7 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LJE |
| ADP222ACPZ-3325-R7 | −40°C to +125°C | 3.3 | 2.5 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKV |
| ADP222ACPZ-3328-R7 | −40°C to +125°C | 3.3 | 2.8 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKW |
| ADP222ACPZ-3330-R7 | −40°C to +125°C | 3.3 | 3.0 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKX |
| ADP224ACPZ-2818-R7 | −40°C to +125°C | 2.8 | 1.8 | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKP |

| Model[1] | Temperature Range | Output Voltage (V) | | Package Description | Package Option | Branding |
|---|---|---|---|---|---|---|
| | | VOUT1 | VOUT2 | | | |
| ADP225ACPZ-R7 | −40°C to +125°C | Adjustable | Adjustable | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LKQ |
| ADP223ACPZ-R7 | −40°C to +125°C | Adjustable | Adjustable | 8-Lead Lead Frame Chip Scale Package [LFCSP_UD] | CP-8-10 | LJQ |
| ADP223CP-EVALZ | | Adjustable | Adjustable | Evaluation Board | | |
| ADP225CP-EVALZ | | Adjustable | Adjustable | Evaluation Board | | |

[1] Z = RoHS Compliant Part.


D09376-0-1/13(D)