BENCHMARQ

bq2005

Fast-Charge IC for Dual-Battery Packs

Features

- Sequential fast charge and conditioning of two NiCd or NiMH nickel cadmium or nickel-metal hydride battery packs
- Hysteretic PWM switch-mode current regulation or gated control of an external regulator
- Easily integrated into systems or used as a stand-alone charger
- Pre-charge qualification of temperature and voltage
- Direct LED outputs display battery and charge status
- Fast-charge termination by Δ temperature/Δ time, -ΔV, maximum voltage, maximum temperature, and maximum time
- Optional top-off and pulse-trickle charging

General Description

The bq2005 Fast-Charge IC provides comprehensive fast charge control functions together with high-speed switching power control circuitry on a monolithic CMOS device for sequential charge management in dual battery pack applications.

Integration of closed-loop current control circuitry allows the bq2005 to be the basis of a cost-effective solution for stand-alone and system-integrated chargers for batteries of one or more cells.

Switch-activated discharge-before-charge allows bq2005-based chargers to support battery conditioning and capacity determination.

High-efficiency power conversion is accomplished using the bq2005 as a hysteretic PWM controller for switch-mode regulation of the charging current. The bq2005 may alternatively be used to gate an externally regulated charging current.

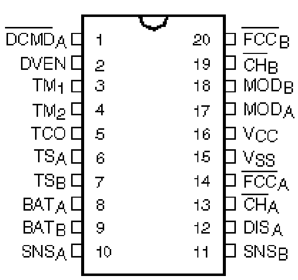
Fast charge may begin on application of the charging supply, replacement of the battery, or switch depression. For safety, fast charge is inhibited unless/until the battery temperature and voltage are within configured limits.

Temperature, voltage, and time are monitored throughout fast charge. Fast charge is terminated by any of the following:

- Rate of temperature rise ($\Delta T/\Delta t$)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, optional top-off and pulsed current maintenance phases are available.

Pin Connections



20-Pin DIP or SOIC

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Pin Names

$\overline{DCMD}_A$	Discharge command input, battery A	DIS_A	Discharge control output, battery A
DVEN	DV enable	$\overline{CH}_A$, $\overline{CH}_B$	Charge status output, battery A/B
TM_1	Timer mode select 1	$\overline{FCC}_A$, $\overline{FCC}_B$	Fast charge complete output, battery A/B
TM_2	Timer mode select 2	V_{SS}	System ground
TCO	Temperature cut-off	V_{CC}	5.0V ±10% power
TS_A, TS_B	Temperature sense input, battery A/B	MOD_A, MOD_B	Charge current control output, battery A/B
BAT_A, BAT_B	Battery voltage input, battery A/B		
SNSA, SNSB	Sense resistor input, battery A/B		

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Pin Descriptions

$DCMD_A$ **Discharge-before-charge control input, battery A**

$\overline{DCMD_A}$ controls the discharge-before-charge function of the bq2005. A negative-going pulse on $\overline{DCMD_A}$ initiates a discharge to EDV followed by a charge if conditions allow. By tying $\overline{DCMD_A}$ to ground, automatic discharge-before-charge is enabled on every new charge cycle start.

DVEN **-ΔV enable input**

This input enables/disables -ΔV charge termination. If DVEN is high, the -ΔV test is enabled. If DVEN is low, -ΔV test is disabled. The state of DVEN may be changed at any time.

TM_1–TM_2 **Timer mode inputs**

TM_1 and TM_2 are three-state inputs that configure the fast charge safety timer, -ΔV hold-off time, and that enhance/disable top-off. See Table 2.

TCO **Temperature cutoff threshold input**

Input to set maximum allowable battery temperature. If the potential between TS_A and SNS_A or TSB and SNS_B is less than the voltage at the TCO input, then fast charge or top-off charge is terminated for the corresponding battery pack.

TS_A, TS_B **Temperature sense inputs**

Input, referenced to SNS_A or SNS_B, respectively, for an external thermistor monitoring battery temperature.

BAT_A, BAT_B **Voltage inputs**

The battery voltage sense input, referenced to $SNS_{A,B}$, respectively. This is created by a high-impedance resistor divider network connected between the positive and the negative terminals of the battery.

SNS_A, SNS_B **Charging current sense inputs,**

$SNS_{A,B}$ controls the switching of $MOD_{A,B}$ based on the voltage across an external sense resistor in the current path of the battery. SNS is the reference potential for the TS and BAT pins. If SNS is connected to V_{SS}, MOD switches high at the beginning of charge and low at the end of charge.

DIS_A **Discharge control output**

Push-pull output used to control an external transistor to discharge battery A before charging.

$\overline{CH_A}$, $\overline{CH_B}$ **Charge status outputs**

Push-pull outputs indicating charging status for batteries A and B, respectively. See Figure 1 and Table 2.

$\overline{FCC_A}$, $\overline{FCC_B}$ **Fast charge complete outputs**

Open-drain outputs indicating fast charge complete for batteries A and B, respectively. See Figure 1 and Table 2.

MOD_A, MOD_B **Charge current control outputs**

$MOD_{A,B}$ is a push-pull output that is used to control the charging current to the battery. $MOD_{A,B}$ switches high to enable charging current to flow and low to inhibit charging current flow to batteries A and B, respectively.

V_{CC} **V_{CC} supply input**

5.0 V, ±10% power input.

V_{SS} **Ground**

Functional Description

Figure 3 shows a block diagram and Figure 4 shows a state diagram of the bq2005.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, $BAT_{A,B}$, must be divided down to between $0.95 * V_{CC}$ and $0.475 * V_{CC}$ for proper operation. A resistor-divider ratio of:

$$\frac{RB1}{RB2} = \frac{N}{2.375} - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor

The valid battery voltage range is $V_{EDV} < V_{BAT} < V_{MCV}$. The valid temperature range is $V_{HTF} < V_{TEMP} < V_{LTF}$, where:

$$V_{LTF} = 0.4 * V_{CC} \pm 30mV$$

$$V_{HTF} = [(1/4 * V_{LTF}) + (3/4 * V_{TCO})] \pm 30mV$$

V_{TCO} is the voltage presented at the TCO input pin, and is configured by the user with a resistor divider between V_{CC} and ground. The allowed range is 0.2 to $0.4 * V_{CC}$.

If the temperature of the battery is out of range, or the voltage is too low, the chip enters the charge pending state and waits for both conditions to fall within their allowed limits. The $MOD_{A,B}$ output is modulated to provide the configured trickle charge rate in the charge pending state. There is no time limit on the charge pending state; the charger remains in this state as long as the voltage or temperature conditions are outside of the allowed limits. If the voltage is too high, the chip goes to the battery absent state and waits until a new charge cycle is started.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Delta temperature/delta time ($\Delta T/\Delta t$)
- Negative delta voltage ($-\Delta V$)
- Maximum voltage
- Maximum temperature
- Maximum time

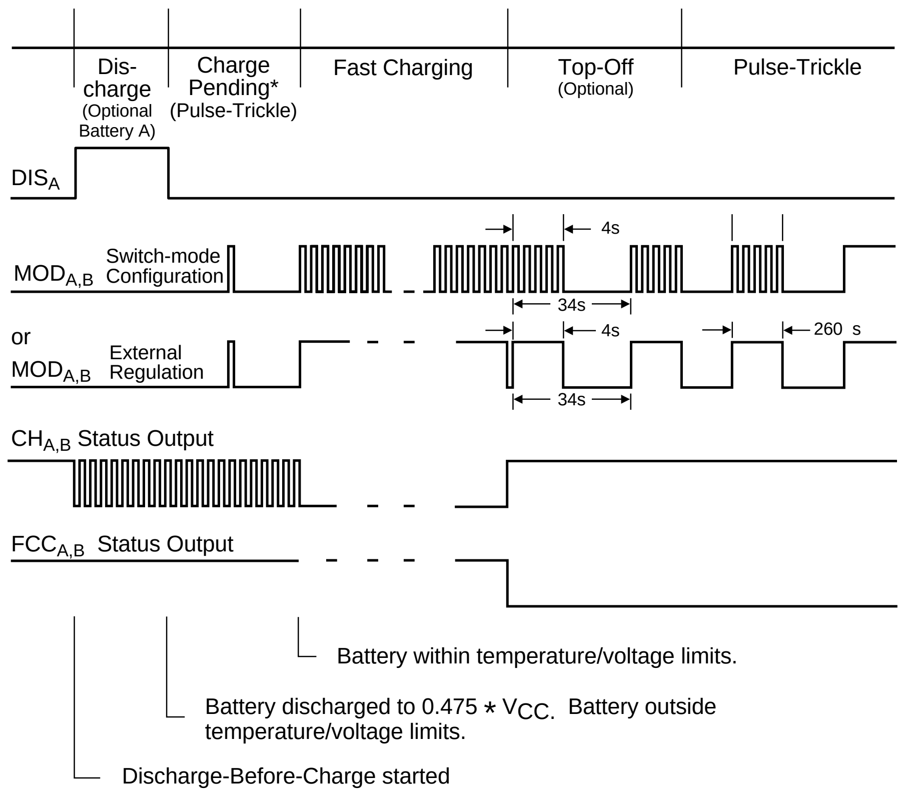

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Table 1. Fast Charge Safety Time/Hold-Off/Top-Off Table

Corresponding Fast-Charge Rate	TM1	TM2	Typical Fast-Charge and Top-Off Time Limits	Typical -ΔV/MCV Hold-Off Time (seconds)	Top-Off Rate
C/4	Low	Low	360	137	Disabled
C/2	Float	Low	180	820	Disabled
1C	High	Low	90	410	Disabled
2C	Low	Float	45	200	Disabled
4C	Float	Float	23	100	Disabled
C/2	High	Float	180	820	C/16
1C	Low	High	90	410	C/8
2C	Float	High	45	200	C/4
4C	High	High	23	100	C/2

Note: Typical conditions = 25°C, V_{CC} = 5.0V.

- V Termination

If the DVEN input is high, the bq2005 samples the voltage at the BAT pin once every 34s. If V_{CELL} is lower than any previously measured value by 12mV ±4mV, fast charge is terminated. The -ΔV test is valid in the range $V_{MCV} - (0.2 * V_{CC}) < V_{CELL} < V_{MCV}$.

Voltage Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off period, -ΔV termination is disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. ΔT/Δt, maximum voltage and maximum temperature terminations are not affected by the hold-off period.

T/ t Termination

The bq2005 samples at the voltage at the TS pin every 34s, and compares it to the value measured two samples earlier. If V_{TEMP} has fallen 16mV ±4mV or more, fast charge is terminated. The ΔT/Δt termination test is valid only when $V_{TCO} < V_{TEMP} < V_{LTF}$.

Temperature Sampling

Each sample is an average of 16 voltage measurements taken 57µs apart. The resulting sample period (18.18ms) filters out harmonics around 55Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50Hz or 60Hz AC sources. Tolerance on all timing is ±16%.

Maximum Voltage, Temperature, and Time

Anytime V_{CELL} rises above V_{MCV}, CHG goes high (the LED goes off) immediately. If the bq2005 is not in the voltage hold-off period, fast charging also ceases immediately. If V_{CELL} then falls back below V_{MCV} before t_{MCV} = 1s (maximum), the chip transitions to the Charge Complete state (maximum voltage termination). If V_{CELL} remains above V_{MCV} at the expiration of t_{MCV}, the bq2005 transitions to the Battery Absent state (battery removal). See Figure 4.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}. Charge will also be terminated if V_{TEMP} rises above the minimum temperature fault threshold, V_{LTF}, after fast charge begins.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/4, C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for the C/2 through 4C rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM_1 and TM_2 input pins. (See Table 2.) During top-off, the CC pin is modulated at a duty cycle of 4s active for every 30s inactive. This modulation results in an average rate 1/8th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

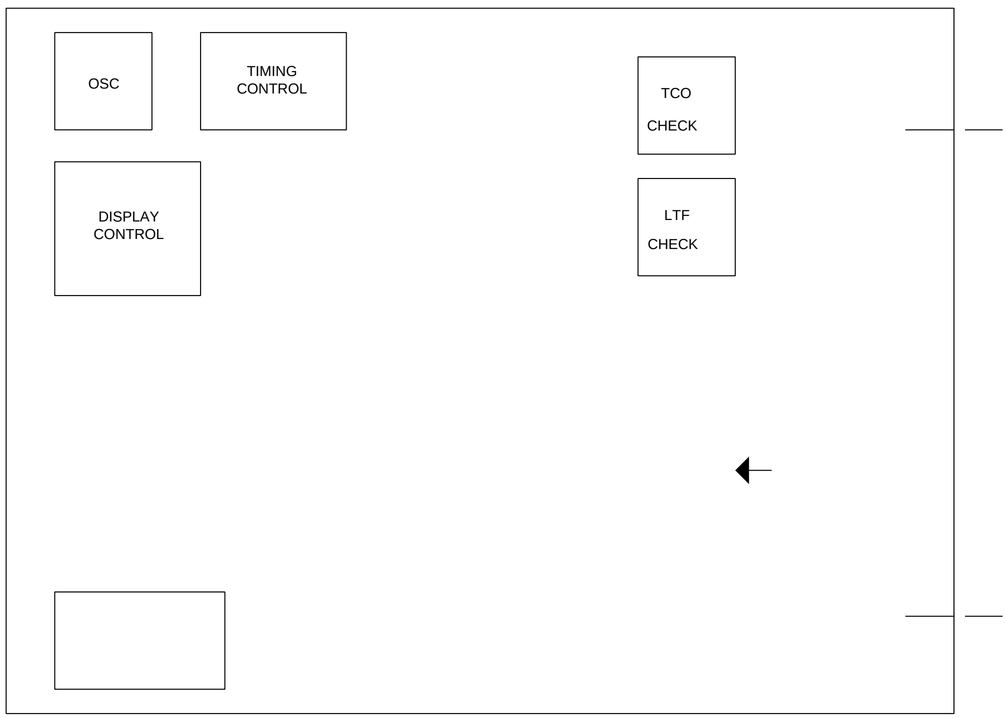
Pulse-Trickle Charge

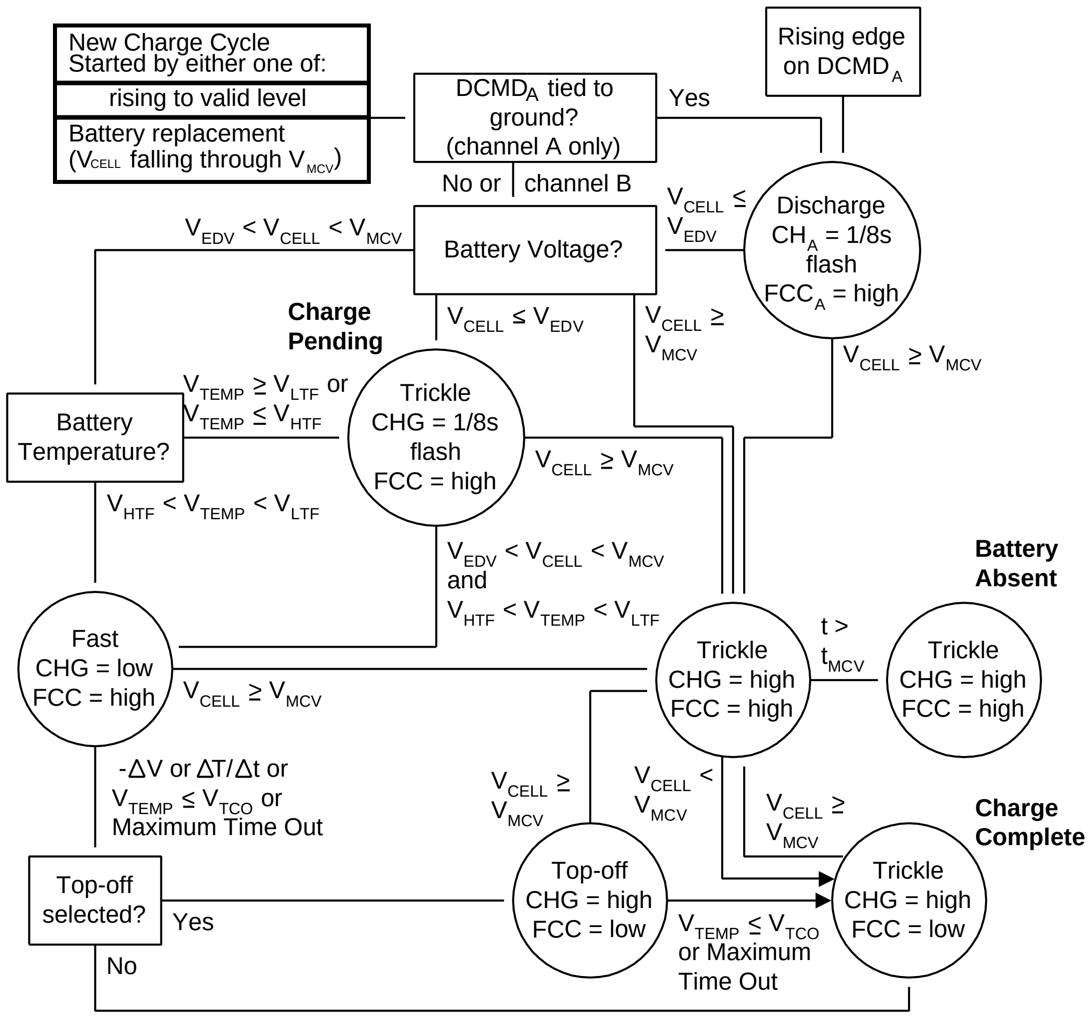
Pulse-trickle charging follows the fast charge and optional top-off charge phases to compensate for self-discharge of the battery while it is idle in the charger. The configured pulse-trickle rate is also applied in the charge pending state to raise the voltage of an over-discharged battery up to the minimum required before fast charge can begin.

In the pulse-trickle mode, MOD is active for 260µs of a period specified by the settings of TM1 and TM2. See Table 1. The resulting trickle-charge rate is C/64 when top-off is enabled and C/32 when top-off is disabled. Both pulse trickle and top-off may be disabled by tying TM1 and TM2 to V_{SS}.

Charge Status Indication

Charge status is indicated by the CHG output. The state of the CHG output in the various charge cycle phases is shown in Figure 4 and illustrated in Figure 2.


OSC
TIMING CONTROL
TCO CHECK
DISPLAY CONTROL
LTF CHECK



New Charge Cycle
Started by either one of:
rising to valid level
Battery replacement
(VCELL falling through VMCV)
DCMDA tied to ground?
(channel A only)
Yes
No or channel B
Rising edge on DCMDA
VCELL ≤ VEDV
Discharge
CHA = 1/8s flash
FCCA = high
VEDV < VCELL < VMCV
Battery Voltage?
VCELL ≤ VEDV
VCELL ≥ VMCV
VCELL ≥ VMCV
Charge Pending
VTEMP ≥ VLTF or
VTEMP ≤ VHTF
Battery Temperature?
Trickle
CHG = 1/8s flash
FCC = high
VCELL ≥ VMCV
VHTF < VTEMP < VLTF
VEDV < VCELL < VMCV
and
VHTF < VTEMP < VLTF
Battery Absent
Fast
CHG = low
FCC = high
VCELL ≥ VMCV
Trickle
CHG = high
FCC = high
t > tMCV
Trickle
CHG = high
FCC = high
-ΔV or ΔT/Δt or
VTEMP ≤ VTCO or
Maximum Time Out
VCELL ≥ VMCV
VCELL < VMCV
VCELL ≥ VMCV
Charge Complete
Top-off selected?
Yes
No
Top-off
CHG = high
FCC = low
VTEMP ≤ VTCO
or Maximum Time Out
Trickle
CHG = high
FCC = low

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} relative to V_{SS}	-0.3	+7.0	V	
V_T	DC voltage applied on any pin excluding V_{CC} relative to V_{SS}	-0.3	+7.0	V	
T_{OPR}	Operating ambient temperature	-20	+70	°C	Commercial
T_{STG}	Storage temperature	-55	+125	°C	
T_{SOLDER}	Soldering temperature	-	+260	°C	10s max.
T_{BIAS}	Temperature under bias	-40	+85	°C	

Note: Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

DC Thresholds ($T_A = T_{OPR}$; V_{CC} ±10%)

Symbol	Parameter	Rating	Tolerance	Unit	Notes
V_{SNSHI}	High threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = Low	$0.05 * V_{CC}$	±0.025	V	
V_{SNSLO}	Low threshold at $SNS_{A,B}$ resulting in $MOD_{A,B}$ = High	$0.04 * V_{CC}$	±0.010	V	
V_{LTF}	Low-temperature fault	$0.4 * V_{CC}$	±0.030	V	$V_{TEMP} \geq V_{LTF}$ inhibits/ terminates charge
V_{HTF}	High-temperature fault	$(1/4 * V_{LTF}) + (3/4 * V_{TCO})$	±0.030	V	$V_{TEMP} \leq V_{HTF}$ inhibits charge
V_{EDV}	End-of-discharge voltage	$0.475 * V_{CC}$	±0.030	V	$V_{CELL} < V_{EDV}$ inhibits fast charge
V_{MCV}	Maximum cell voltage	$0.95 * V_{CC}$	±0.030	V	$V_{CELL} > V_{MCV}$ inhibits/ terminates charge
V_{THERM}	TS input change for $\Delta T/\Delta t$ detection	16	±4	mV	
$-\Delta V$	BAT input change for $-\Delta V$ detection	12	±4	mV	

Recommended DC Operating Conditions (T_A = 0 to +70°C)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.5	5.0	5.5	V	
V_{CELL}	BAT voltage potential	0	-	V_{CC}	V	V_{BAT} - V_{SNS}
V_{BAT}	Battery input	0	-	V_{CC}	V	
V_{TEMP}	TS voltage potential	0	-	V_{CC}	V	V_{TS} - V_{SNS}
V_{TS}	Thermistor input	0	-	V_{CC}	V	
V_{TCO}	Temperature cutoff	$0.2 * V_{CC}$	-	$0.4 * V_{CC}$	V	
V_{IH}	Logic input high	2.0	-	-	V	$\overline{DCMD}_A$, DVEN
	Logic input high	V_{CC} - 0.3	-	-	V	TM_1, TM_2
V_{IL}	Logic input low	-	-	0.8	V	$\overline{DCMD}_A$, DVEN
	Logic input low	-	-	0.3	V	TM_1, TM_2
V_{OH}	Logic output high	V_{CC} - 0.5	-	-	V	DIS_A, $MOD_{A,B}$, $I_{OH} \leq$ -5mA
V_{OL}	Logic output low	-	-	0.5	V	DIS_A, $\overline{FCC}_{A,B}$, $\overline{CH}_{A,B}$, $MOD_{A,B}$, $I_{OL} \leq$ 5mA
I_{CC}	Supply current	-	1.0	3.0	mA	Outputs unloadmH5.1(.581 0 0 5.833 94.968 393.466 Tm

Timing **(T_A = 0 to +70°C; V**

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
3	9	V_{SNSLO} rating	Was V_{SNSHI} - (0.01 * V_{CC}); is 0.04 * V_{CC}
4	5	Corrected sample period	Was: 32s; Is: 34s
4	5, 9	Corrected -ΔV threshold	Was: 13mV Is: 12mV
4	All	Revised and expanded format of this data sheet	Clarification
5	9	T_{OPR}	Deleted industrial temperature range
6	1, 13	Deleted DIP package option	Removed DIP from pinout drawing and Ordering Information; deleted DIP package specifications

Notes: Change 3 = Sept. 1996 D changes from Nov. 1993 C.
Change 4 = Nov. 1997 E changes from Sept. 1996 D.
Change 5 = June 1999 F changes from Nov. 1997 E.
Change 6 = Aug. 2000 G changes from June 1999 F

Ordering Information

bq2005 _

Package Option:
S = 20-pin SOIC

Device:
bq2005 Dual-Battery Fast-Charge IC

S: 20-Pin SOIC

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ2005PN	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	-20 to 70		
BQ2005S	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D	Samples
BQ2005SG4	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D	Samples
BQ2005STR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D	Samples
BQ2005STRG4	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 70	2005S -D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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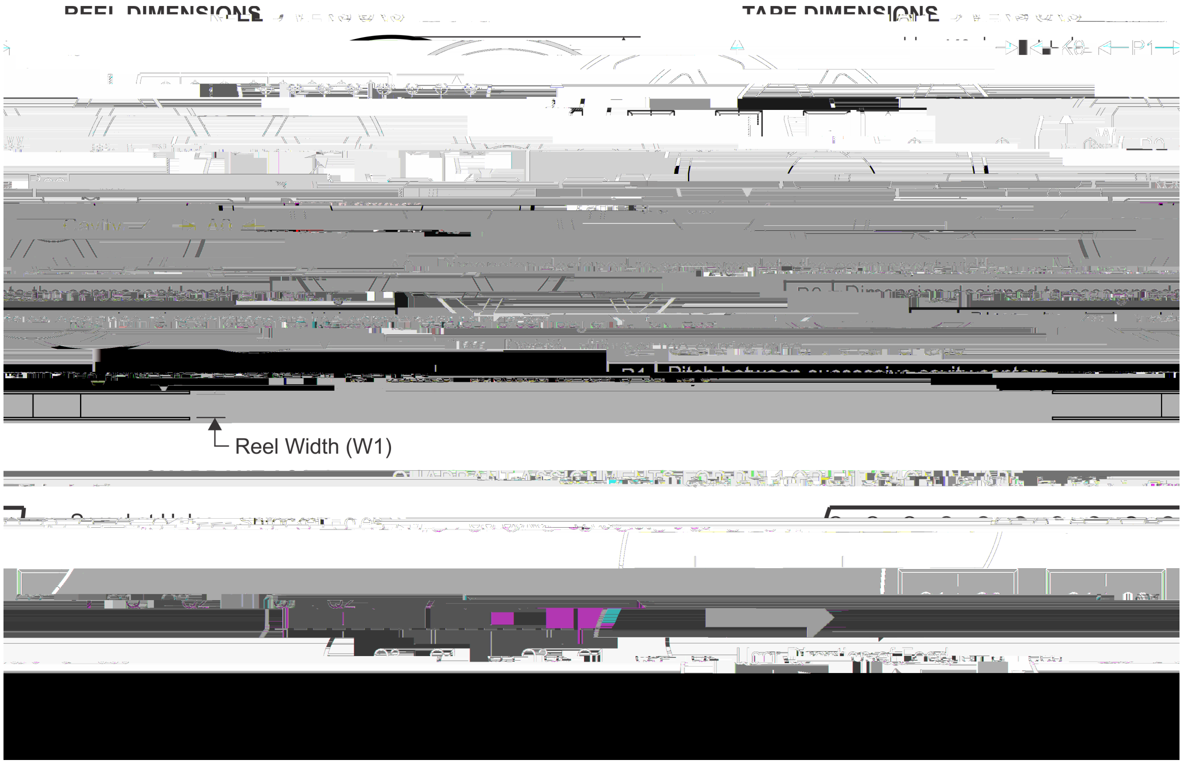
TEXAS
INSTRUMENTS

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2005STR	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1

[redacted]

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2005STR	SOIC	DW	20	2000	367.0	367.0	45.0

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