# Overvoltage and Overcurrent Protection IC and Li+ Charger Front-End Protection IC

**Check for Samples :bq24308**

## FEATURES

- **Provides Protection for Three Variables:**
  - **Input Overvoltage**
  - **Input Overcurrent with Current Limiting**
  - **Battery Overvoltage**
- **30V Maximum Input Voltage**
- **Supports Up to 1.5A Input Current**
- **Robust Against False Triggering Due to Current Transients**
- **Thermal Shutdown**
- **LDO Mode Voltage Regulation of 5V**
- **Small 2 mm × 2 mm 8-Pin SON Package**

## APPLICATIONS

- **Mobile and Smart Phones**
- **PDAs**
- **MP3 Players**
- **Low-Power Handheld Devices**
- **Bluetooth Headsets**

## DESCRIPTION

The bq24308 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. In case of an input over-voltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an over-current condition, it limits the current to a safe value for a blanking duration before turning the switch off. Battery voltage may also be monitored and if the battery voltage exceeds the specified value the internal switch is turned off. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

The input over-current threshold can be increased using an external resistor. The IC also offers optional protection against reverse voltage at the input using an external P-channel FET.

## PINOUT
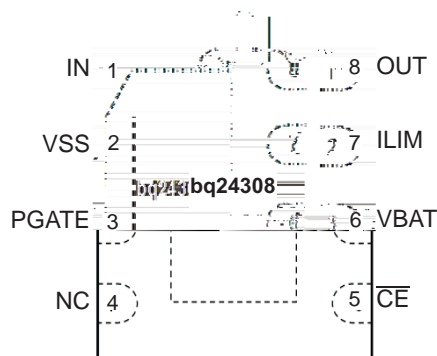


## TYPICAL APPLICATION CIRCUIT
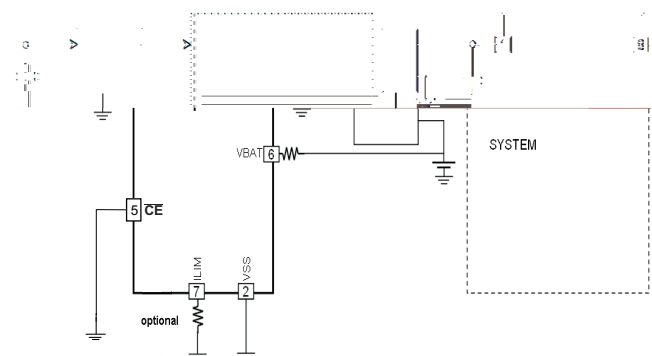


⚠ Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PowerPAD is a trademark of Texas Instruments.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE DISSIPATION RATINGS

| PACKAGE | R $_{JC}$ | R $_{JA}$ (1) |
|---|---|---|
| DSG | 5°C/W | 75°C/W |

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a Cu pad on the board. The pad is connected to the ground plane by a 2x3 via matrix.

## ABSOLUTE MAXIMUM RATINGS[1]

over operating free-air temperature range (unless otherwise noted)

| | | VALUE | UNIT |
|---|---|---|---|
| Input voltage | IN, PGATE (with respect to VSS) | −0.3 to 30 | V |
| | OUT (with respect to VSS) | −0.3 to 12 | V |
| | ILIM, $\overline{CE}$, VBAT (with respect to VSS) | −0.3 to 7 | V |
| Input current | IN | 2.0 | A |
| Output current | OUT | 2.0 | A |
| | PGATE | 5 | mA |
| ESD Withstand voltages | All (Human body Model per JESD22-A114-E) | 2000 | V |
| | All (Machine Model per JESD22-A115-A) | 200 | V |
| | All (Charged Device Model per JESD22-C101-C) | 500 | V |
| | IN (IEC 61000-4-2) (with IN pin bypassed to VSS with 1.0-μF low-ESR ceramic capacitor) | 15 (Air discharge) 8 (Contact) | kV |
| Junction temperature, $T_J$ | | −40 to 150 | °C |
| Storage temperature, $T_{STG}$ | | −65 to 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | 3.3 | 26 | V |
| $I_{IN}$ | Input current, IN pin | | 1.5 | A |
| $I_{OUT}$ | Current, OUT pin | | 1.5 | A |
| $R_{ILIM}$ | OCP programming resistor | 31 | | k |
| $T_J$ | Junction temperature | −40 | 125 | °C |

## ORDERING INFORMATION

| PART NUMBER | MARKING | MEDIUM | QUANTITY | PACKAGE |
|---|---|---|---|---|
| bq24308DSGR | DAS | Tape and Reel | 3000 | 2mm × 2mm SON |
| bq24308DSGT | DAS | Tape and Reel | 250 | 2mm × 2mm SON |

## ELECTRICAL CHARACTERISTICS

over junction temperature range –40°C   $T_J$   125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | E3ET BT 00 8 Tf 9.60 |
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**bq24308**

## ELECTRICAL CHARACTERISTICS (continued)

over junction temperature range –40°C  $T_J$  125°C and recommended supply voltage (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **LOGIC LEVELS ON CE** | | | | | | |
| $V_{IL}$ | Low-level input voltage | | 0 | | 0.4 | V |
| $V_{IH}$ | High-level input voltage | | 1.4 | | | V |
| $I_{IL}$ | Low-level input current | | | | 1 | A |
| $I_{IH}$ | High-level input current | $V_{CE}$ = 1.8 V | | | 15 | A |
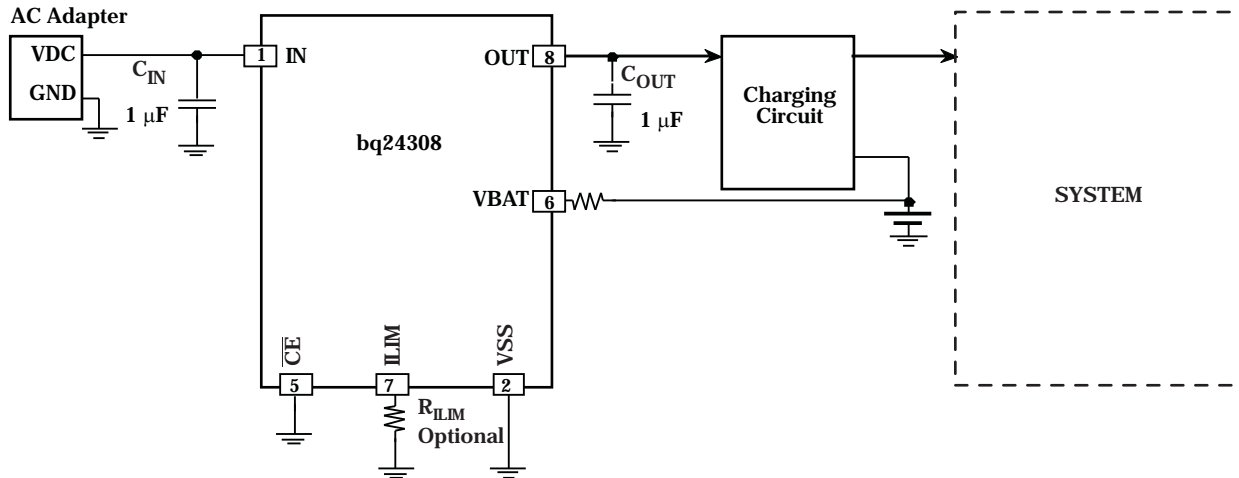


**Figure 1. Overvoltage, Overcurrent, and Battery Overvoltage Protection**
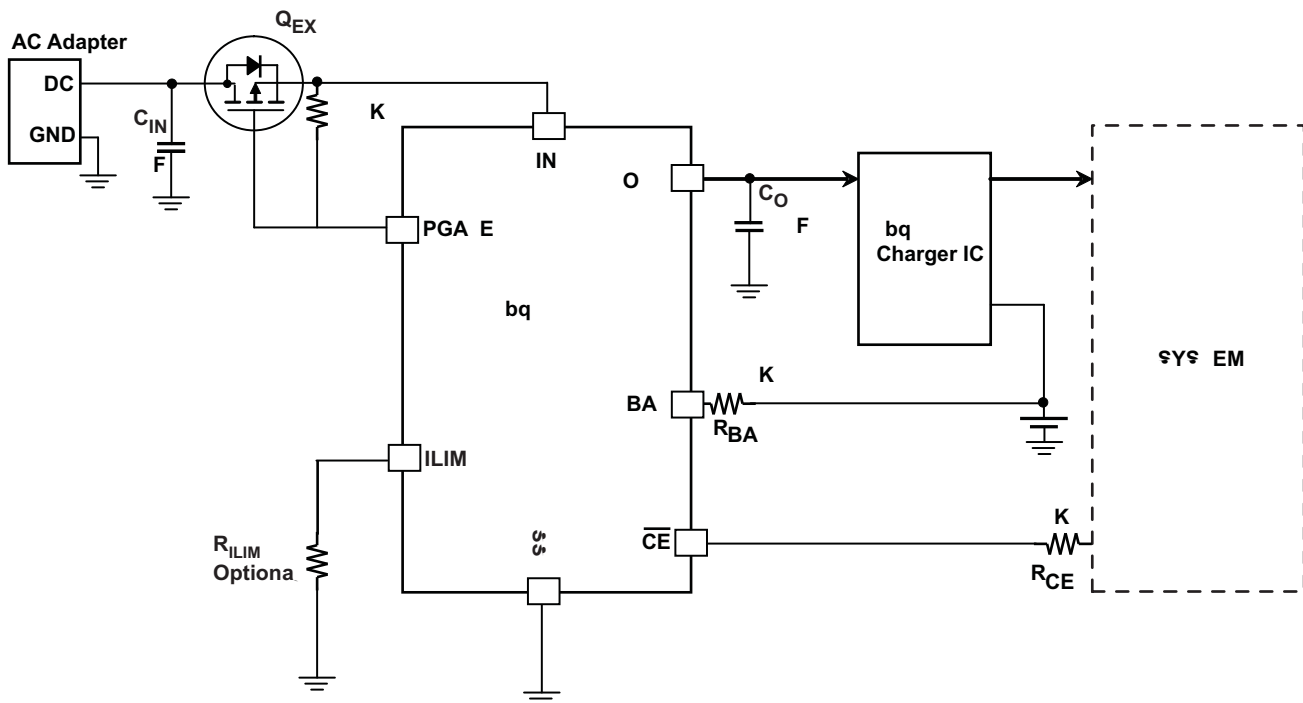


**Figure 2. OVP, OCP, BATOVP With Input Reverse-Polarity Protection**

Product Folder Link(s) :*bq24308*
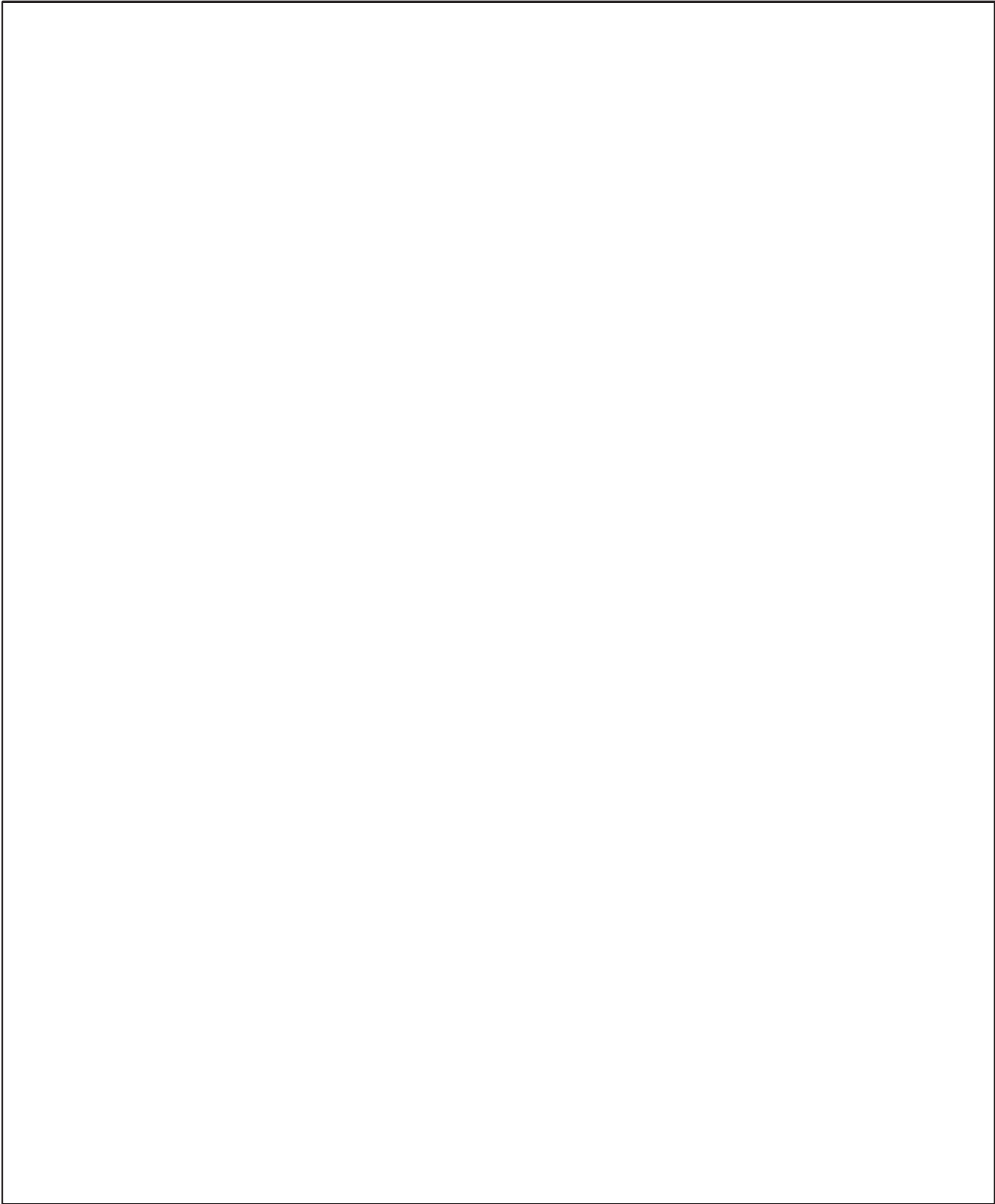
**Figure 3.  Simplified Block Diagram**

## TYPICAL OPERATING PERFORMANCE

Test conditions (unless otherwise noted) for typical operating performance are: $V_{IN}$ = 5 V, $C_{IN}$ = 1 F, $C_{OUT}$ = 1 F, $R_{BAT}$ = 100 k , $R_{OUT}$ = 16 , $T_A$ = 25°C (see Figure 1 - Typical Application Circuit)
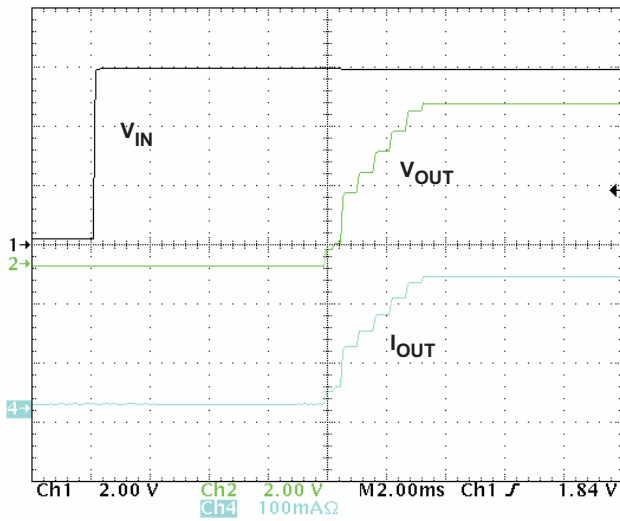


**Figure 4. Normal Power-On Showing Soft-Start.**
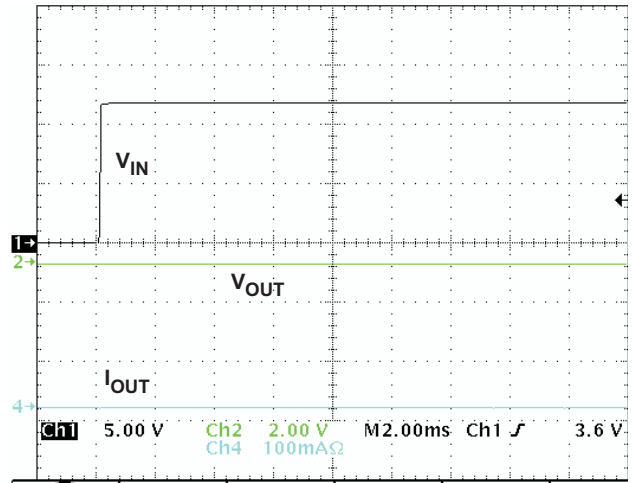$V_{IN}$ 0 V to 6.0 V, $t_R$ = 20 s



**Figure 5. Power-On with Input Overvoltage.**
$V_{IN}$ 0 V to 12.0 V, $t_R$ = 50 s
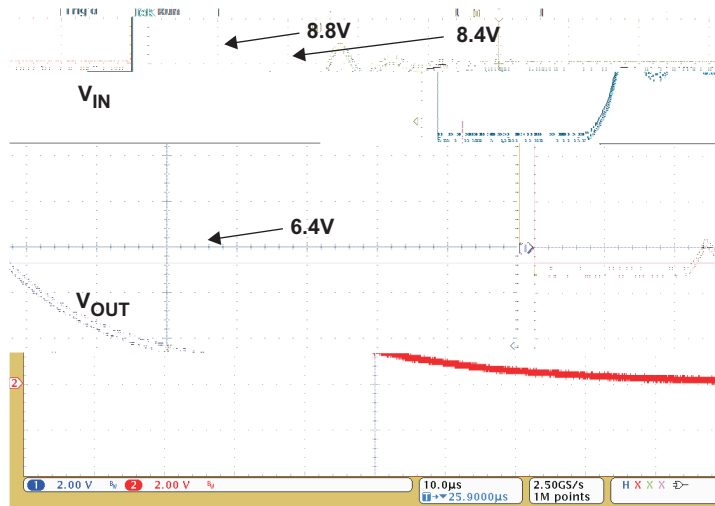


**Figure 6. bq24308 OVP Response for Input Step.**
$V_{IN}$ 5 V to 8 V, $t_R$ = 3 s.

## TYPICAL OPERATING PERFORMANCE
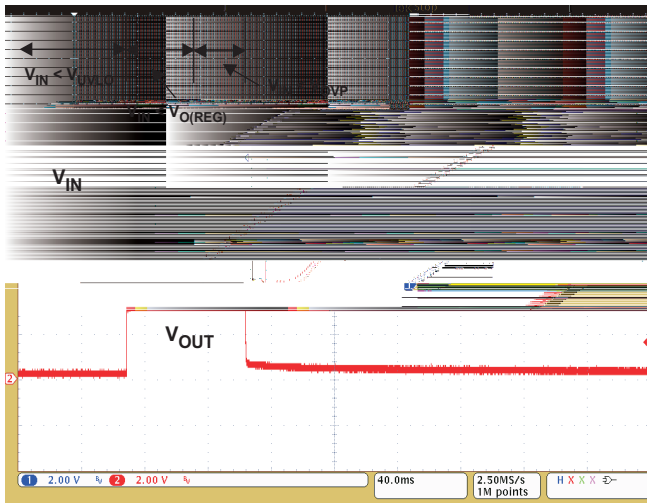


Figure 7. OUT Pin Response to Slow Input Ramp.

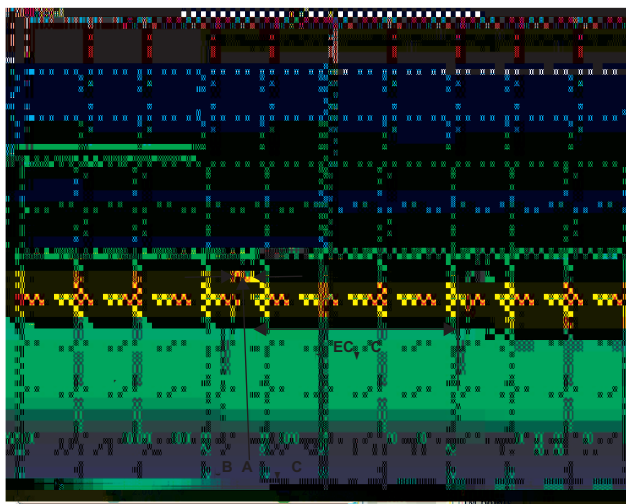Figure 8. bq24308 Recovery from Input OVP.
$V_{IN}$ 8 V to 5 V, $t_F$ = 100 s
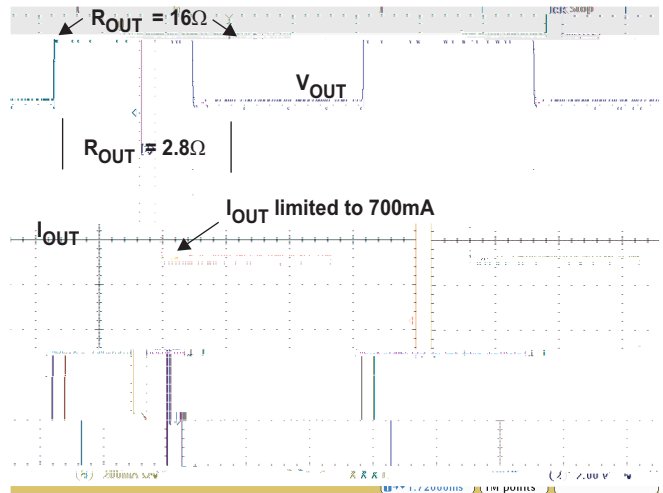


Figure 9. OCP, Powering up with OUT Pin Shorted to VSS

Figure 10. OCP, Showing Current Limiting,
$R_{OUT}$ 16 to 2.8
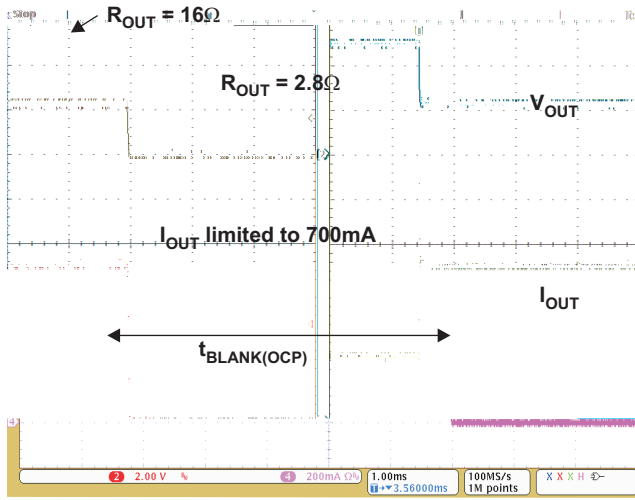
Product Folder Link(s) :*bq24308*

## TYPICAL OPERATING PERFORMANCE (continued)



Figure 11. OCP, Showing Current Limiting and
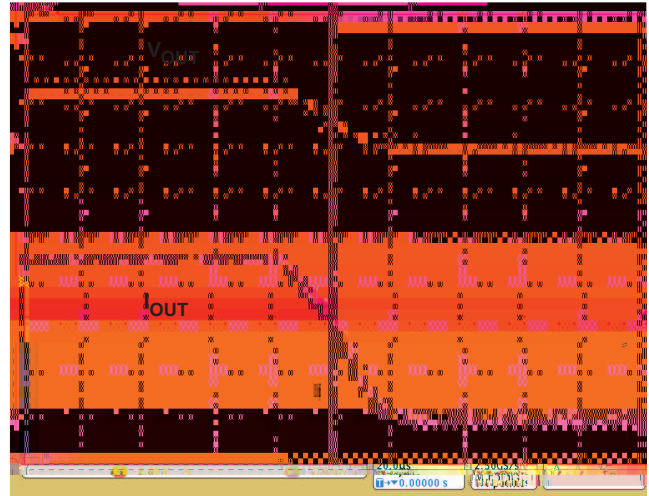OCP Blanking. $R_{OUT}$ 16 to 2.8



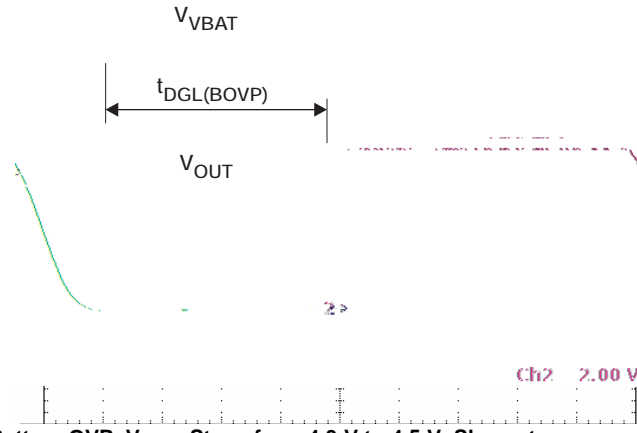Figure 12. Zoom-in on Turn-off Region of Figure 11, Showing
Soft-Stop



Figure 13. Battery OVP. $V_{VBAT}$ Steps from 4.3 V to 4.5 V. Shows $t_{DGL(BOVP)}$ and Soft-Stop

## TYPICAL OPERATING PERFORMANCE (continued)

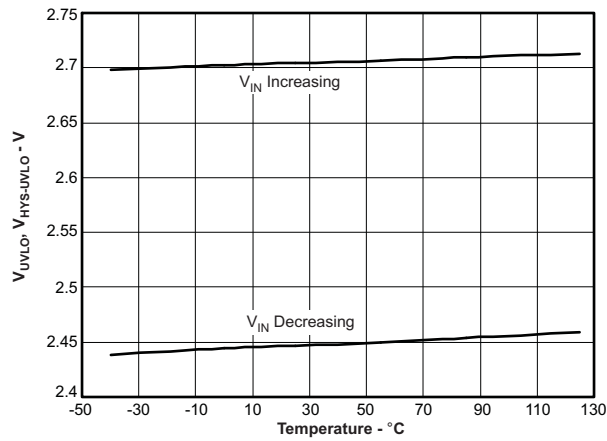**UNDERVOLTAGE LOCKOUT
vs
FREE-AIR TEMPERATURE**



**Figure 14.**
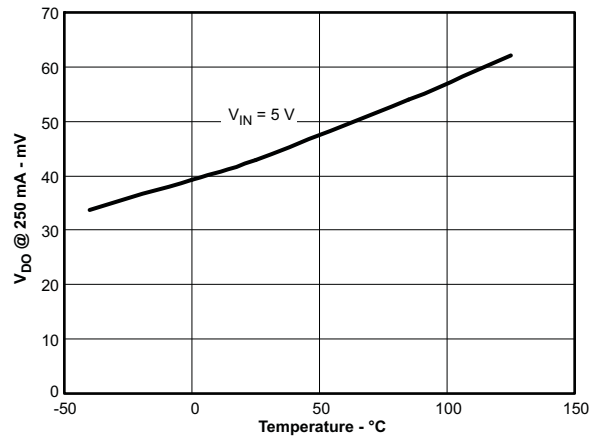
**DROPOUT VOLTAGE (IN to OUT)
vs
FREE-AIR TEMPERATURE**



**Figure 15.**

**REGULATION VOLTAGE (OUT pin)
vs
FREE-AIR TEMPERATURE**

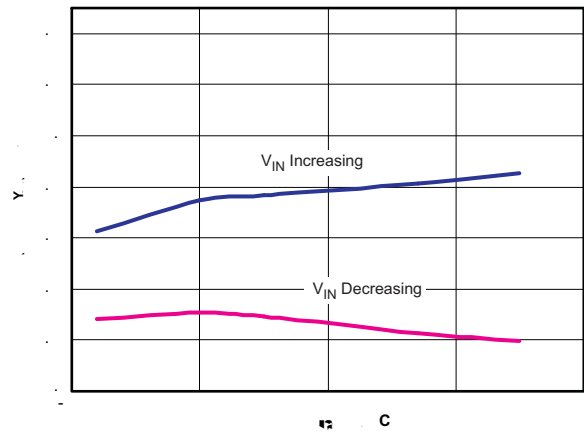**Figure 16.**

**OVP THRESHOLD
vs
FREE-AIR TEMPERATURE**



**Figure 17.**

Product Folder Link(s) : *bq24308*

## TYPICAL OPERATING PERFORMANCE (continued)
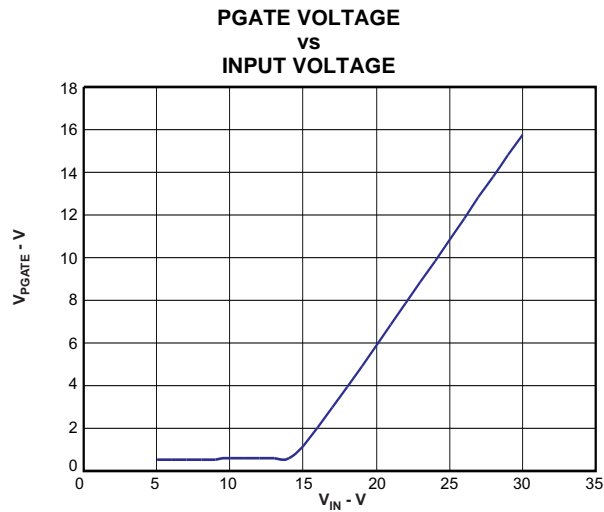
**PGATE VOLTAGE**
**vs**
**INPUT VOLTAGE**



**Figure 22.**

## DETAILED FUNCTIONAL DESCRIPTION

The bq24308 is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. In case of an input over-voltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an over-current condition, it limits the current to a safe value for a blanking duration before turning the switch off. Additionally, the IC also monitors its own die temperature and switches off if it becomes too hot.

The input and over-current threshold is user-programmable. The IC can be controlled by a processor using the CE pin.

## POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the IN under-voltage lockout threshold, VUVLO. The FET under-vol(se0 Td j ET of

**Thermal Protection**

If the junction temperature of the device exceeds $T_{J(OFF)}$, FET Q1 is turned off. The FET is turned back on when the junction temperature falls below $T_{J(OFF)} − T_{J(OFF-HYS)}$.

**Enable Function**

The IC has an enable pin which can be used to enable or disable the device. When the $\overline{CE}$ pin is driven high, the internal FET is turned off. When the $\overline{CE}$ pin is low, the FET is turned on if other conditions are safe. The $\overline{CE}$ pin has an internal pull-down resistor of 200 k    (typical) and can be left floating.
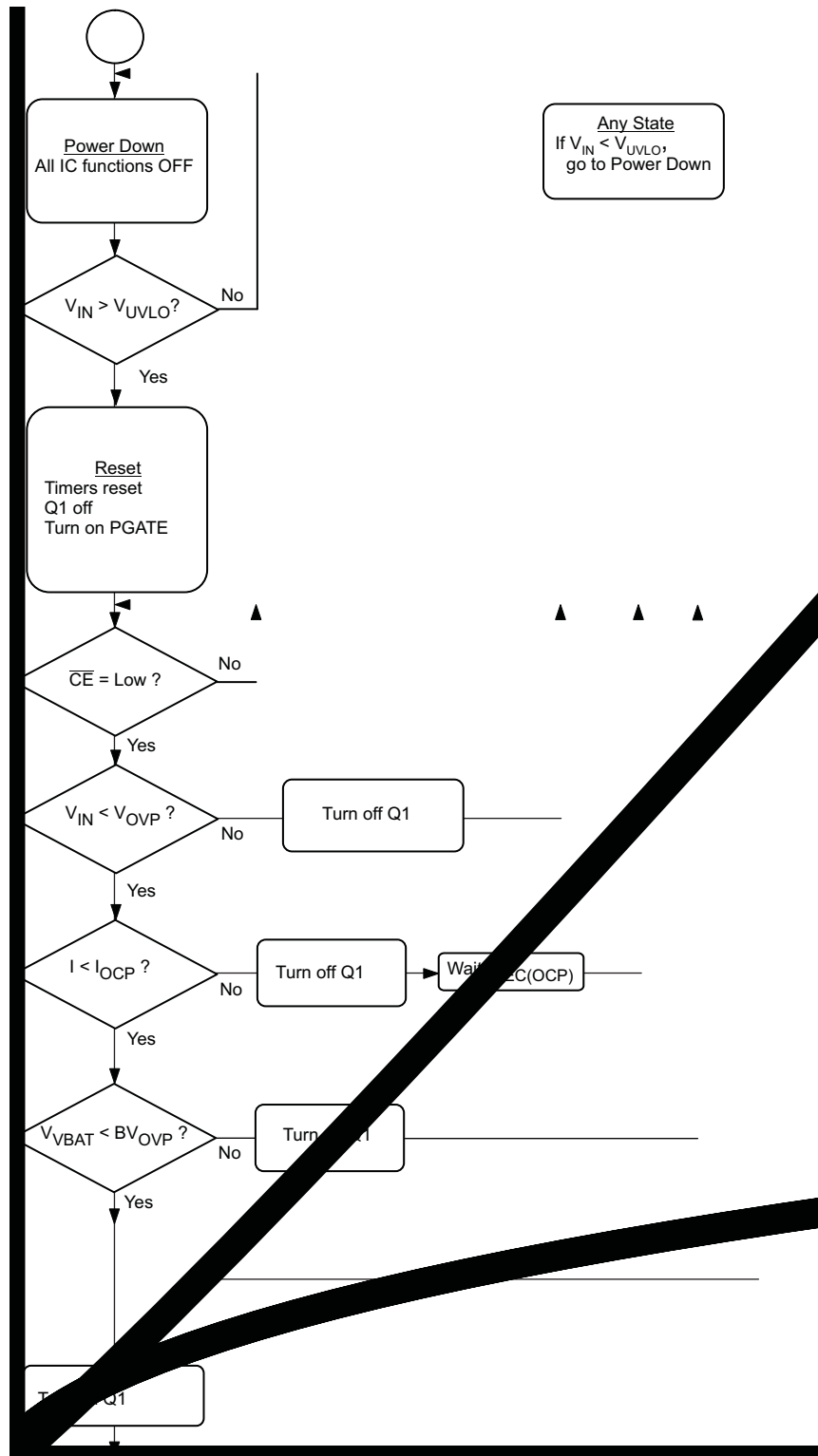
**Figure 23.  State Diagram**

# APPLICATION INFORMATION

## Selection of $R_{BAT}$:

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the device can be hazardous. Connecting the VBAT pin through $R_{BAT}$ prevents a large current from flowing into the battery in case of failure of the IC. In the interests of safety, $R_{BAT}$ should have a very high value. The problem with a large $R_{BAT}$ is that the voltage drop across this resistor because of the VBAT bias current $I_{VBAT}$ causes an error in the $BV_{OVP}$ threshold. This error is over and above the tolerance on the nominal 4.35V $BV_{OVP}$ threshold.

Choosing $R_{BAT}$ in the range 100K to 470k is a good compromise. In the case of IC failure, with $R_{BAT}$ equal to 100k, the maximum current flowing into the battery would be $(30V – 3V) \div 100k = 270 A$, which is low enough to be absorbed by the bias currents of the system components. $R_{BAT}$ equal to 100k would result in a worst-case voltage drop of $R_{BAT}$ X $I_{VBAT}$ 1mV. This is negligible compared to the internal tolerance of 50mV on the $BV_{OVP}$ threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

## Selection of $R_{CE}$:

The $\overline{CE}$ pin can be used to enable and disable the IC. If host control is not required, the $\overline{CE}$ pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the $\overline{CE}$ pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the $\overline{CE}$ pin should be connected to the host GPIO pin through a resistor as large as possible. The limitation on the resistor value is that the minimum $V_{OH}$ of the host GPIO pin less the drop across the resistor should be greater than $V_{IH}$ of the bq24308 $\overline{CE}$ pin. The drop across the resistor is given by $R_{CE}$ X $I_{IH}$.

## Selection of Input and Output Bypass Capacitors:

The input capacitor $C_{IN}$ in **Figure 1** and **Figure 2** is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up. $C_{IN}$ prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1 F be used at the input of the device. It should be located in close proximity to the IN pin.

$C_{OUT}$ in **Figure 1** and **Figure 2** is also important: If a very fast (< 1μs rise-time) overvoltage transient occurs at the input, the current that charges $C_{OUT}$ causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection. $C_{OUT}$ should also be a ceramic capacitor of at least 1μF, located close to the OUT pin. $C_{OUT}$ also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

## PCB Layout Guidelines:

1. This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for the maximum voltages expected to be seen in the system.
2. The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
3. $C_{IN}$ and $C_{OUT}$ should be located close to the IC. Other components like $R_{BAT}$ should also be located close to the IC.

## REVISION HISTORY

NOTE: Page numbers of current version may differ from previous versions.

**Changes from Original (September 2009) to Revision A**                                    **Page**

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| BQ24308DSGR | ACTIVE | WSON | DSG | 8 | 3000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |
| BQ24308DSGT | ACTIVE | WSON | DSG | 8 | 250 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-2-260C-1 YEAR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
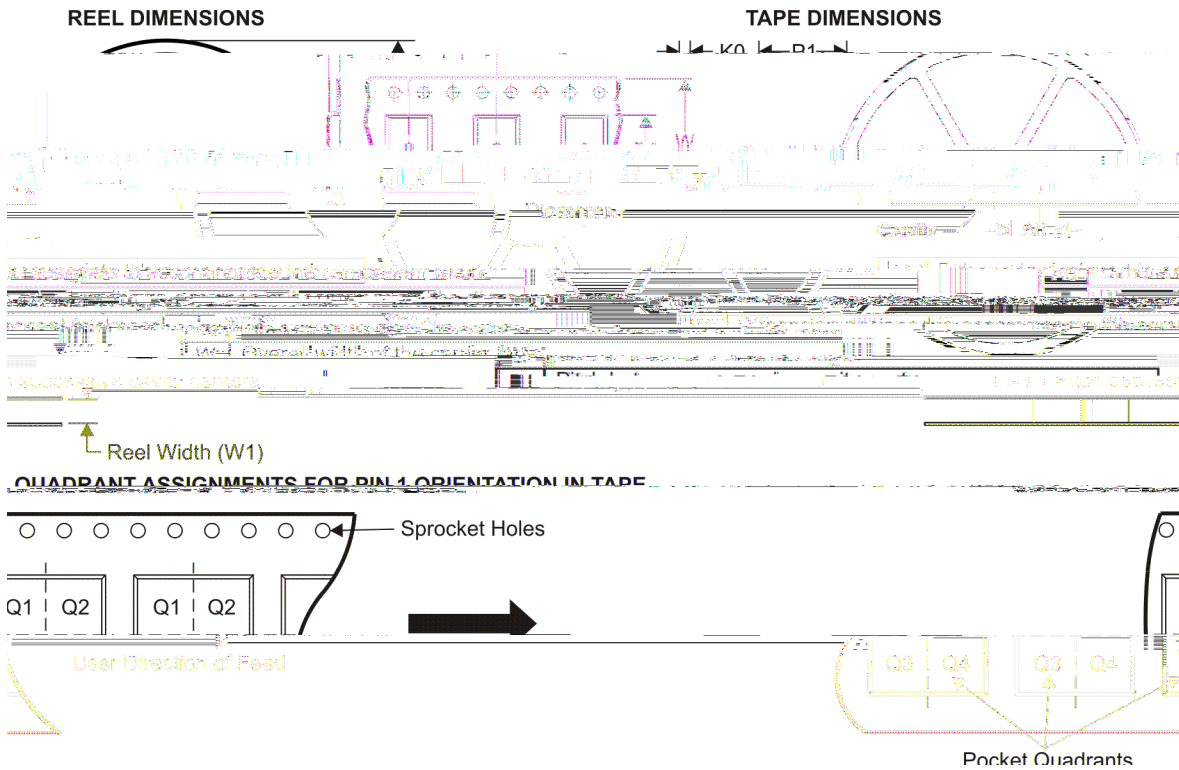**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

Reel Width (W1)

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

Sprocket Holes

| Q1 | Q2 | | Q1 | Q2 |

User Direction of Feed

| Q3 | Q4 | | Q3 | Q4 |

Pocket Quadrants

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ24308DSGR | WSON | DSG | 8 | 3000 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |
| BQ24308DSGT | WSON | DSG | 8 | 250 | 179.0 | 8.4 | 2.2 | 2.2 | 1.2 | 4.0 | 8.0 | Q2 |

# PACKAGE MATERIALS INFORMATION
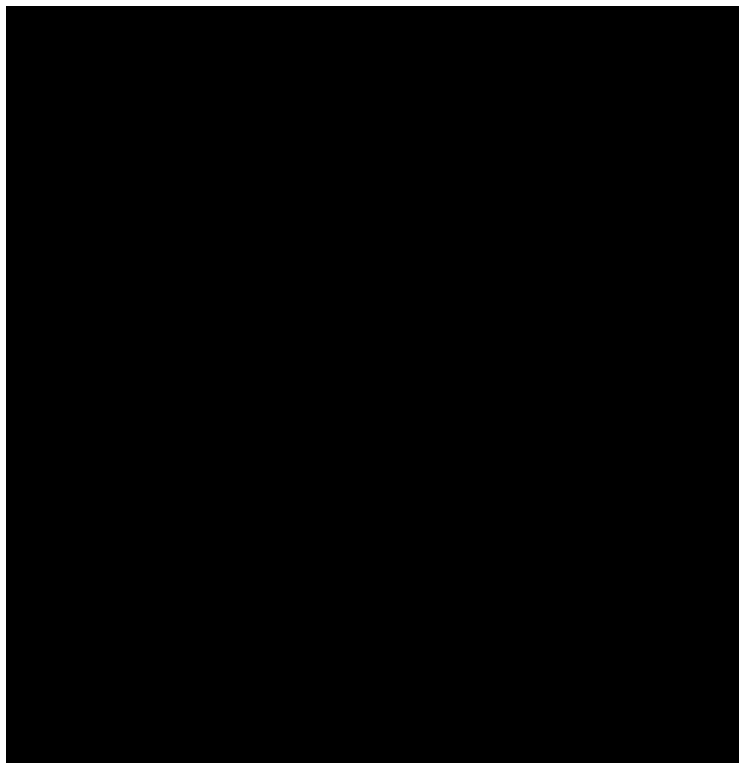


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ24308DSGR | WSON | DSG | 8 | 3000 | 195.0 | 200.0 | 45.0 |
| BQ24308DSGT | WSON | DSG | 8 | 250 | 195.0 | 200.0 | 45.0 |

1,0

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0,20 REF.

0,05

20

$\boxed{0,50}$

$\dfrac{0,30}{0,20}$
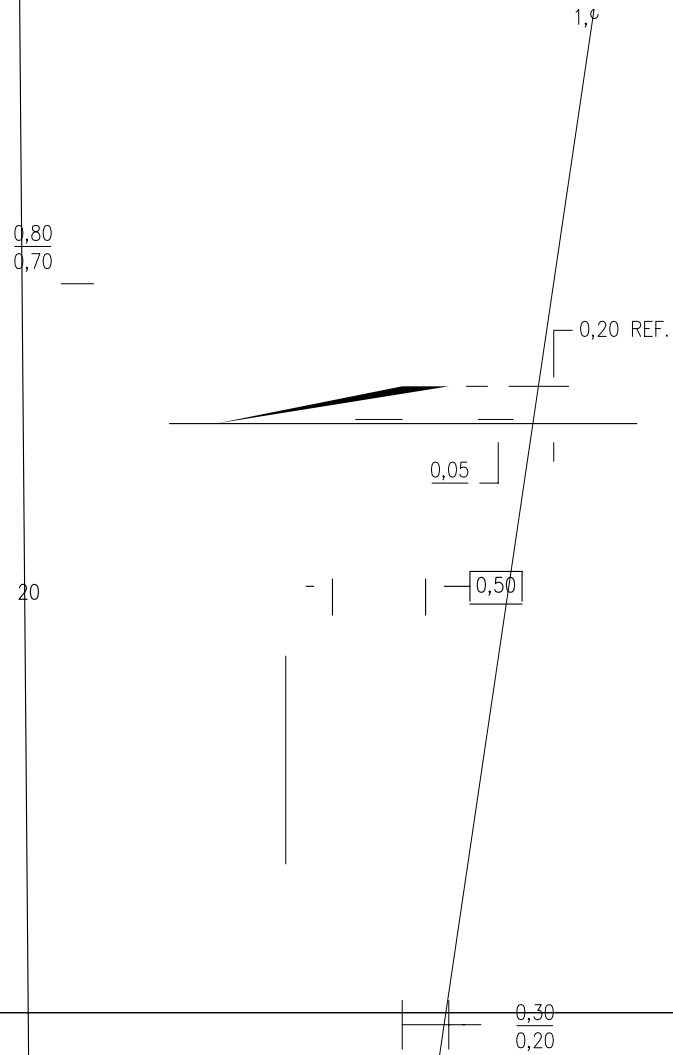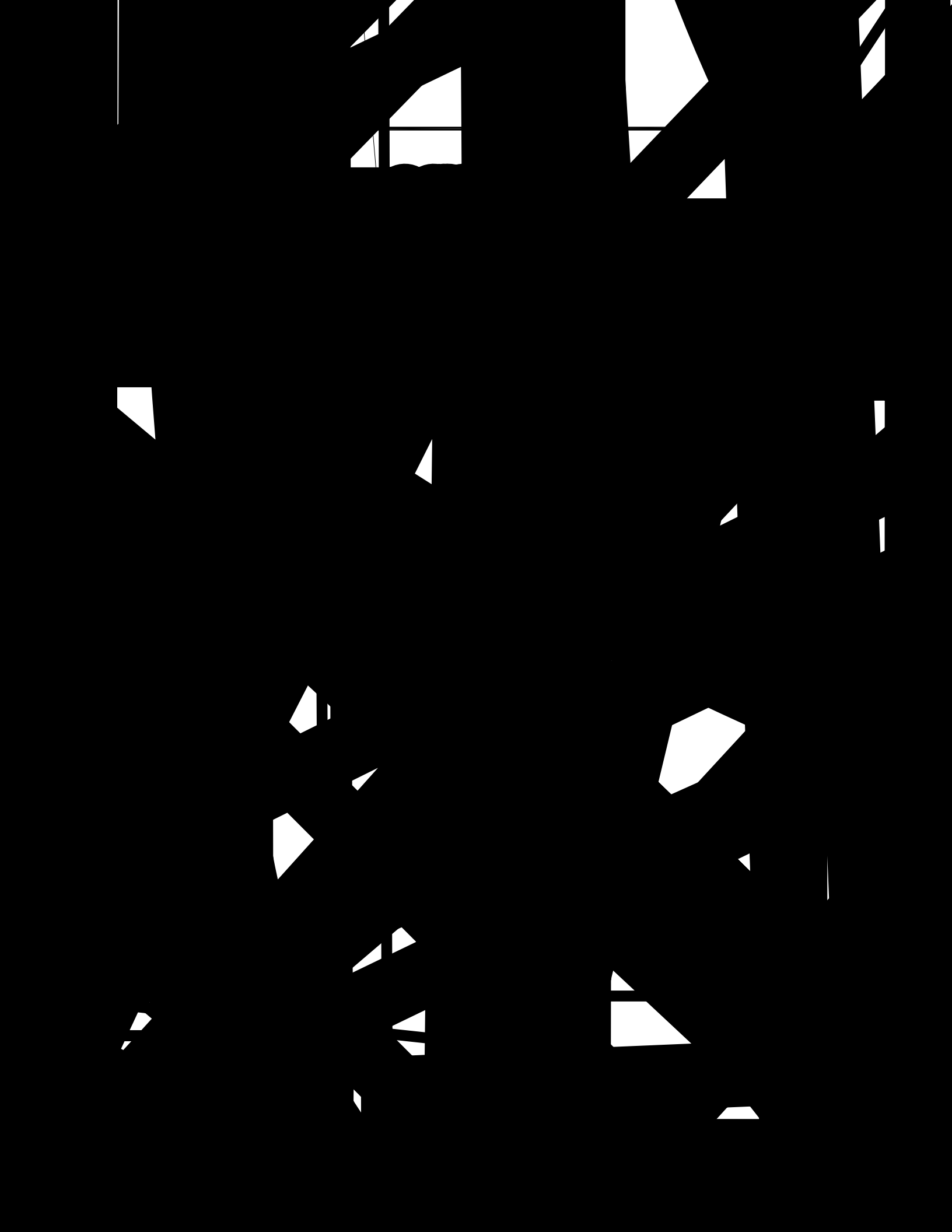
4208210/B 10/10

A.  All linear dimensions ar—
B.  This drawing is subject to change without notice.

thermal pad dimensions

E.  Fn

EXAS
RUMENTS
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**IMPORTANT NOTICE**