Dual, 300 mA Output, Adjustable, Low Noise, High PSRR Voltage Regulator

ADP223

FEATURES

- Input voltage range: 2.5 V to 5.5 V
- Dual, independent, 300 mA, adjustable low dropout voltage regulators
- Adjustable output voltage range, V_{OUT} = 0.5 V to 5 V
- Small, 8-lead, 2 mm × 2 mm LFCSP package
- Initial accuracy: ±1%
- Stable with 1 µF ceramic output capacitors
- Two independent logic controlled enables
- Outputs can be paralleled for higher output current
- Overcurrent and thermal protection
- High PSRR
  - 76 dB PSRR up to 1 kHz
  - 70 dB PSRR at 10 kHz
  - 60 dB PSRR at 100 kHz
  - 40 dB PSRR at 1 MHz
- Low output noise
  - 27 µV rms typical output noise at V_{OUT} = 1.2 V
  - 55 µV rms typical output noise at V_{OUT} = 2.8 V
- Excellent transient response
- Low dropout voltage: 120 mV at 300 mA load
- 65 µA typical ground current at no load, both LDOs enabled
- 100 µs fast turn-on circuit
- Guaranteed 300 mA output current per regulator
- –40°C to +125°C junction temperature

APPLICATIONS

- Wireless network equipment
- Point of sales equipment, barcode scanners, credit card readers
- Portable and battery-powered equipment
- Portable medical devices
- Post dc-to-dc regulation

TYPICAL APPLICATION CIRCUITS

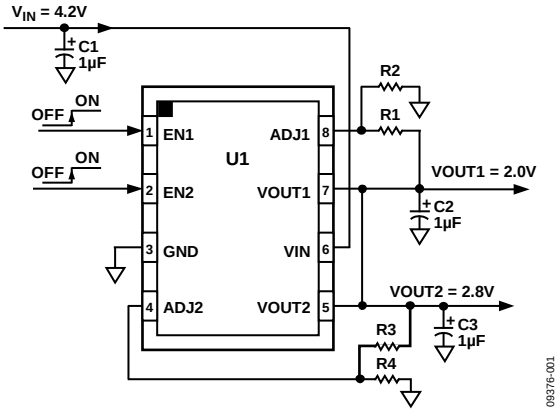

Figure 1. Dual Outputs

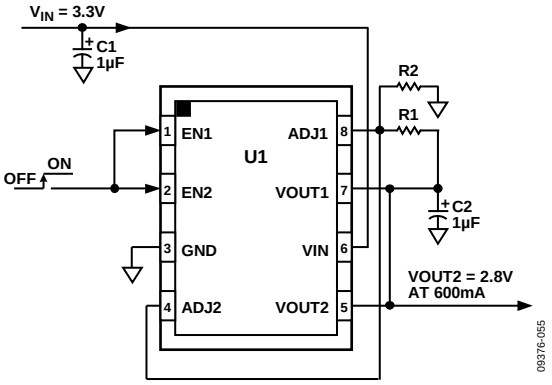

Figure 2. Paralleled Outputs for Increased Output Current

GENERAL DESCRIPTION

The 300 mA, dual adjustable output ADP223 combines high PSRR, low noise, low quiescent current, and low dropout voltage in a voltage regulator that is ideally suited for wireless applications with demanding performance and board space requirements.

The low quiescent current, low dropout voltage, and wide input voltage range of the ADP223 extend the battery life of portable devices. The ADP223 maintains power supply rejection greater than 60 dB for frequencies as high as 100 kHz while operating with a low headroom voltage. The ADP223 offers much lower noise performance than competing LDOs without the need for a noise bypass capacitor.

The ADP223 is available in a small, 8-lead, 2 mm × 2 mm LFCSP package and is stable with tiny, 1 µF, ±30% ceramic output capacitors, resulting in the smallest possible board area for a wide variety of portable power needs.

Overcurrent and thermal protection prevent damage in adverse conditions.

Rev. 0

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REVISION HISTORY

4/11—Revision 0: Initial Version

SPECIFICATIONS

V_{IN} = (V_{OUT} + 0.5 V) or 2.5 V (whichever is greater), EN1 = EN2 = V_{IN}, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = C_{OUT1} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT VOLTAGE RANGE	V_{IN}	T_J = −40°C to +125°C	2.5		5.5	V
OPERATING SUPPLY CURRENT WITH BOTH REGULATORS ON	I_{GND}	I_{OUT} = 0 µA		65		µA
		I_{OUT} = 0 µA, T_J = −40°C to +125°C			120	µA
		I_{OUT} = 10 mA		90		µA
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			150	µA
		I_{OUT} = 300 mA		180		µA
		I_{OUT} = 300 mA, T_J = −40°C to +125°C			300	µA
SHUTDOWN CURRENT	I_{GND-SD}	EN1 = EN2 = GND		0.1	1.5	µA
ADJUSTABLE OUTPUT VOLTAGE ACCURACY[1]	V_{ADJ}	I_{OUT} = 10 mA	0.495	0.500	0.505	V
		0 µA < I_{OUT} < 300 mA, V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	0.490		0.510	V
LINE REGULATION	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V		0.01		%/V
		V_{IN} = (V_{OUT} + 0.5 V) to 5.5 V, T_J = −40°C to +125°C	−0.05		+0.05	%/V
LOAD REGULATION[2]	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 1 mA to 300 mA		0.001		%/mA
		I_{OUT} = 1 mA to 300 mA, T_J = −40°C to +125°C			0.004	%/mA
DROPOUT VOLTAGE[3]	$V_{DROPOUT}$	V_{OUT} = 3.3 V				
		I_{OUT} = 10 mA		4		mV
		I_{OUT} = 10 mA, T_J = −40°C to +125°C			8	mV
		I_{OUT} = 300 mA		120		mV
		I_{OUT} = 300 mA, T_J = −40°C to +125°C			240	mV
ADJx INPUT BIAS CURRENT	ADJ_{I-BIAS}	2.5 V ≤ V_{IN} ≤ 5.5 V, ADJx connected to VOUTx		10		nA
START-UP TIME[4]	$t_{START-UP}$	V_{OUT} = 3.3 V		240		µs
		V_{OUT} = 0.8 V		100		µs
CURRENT-LIMIT THRESHOLD[5]	I_{LIMIT}		340	440	650	mA
THERMAL SHUTDOWN						
Thermal Shutdown Threshold	TS_{SD}	T_J rising		155		°C
Thermal Shutdown Hysteresis	TS_{SD-HYS}			15		°C
ENx INPUT						
ENx Input Logic High	V_{IH}	2.5 V ≤ V_{IN} ≤ 5.5 V	1.2			V
ENx Input Logic Low	V_{IL}	2.5 V ≤ V_{IN} ≤ 5.5 V			0.4	V
ENx Input Leakage Current	$V_{I-LEAKAGE}$	EN1 = EN2 = V_{IN} or GND		0.01		µA
		EN1 = EN2 = V_{IN} or GND, T_J = −40°C to +125°C			1	µA
UNDERVOLTAGE LOCKOUT	UVLO					
Input Voltage Rising	$UVLO_{RISE}$				2.45	V
Input Voltage Falling	$UVLO_{FALL}$		2.0			V
Hysteresis	$UVLO_{HYS}$			180		mV
OUTPUT NOISE	OUT_{NOISE}	10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 3.3 V		62		µV rms
		10 Hz to 100 kHz, V_{IN} = 5 V, V_{OUT} = 2.8 V		55		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 2.5 V		50		µV rms
		10 Hz to 100 kHz, V_{IN} = 3.6 V, V_{OUT} = 1.2 V		27		µV rms

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLY REJECTION RATIO	PSRR	V_{IN} = 2.5 V, V_{OUT} = 0.8 V, I_{OUT} = 100 mA				
		100 Hz		76		dB
		1 kHz		76		dB
		10 kHz		70		dB
		100 kHz		60		dB
		1 MHz		40		dB
		V_{IN} = 3.8 V, V_{OUT} = 2.8 V, I_{OUT} = 100 mA				
		100 Hz		68		dB
		1 kHz		68		dB
		10 kHz		68		dB
		100 kHz		60		dB
		1 MHz		40		dB

[1] Accuracy when VOUTx is connected directly to ADJx. When the VOUTx voltage is set by external feedback resistors, the absolute accuracy in adjust mode depends on the tolerances of the resistors used.
[2] Based on an endpoint calculation using 1 mA and 300 mA loads.
[3] Dropout voltage is defined as the input-to-output voltage differential when the input voltage is set to the nominal output voltage. This applies only for output voltages above 2.5 V.
[4] Start-up time is defined as the time between the rising edge of EN to V_{OUT} being at 90% of its nominal value.
[5] Current-limit threshold is defined as the current at which the output voltage drops to 90% of the specified typical value. For example, the current limit for a 3.0 V output voltage is defined as the current that causes the output voltage to drop to 90% of 3.0 V, or 2.7 V.

INPUT AND OUTPUT CAPACITOR, RECOMMENDED SPECIFICATIONS

The minimum input and output capacitance should be greater than 0.70 µF over the full range of operating conditions. The full range of operating conditions in the application must be considered during capacitor selection to ensure that the minimum capacitance specification is met. X7R and X5R type capacitors are recommended for use with the LDOs, whereas Y5V and Z5U type capacitors are not recommended for use with the LDOs.

Table 2.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
MINIMUM INPUT AND OUTPUT CAPACITANCE	C_{MIN}	T_A = −40°C to +125°C	0.70			µF
CAPACITOR ESR	R_{ESR}	T_A = −40°C to +125°C	0.001		1	Ω

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VIN to GND	−0.3 V to +6.5 V
ADJ1, ADJ2, VOUT1, VOUT2 to GND	−0.3 V to VIN
EN1, EN2 to GND	−0.3 V to +6.5 V
Storage Temperature Range	−65°C to +150°C
Operating Junction Temperature Range	−40°C to +125°C
Soldering Conditions	JEDEC J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Absolute maximum ratings apply individually only, not in combination.

THERMAL DATA

The ADP223 can be damaged when the junction temperature (T_J) limits are exceeded. Monitoring ambient temperature does not guarantee that T_J is within the specified temperature limits. In applications with high power dissipation and poor PCB thermal resistance, the maximum ambient temperature may need to be derated. In applications with moderate power dissipation and low PCB thermal resistance, the maximum ambient temperature can exceed the maximum limit as long as the junction temperature is within specification limits.

The T_J of the device is dependent on the ambient temperature (T_A), the power dissipation of the device (P_D), and the junction-to-ambient thermal resistance of the package (θ_{JA}). Maximum junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) using the formula

$$T_J = T_A + (P_D \times \theta_{JA})$$

The junction-to-ambient thermal resistance (θ_{JA}) of the package is based on modeling and calculation using a 4-layer board. θ_{JA} is highly dependent on the application and board layout. In applications where high maximum power dissipation exists, close attention to thermal board design is required.

The value of θ_{JA} may vary, depending on PCB material, layout, and environmental conditions. The specified value of θ_{JA} is based on a 4-layer, 4 inch × 3 inch 2½ oz. copper board, as per JEDEC standards. For more information, see the AN-772 Application Note, *A Design and Manufacturing Guide for the Lead Frame Chip Scale Package (LFCSP)*.

Ψ_{JB} is the junction-to-board thermal characterization parameter with units of °C/W. Ψ_{JB} of the package is based on modeling and calculation using a 4-layer board. The JEDEC JESD51-12 document, *Guidelines for Reporting and Using Electronic Package Thermal Information*, states that thermal characterization parameters are not the same as thermal resistances. Ψ_{JB} measures the component power flowing through multiple thermal paths rather than through a single path, as in thermal resistance, θ_{JB}. Therefore, Ψ_{JB} thermal paths include convection from the top of the package as well as radiation from the package, factors that make Ψ_{JB} more useful in real-world applications. Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the formula

$$T_J = T_B + (P_D \times \Psi_{JB})$$

Refer to the JEDEC JESD51-8 and JESD51-12 documents for more detailed information about Ψ_{JB}.

THERMAL RESISTANCE

θ_{JA} and Ψ_{JB} are specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 4. Thermal Resistance

Package Type	θ_{JA}	Ψ_{JB}	Unit
8-Lead, 2 mm × 2 mm LFCSP	50.2	18.2	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

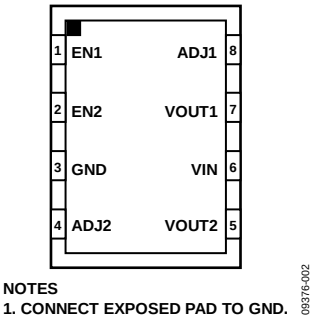

Figure 3. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	EN1	Enable Input for the First Regulator. Drive EN1 high to turn on Regulator 1, and drive EN1 low to turn off Regulator 1. For automatic startup, connect EN1 to VIN.
2	EN2	Enable Input for the Second Regulator. Drive EN2 high to turn on Regulator 2, and drive EN2 low to turn off Regulator 2. For automatic startup, connect EN2 to VIN.
3	GND	Ground Pin.
4	ADJ2	Adjust Pin for VOUT2. A resistor divider from VOUT2 to ADJ2 sets the output voltage.
5	VOUT2	Regulated Output Voltage. Connect a 1 µF or greater output capacitor between VOUT2 and GND.
6	VIN	Regulator Input Supply. Bypass VIN to GND with a 1 µF or greater capacitor.
7	VOUT1	Regulated Output Voltage. Connect a 1 µF or greater output capacitor between VOUT1 and GND.
8	ADJ1	Adjust Pin for VOUT1. A resistor divider from VOUT1 to ADJ1 sets the output voltage.
	EPAD	The exposed paddle must be connected to ground.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 5 V, V_{OUT1} = 3.3 V, V_{OUT2} = 2.8 V, I_{OUT1} = I_{OUT2} = 10 mA, C_{IN} = C_{OUT1} = C_{OUT2} = 1 µF, T_A = 25°C, unless otherwise noted.

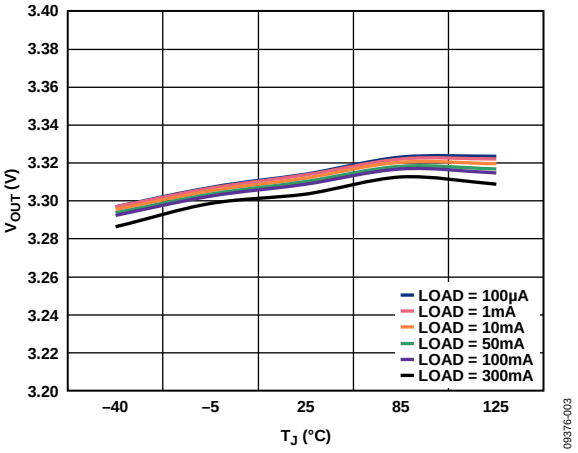

Figure 4. Output Voltage vs. Junction Temperature, V_{OUT} = 3.3 V

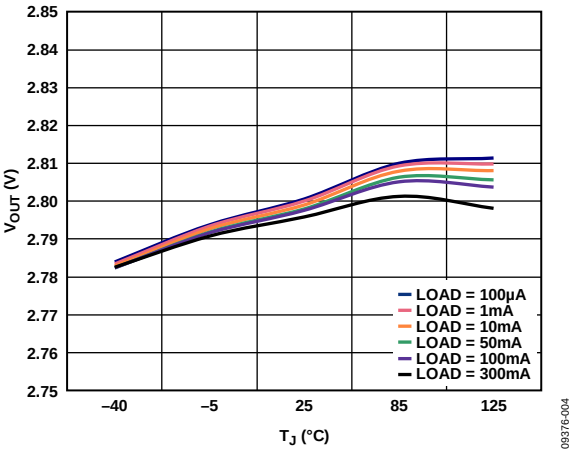

Figure 5. Output Voltage vs. Junction Temperature, V_{OUT} = 2.8 V

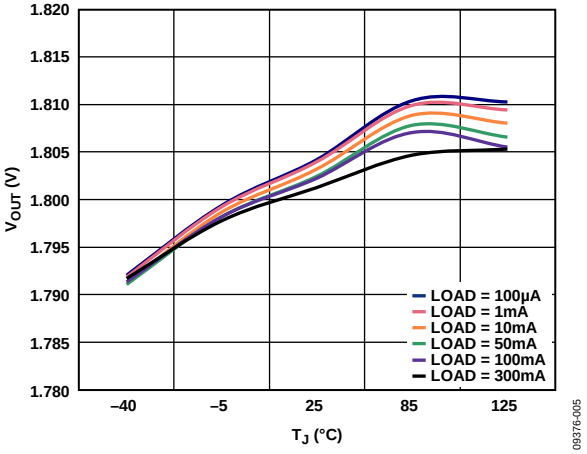

Figure 6. Output Voltage vs. Junction Temperature, V_{OUT} = 1.8 V

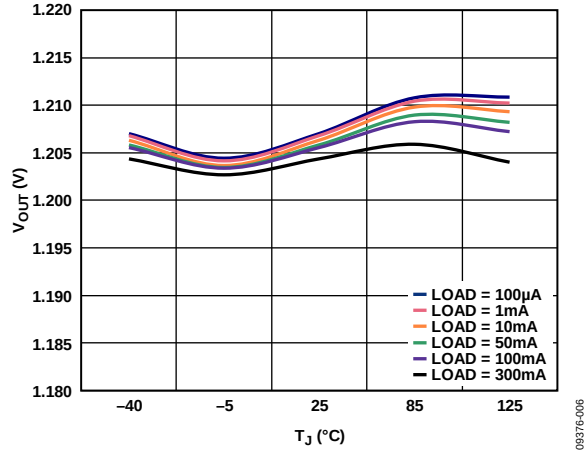

Figure 7. Output Voltage vs. Junction Temperature, V_{OUT} = 1.2 V

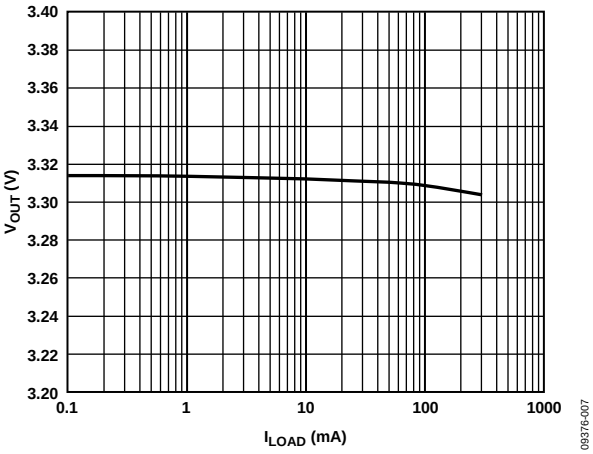

Figure 8. Output Voltage vs. Load Current, V_{OUT} = 3.3 V

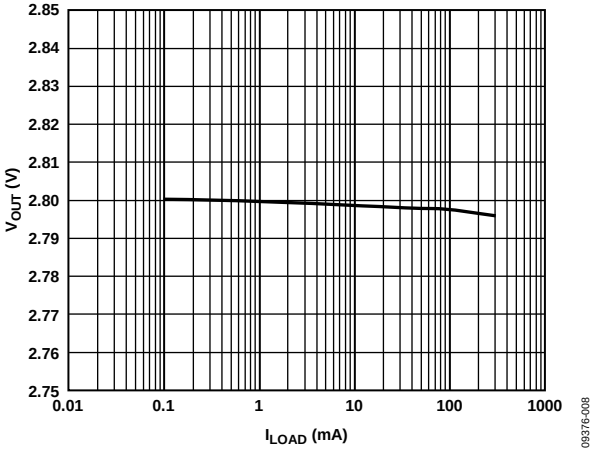

Figure 9. Output Voltage vs. Load Current, V_{OUT} = 2.8 V

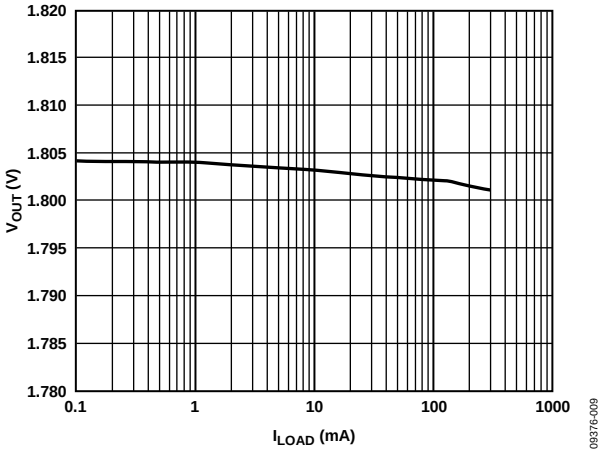

Figure 10. Output Voltage vs. Load Current, V_{OUT} = 1.8 V

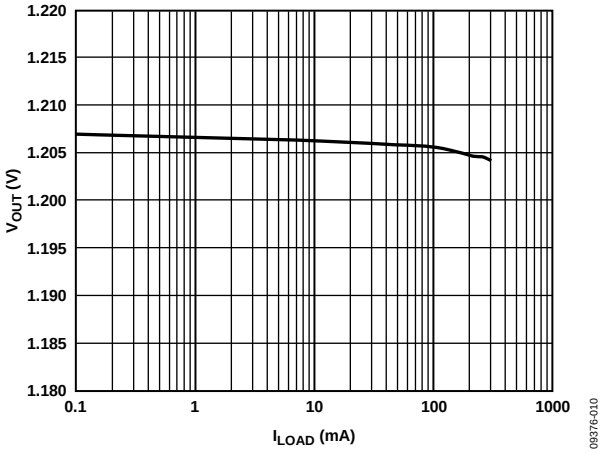

Figure 11. Output Voltage vs. Load Current, V_{OUT} = 1.2 V

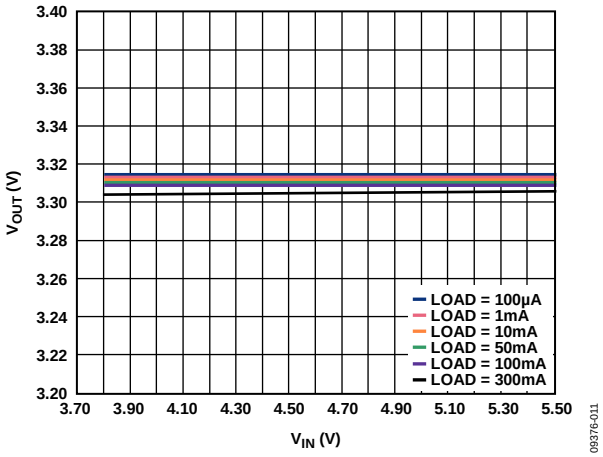

Figure 12. Output Voltage vs. Input Voltage, V_{OUT} = 3.3 V

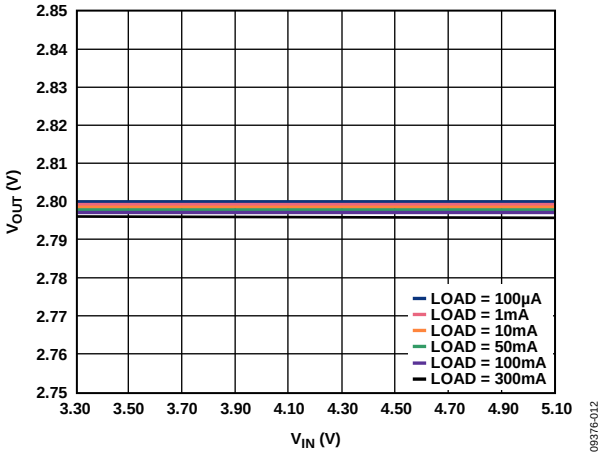

Figure 13. Output Voltage vs. Input Voltage, V_{OUT} = 2.8 V

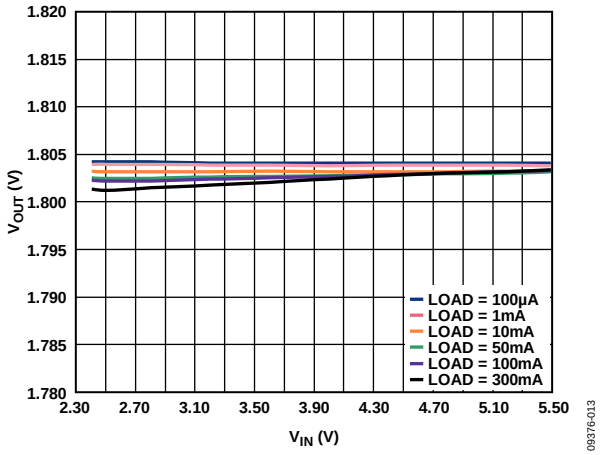

Figure 14. Output Voltage vs. Input Voltage, V_{OUT} = 1.8 V

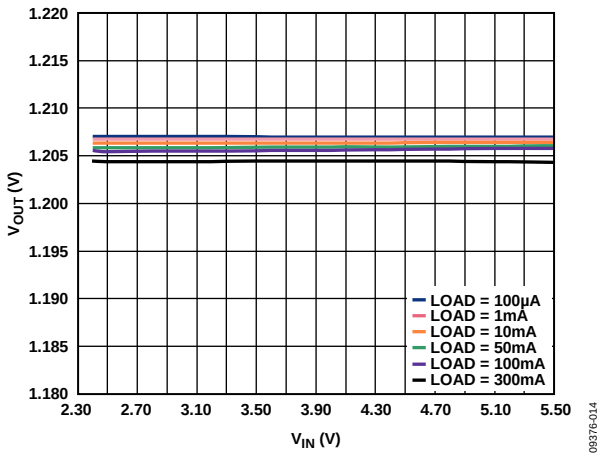

Figure 15. Output Voltage vs. Input Voltage, V_{OUT} = 1.2 V

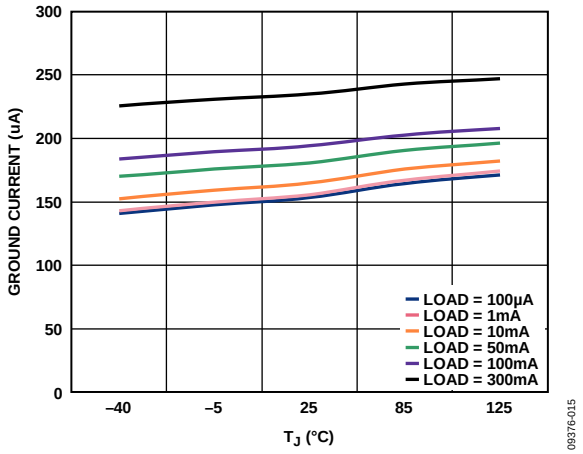

Figure 16. Ground Current vs. Junction Temperature, Single Output, Includes 100 µA for Output Divider

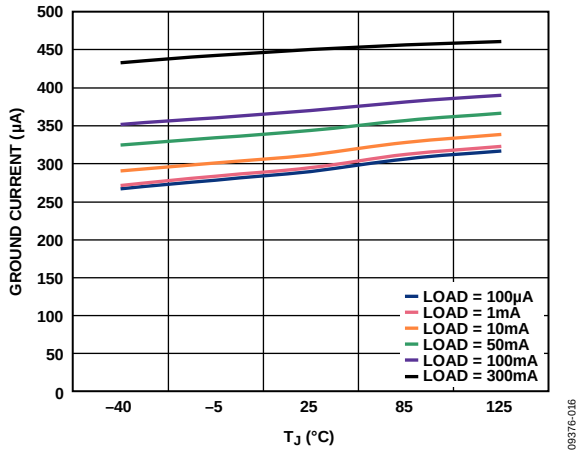

Figure 17. Ground Current vs. Junction Temperature, Dual Output, Includes 200 µA for Output Dividers

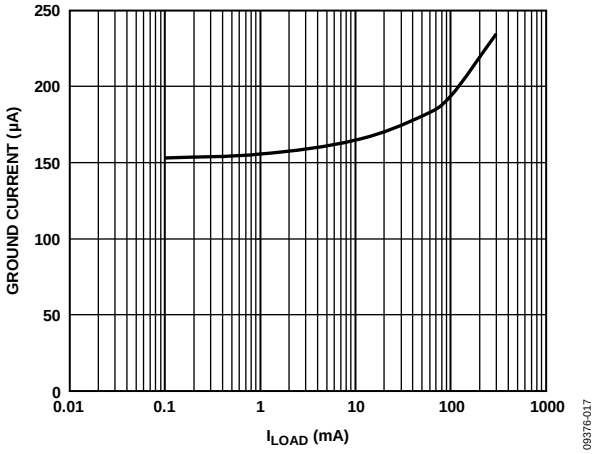

Figure 18. Ground Current vs. Load Current, Single Output, Includes 100 µA for Output Divider

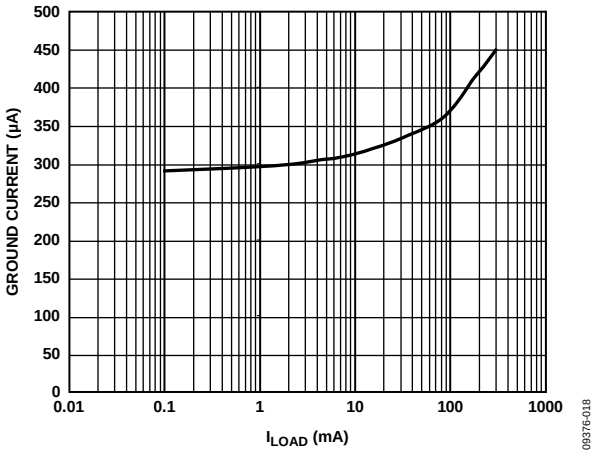

Figure 19. Ground Current vs. Load Current, Dual Output, Includes 200 µA for Output Dividers

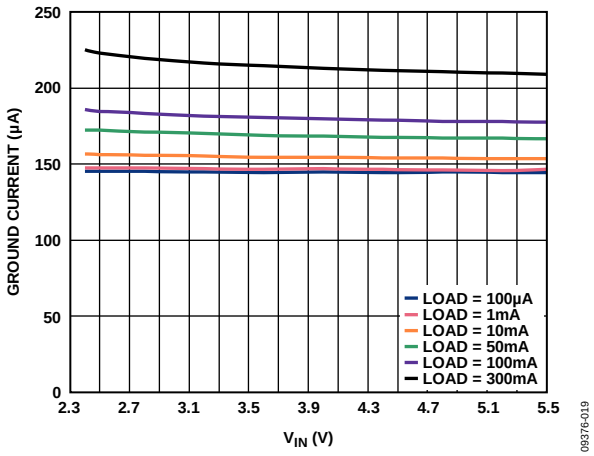

Figure 20. Ground Current vs. Input Voltage, V_{OUT} = 1.2 V, Single Output, Includes 100 µA for Output Divider

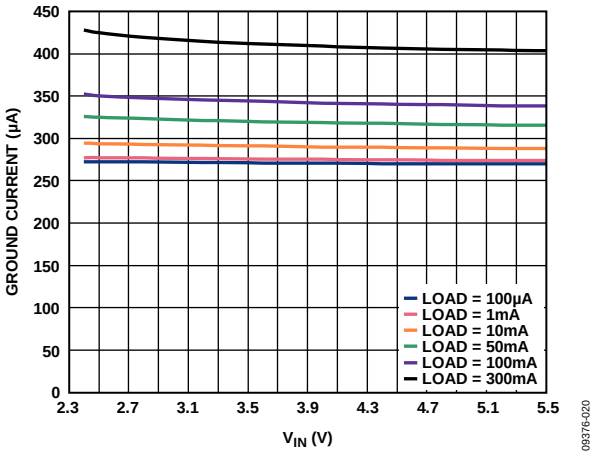

Figure 21. Ground Current vs. Input Voltage, V_{OUT} = 1.2 V and 1.8 V, Dual Output, Includes 200 µA for Output Dividers

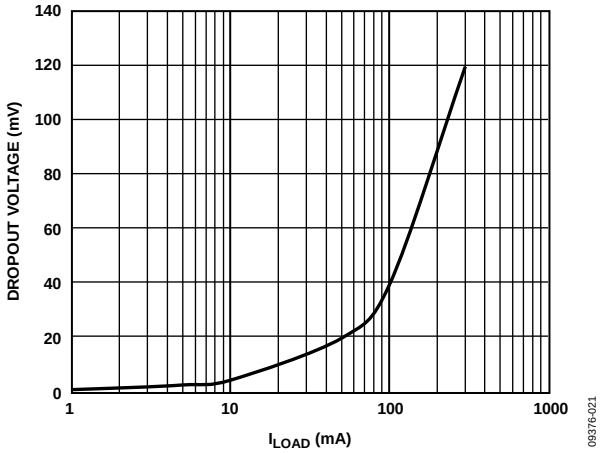

Figure 22. Dropout Voltage vs. Load Current, V_{OUT} = 3.3 V

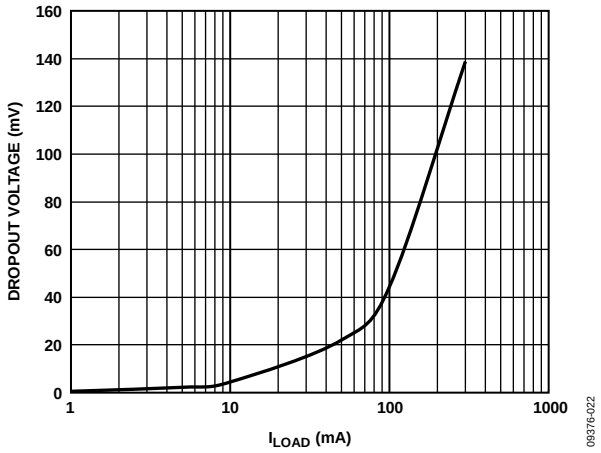

Figure 23. Dropout Voltage vs. Load Current, V_{OUT} = 2.8 V

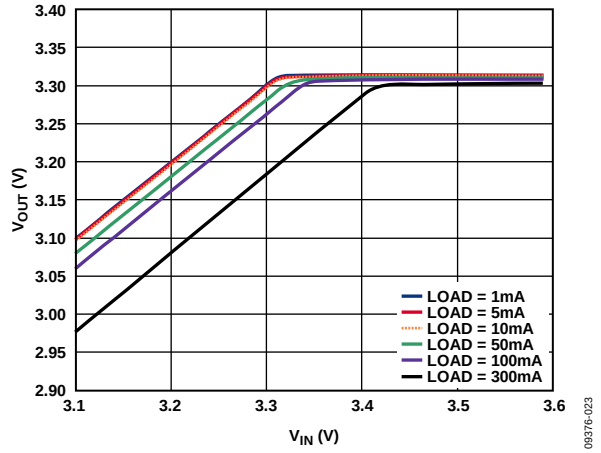

Figure 24. Output Voltage vs. Input Voltage in Dropout, V_{OUT} = 3.3 V

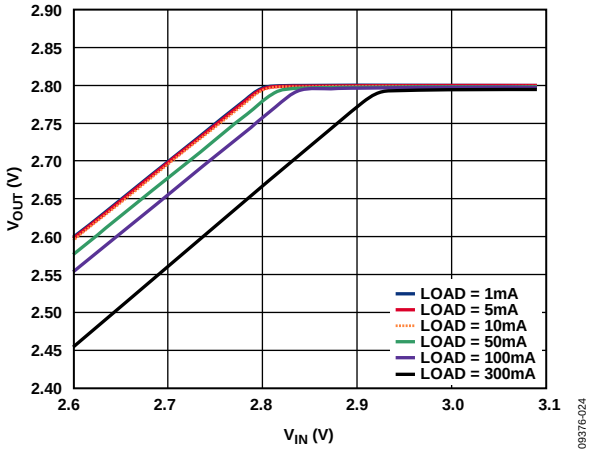

Figure 25. Output Voltage vs. Input Voltage in Dropout, V_{OUT} = 2.8 V

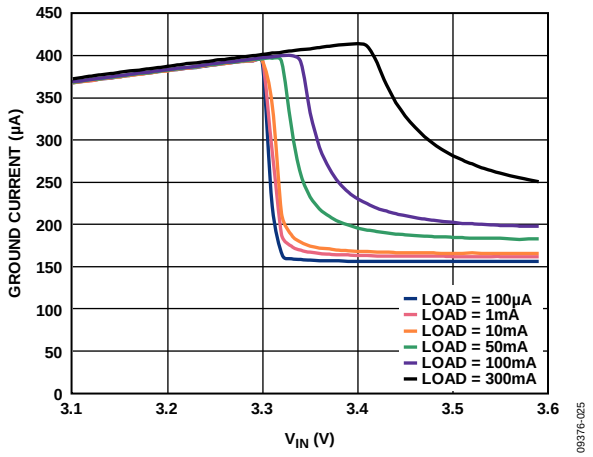

Figure 26. Ground Current vs. Input Voltage in Dropout, V_{OUT} = 3.3 V

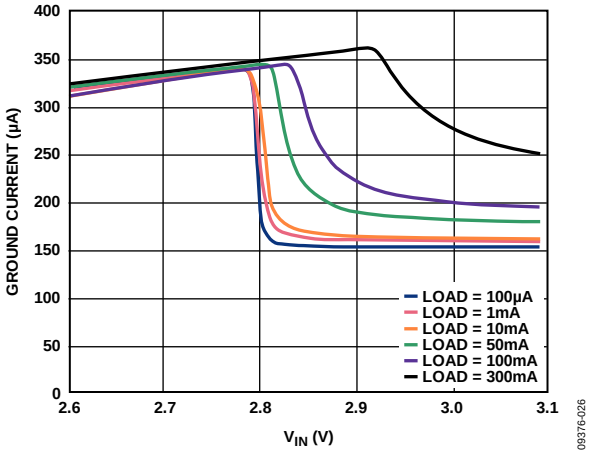

Figure 27. Ground Current vs. Input Voltage in Dropout, V_{OUT} = 2.8 V

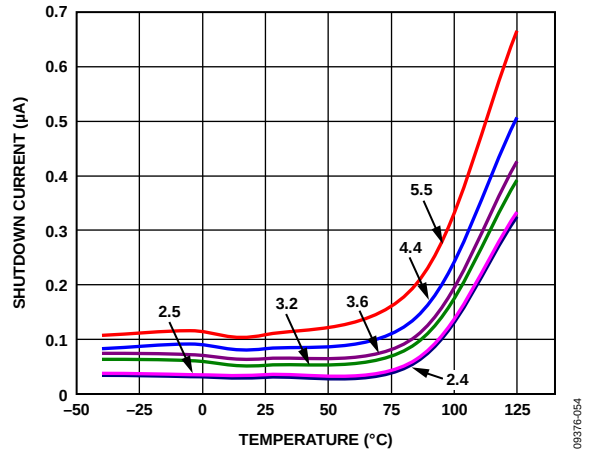

Figure 28. Shutdown Ground Current vs. Temperature, Different Input Voltages

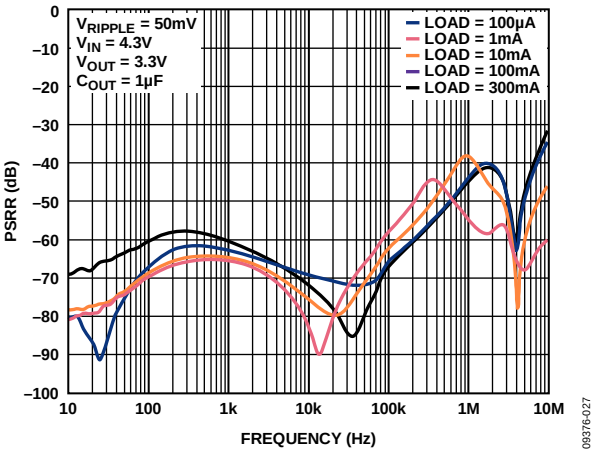

Figure 29. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 4.3 V, V_{OUT} = 3.3 V

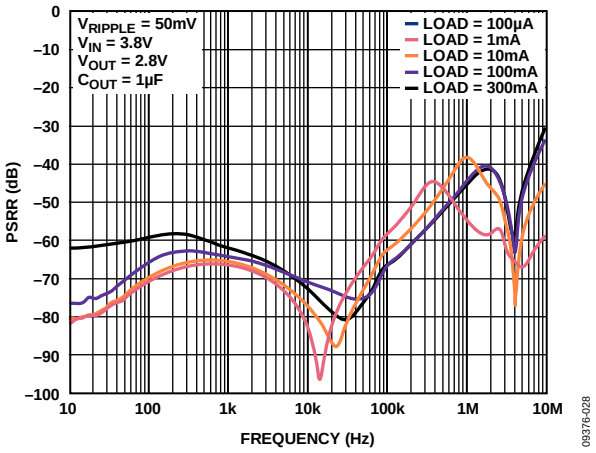

Figure 30. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 3.8 V, V_{OUT} = 2.8 V

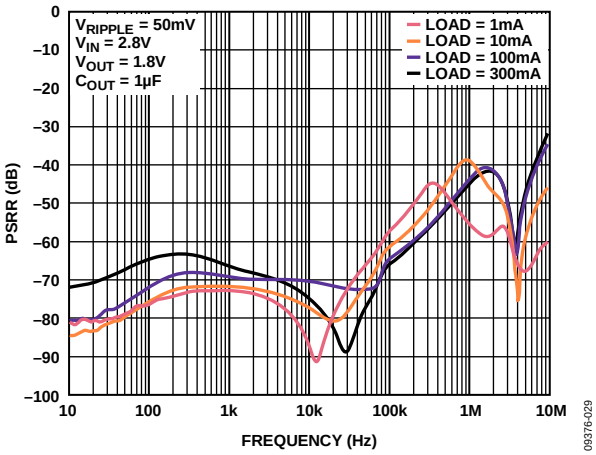

Figure 31. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 2.8 V, V_{OUT} = 1.8 V

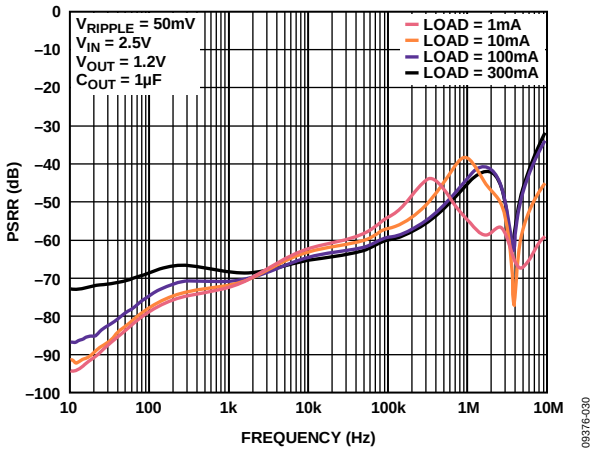

Figure 32. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 2.5 V, V_{OUT} = 1.2 V

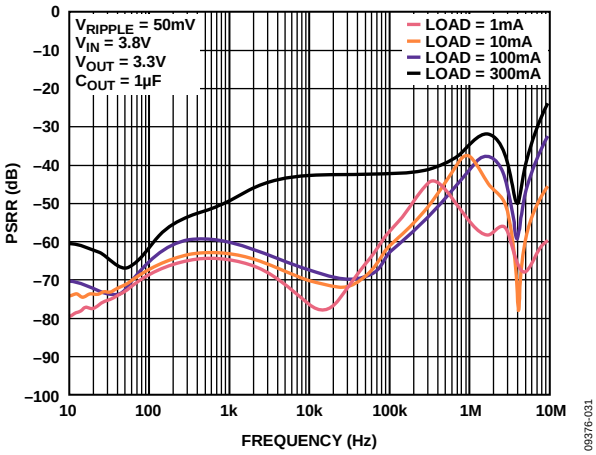

Figure 33. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 3.8 V, V_{OUT} = 3.3 V

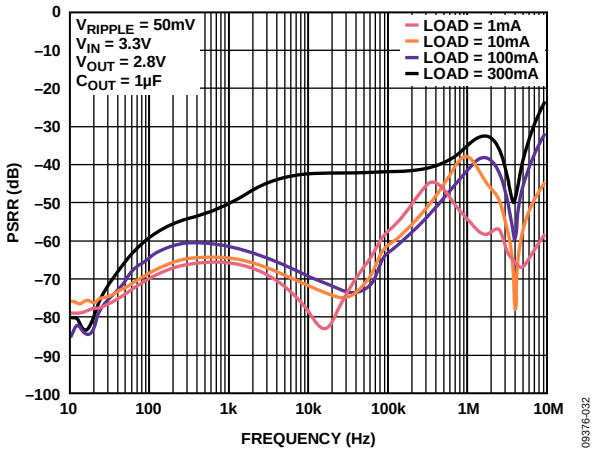

Figure 34. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 3.3 V, V_{OUT} = 2.8 V

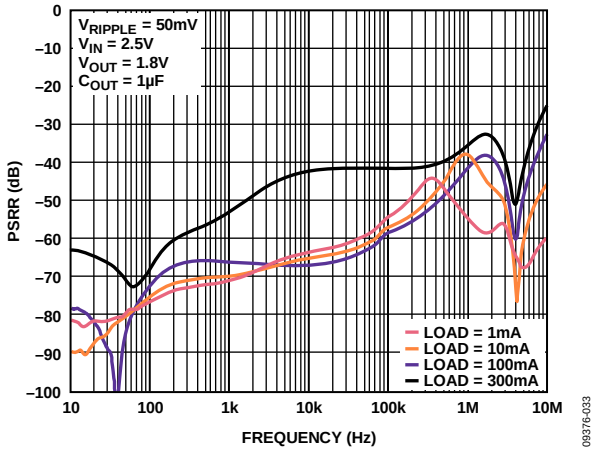

Figure 35. Power Supply Rejection Ratio vs. Frequency, V_{IN} = 2.5 V, V_{OUT} = 1.8 V

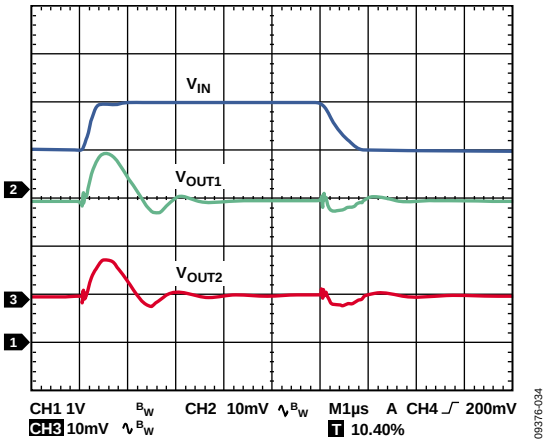

Figure 36. Transient Line Response, V_{OUT} = 3.3 V and 2.8 V, V_{IN} = 4 V to 5 V, I_{LOAD} = 10 mA

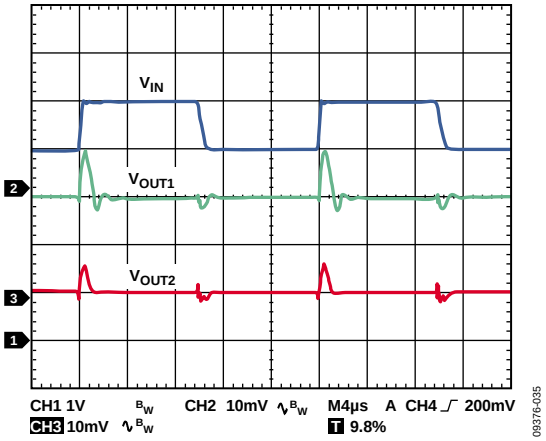

Figure 37. Transient Line Response, V_{OUT} = 1.2 V and 1.8 V, V_{IN} = 4 V to 5 V, I_{LOAD} = 10 mA

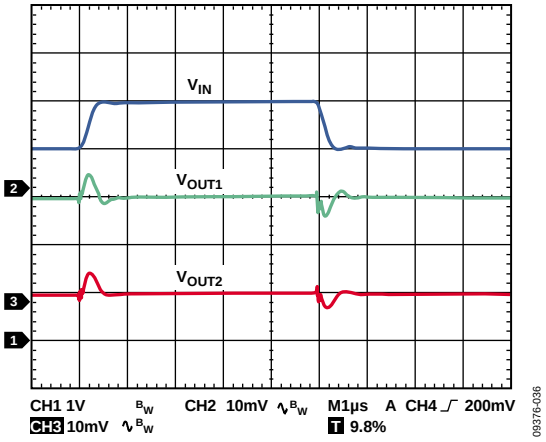

Figure 38. Transient Line Response, V_{OUT} = 3.3 V and 2.8 V, V_{IN} = 4 V to 5 V, I_{LOAD} = 300 mA

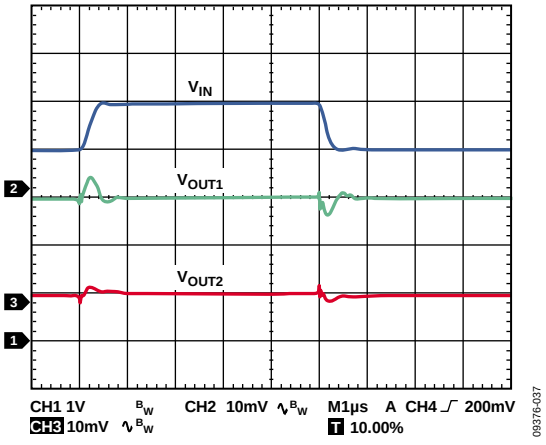

Figure 39. Transient Line Response, V_{OUT} = 1.2 V and 1.8 V, V_{IN} = 4 V to 5 V, I_{LOAD} = 300 mA

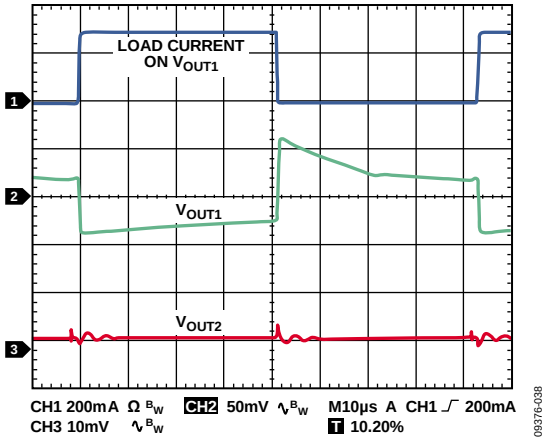

Figure 40. Transient Load Response, V_{OUT1} = 3.3 V, I_{LOAD} = 1 mA to 300 mA, V_{OUT2} = 2.8 V, I_{LOAD} = 1 mA

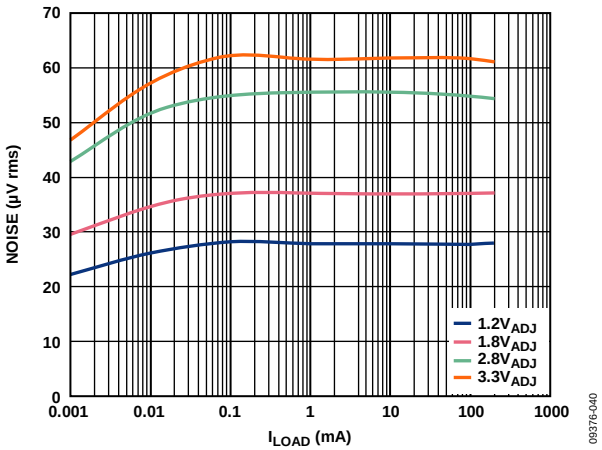

Figure 42. RMS Output Noise vs. Load Current and Output Voltage, V_{IN} = 5 V, C_{OUT} = 1 µF

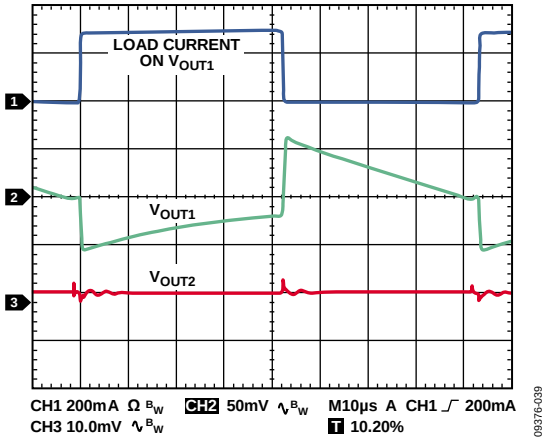

Figure 41. Transient Load Response, V_{OUT1} = 1.2 V, I_{LOAD} = 1 mA to 300 mA, V_{OUT2} = 1.8 V, I_{LOAD} = 1 mA

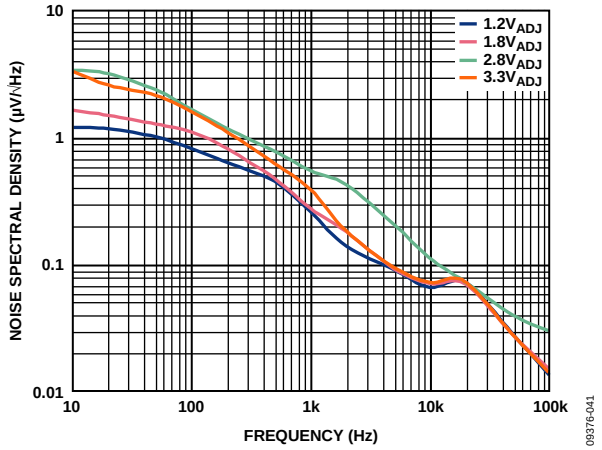

Figure 43. Output Noise Spectral Density, V_{IN} = 5 V, I_{LOAD} = 10 mA, C_{OUT} = 1 µF

THEORY OF OPERATION

The ADP223 is a low quiescent current, adjustable dual output, low dropout linear regulator that operates from 2.5 V to 5.5 V and provides up to 300 mA of current from each output. Drawing a low 300 μA quiescent current (typical) at full load makes the ADP223 ideal for battery-operated portable equipment. Shutdown current consumption is typically 100 nA.

Optimized for use with small 1 μF ceramic capacitors, the ADP223 provides excellent transient performance.

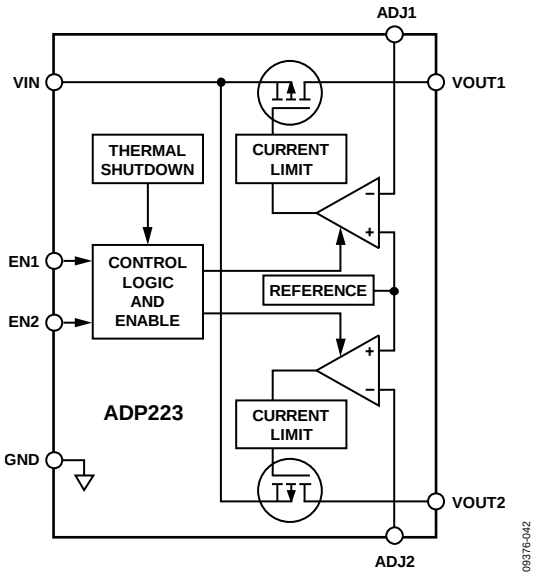

Figure 44. Internal Block Diagram

Internally, the ADP223 consist of a reference, two error amplifiers, and two PMOS pass transistors. Output current is delivered via the PMOS pass device, which is controlled by the error amplifier. The error amplifier compares the reference voltage with the feedback voltage from the output and amplifies the difference. If the feedback voltage is lower than the reference voltage, the gate of the PMOS device is pulled lower, allowing more current to flow and increasing the output voltage. If the feedback voltage is higher than the reference voltage, the gate of the PMOS device is pulled higher, allowing less current to flow and decreasing the output voltage.

The ADP223 uses the EN1/EN2 pins to enable and disable the VOUT1/VOUT2 pins under normal operating conditions. When EN1/EN2 are high, VOUT1/VOUT2 turn on; when EN1/EN2 are low, VOUT1/VOUT2 turn off. For automatic startup, EN1/EN2 can be tied to VIN.

The output voltages can be set according to the following equations:

$$V_{OUT1} = 0.50\ \text{V}(1 + R1/R2)$$

$$V_{OUT2} = 0.50\ \text{V}(1 + R3/R4)$$

APPLICATIONS INFORMATION

CAPACITOR SELECTION

Output Capacitor

The ADP223 is designed for operation with small, space-saving ceramic capacitors but functions with most commonly used capacitors as long as care is taken with regard to the effective series resistance (ESR) value. The ESR of the output capacitor affects the stability of the LDO control loop. A minimum of 1 µF capacitance with an ESR of 1 Ω or less is recommended to ensure the stability of the ADP223. Transient response to changes in load current is also affected by output capacitance. Using a larger value of output capacitance improves the transient response of the ADP223 to large changes in load current. Figure 45 shows the transient responses for an output capacitance value of 1 µF.

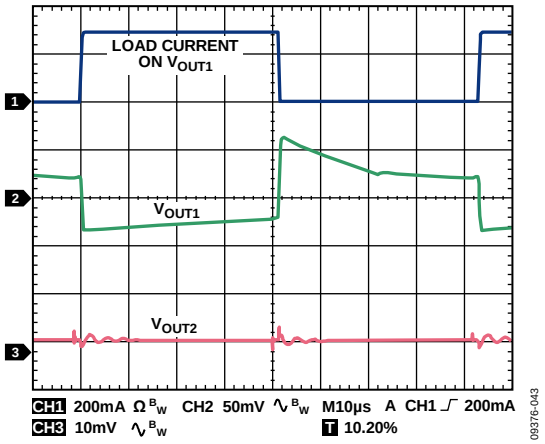

Figure 45. Output Transient Response, C_{OUT} = 1 µF

Input Bypass Capacitor

Connecting a 1 µF capacitor from VIN to GND reduces the circuit sensitivity to the printed circuit board (PCB) layout, especially when long input traces or high source impedance are encountered. If output capacitance greater than 1 µF is required, the input capacitor should be increased to match it.

Input and Output Capacitor Properties

Any good quality ceramic capacitors can be used with the ADP223, as long as they meet the minimum capacitance and maximum ESR requirements. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior over temperature and applied voltage. Capacitors must have a dielectric adequate to ensure the minimum capacitance over the necessary temperature range and dc bias conditions. X5R or X7R dielectrics with a voltage rating of 6.3 V or 10 V are recommended; however, Y5V and Z5U dielectrics are not recommended, due to their poor temperature and dc bias characteristics.

Figure 46 shows the capacitance vs. voltage bias characteristic of an 0402, 1 µF, 10 V, X5R capacitor. The voltage stability of a capacitor is strongly influenced by the capacitor size and voltage rating. In general, a capacitor in a larger package or with a higher voltage rating exhibits better stability. The temperature variation of the X5R dielectric is approximately ±15% over the −40°C to +85°C temperature range and is not a function of package or voltage rating.

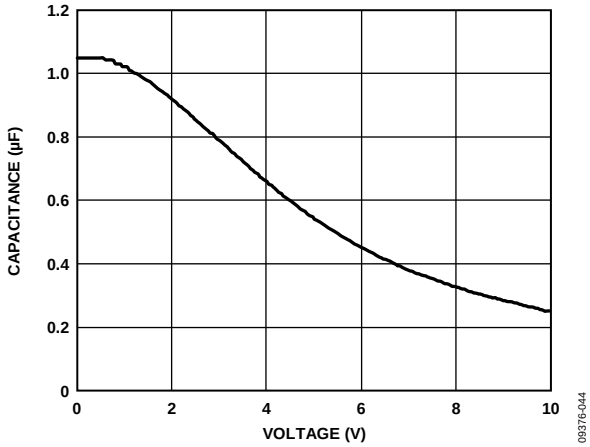

Figure 46. Capacitance vs. Voltage Bias Characteristic

Use Equation 1 to determine the worst-case capacitance, accounting for capacitor variation over temperature, component tolerance, and voltage.

$$C_{EFF} = C_{BIAS} \times (1 - TEMPCO) \times (1 - TOL) \quad (1)$$

where:
C_{BIAS} is the effective capacitance at the operating voltage.
TEMPCO is the worst-case capacitor temperature coefficient.
TOL is the worst-case component tolerance.

In this example, the worst-case temperature coefficient (TEMPCO) over −40°C to +85°C is assumed to be 15% for an X5R dielectric. The tolerance of the capacitor (TOL) is assumed to be 10%, and C_{BIAS} is 0.94 µF at 1.8 V, as shown in Figure 46.

Substituting these values in Equation 1 yields

$$C_{EFF} = 0.94\ \mu F \times (1 - 0.15) \times (1 - 0.1) = 0.719\ \mu F$$

Therefore, the capacitor chosen in this example meets the minimum capacitance requirement of the LDO over temperature and tolerance at the chosen output voltage.

To guarantee the performance of the ADP223, it is imperative that the effects of dc bias, temperature, and tolerances on the behavior of the capacitors be evaluated for each application.

ENABLE FEATURE

The ADP223 uses the ENx pins to enable and disable the VOUTx pins under normal operating conditions. Figure 47 shows a rising voltage on ENx crossing the active threshold, then VOUTx turns on. When a falling voltage on ENx crosses the inactive threshold, VOUTx turns off.

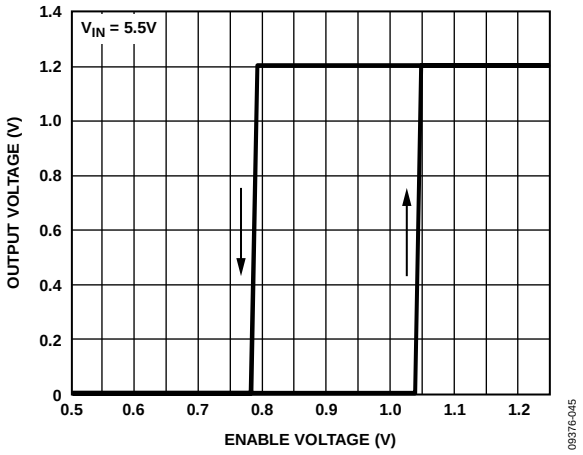

Figure 47. Typical ENx Pin Operation, V_{IN} = 5.5 V

As shown in Figure 47, the ENx pins have built-in hysteresis. This prevents on/off oscillations that can occur due to noise on the ENx pins as they pass through the threshold points.

The active/inactive thresholds of the ENx pins are derived from the VIN voltage. Therefore, these thresholds vary with changing input voltage. Figure 48 shows typical ENx active/inactive thresholds when the input voltage varies from 2.5 V to 5.5 V.

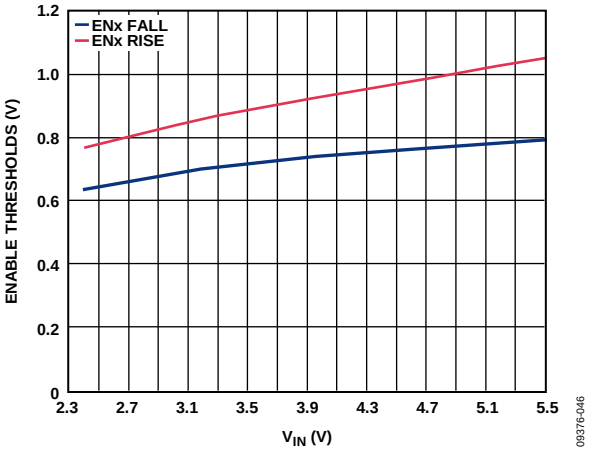

Figure 48. Typical Enable Thresholds vs. Input Voltage

The ADP223 uses an internal soft start to limit the inrush current when the output is enabled. The start-up time for the 3.3 V option is approximately 240 µs from the time the ENx active threshold is crossed to when the output reaches 90% of its final value. The start-up time is somewhat dependent on the output voltage setting and increases slightly as the output voltage increases.

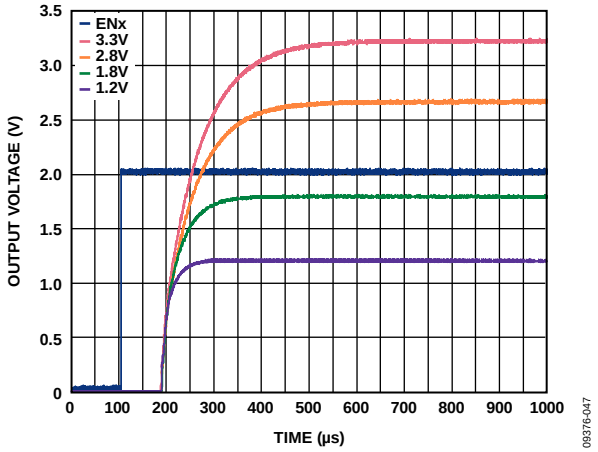

Figure 49. Typical Start-Up Time

PARALLELING OUTPUTS TO INCREASE OUTPUT CURRENT

The ADP223 uses a single band gap to generate the reference voltage for each LDO. The reference voltages are trimmed to plus or minus a couple of millivolts of each other. This allows paralleling of the LDOs to increase the output current to 600 mA. The adjust pins of each LDO are tied together and a single output voltage divider sets the output voltage. Even though the output voltage of each LDO is slightly different, at high load currents, the resistance of the package and the board layout absorbs the difference. Figure 50 shows the schematic of a typical application where the LDO outputs are paralleled.

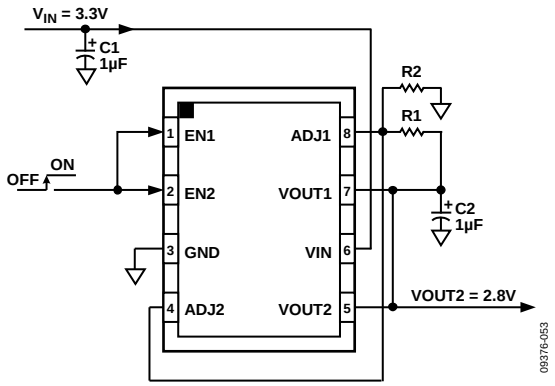

Figure 50. Paralleling Outputs for Higher Output Current

CURRENT LIMIT AND THERMAL OVERLOAD PROTECTION

The ADP223 is protected against damage due to excessive power dissipation by current and thermal overload protection circuits. The ADP223 is designed to limit current when the output load reaches 440 mA (typical). When the output load exceeds 440 mA, the output voltage is reduced to maintain a constant current limit.

Thermal overload protection is included, which limits the junction temperature to a maximum of 155°C (typical). Under extreme conditions (that is, high ambient temperature and/or high power dissipation) when the junction temperature starts to rise above 150°C, the output is turned off, reducing the output current to zero. When the junction temperature drops below 135°C, the output is turned on again, and output current is restored to its operating value.

Consider the case where a hard short from VOUTx to ground occurs. At first, the ADP223 limits current, so that only 300 mA is conducted into the short. If self-heating of the junction is great enough to cause its temperature to rise above 155°C, thermal shutdown is activated, turning off the output and reducing the output current to zero. As the junction temperature cools and drops below 135°C, the output turns on and conducts 300 mA into the short, again causing the junction temperature to rise above 155°C. This thermal oscillation between 135°C and 155°C causes a current oscillation between 300 mA and 0 mA that continues as long as the short remains at the output.

Current and thermal limit protections are intended to protect the device against accidental overload conditions. For reliable operation, device power dissipation must be externally limited so that the junction temperature does not exceed 125°C.

THERMAL CONSIDERATIONS

In applications with low input-to-output voltage differential, the ADP223 does not dissipate much heat. However, in applications with high ambient temperature and high input voltage to output voltage differential, the heat dissipated in the package is large enough that it can cause the junction temperature of the die to exceed the maximum junction temperature of 125°C.

When the junction temperature exceeds 155°C, the converter enters thermal shutdown. It recovers only after the junction temperature has decreased below 135°C to prevent any permanent damage. Therefore, thermal analysis of the chosen application is very important to guarantee reliable performance over all conditions. The junction temperature of the die is the sum of the ambient temperature of the environment and the temperature rise of the package due to power dissipation, as shown in Equation 2.

To guarantee reliable operation, the junction temperature of the ADP223 must not exceed 125°C. To ensure that the junction temperature stays below this maximum value, the user must be aware of the parameters that contribute to junction temperature changes. These parameters include ambient temperature, power dissipation in the device, and thermal resistance between the junction and ambient air (θ_{JA}). The θ_{JA} value is dependent on the package assembly compounds that are used and the amount of copper used to solder the package GND pins to the PCB.

Table 6 shows typical θ_{JA} values for the 8-lead LFCSP package for various PCB copper sizes, and Table 7 shows the typical Ψ_{JB} value for the 8-lead LFCSP.

Table 6. Typical θ_{JA} Values

Copper Size (mm²)	θ_{JA} (°C/W)
25[1]	175.1
100	135.6
500	77.3
1000	65.2
6400	51

[1] Device soldered to minimum size pin traces.

Table 7. Typical Ψ_{JB} Values

Model	Ψ_{JB} (°C/W)
8-Lead LFCSP	18.2

The junction temperature of the ADP223 is calculated from

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (2)$$

where:
T_A is the ambient temperature.
P_D is the power dissipation in the die, given by

$$P_D = [(V_{IN} - V_{OUT}) \times I_{LOAD}] + (V_{IN} \times I_{GND})$$

where:
V_{IN} and V_{OUT} are the input and output voltages, respectively.
I_{LOAD} is the load current.
I_{GND} is the ground current.

Power dissipation due to ground current is quite small and can be ignored. Therefore, the junction temperature equation simplifies to the following:

$$T_J = T_A + \{[(V_{IN} - V_{OUT}) \times I_{LOAD}] \times \theta_{JA}\}$$

As shown in the simplified equation, for a given ambient temperature, input-to-output voltage differential, and continuous load current, there exists a minimum copper size requirement for the PCB to ensure that the junction temperature does not rise above 125°C. Figure 51 to Figure 53 show junction temperature calculations for different ambient temperatures, power dissipation, and areas of PCB copper.

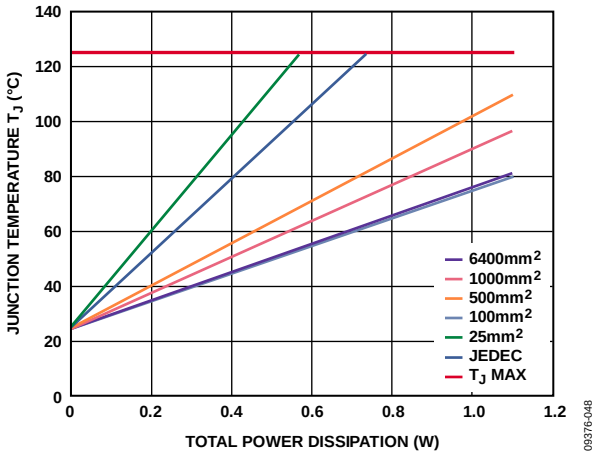

Figure 51. Junction Temperature vs. Total Power Dissipation, T_A = 25°C

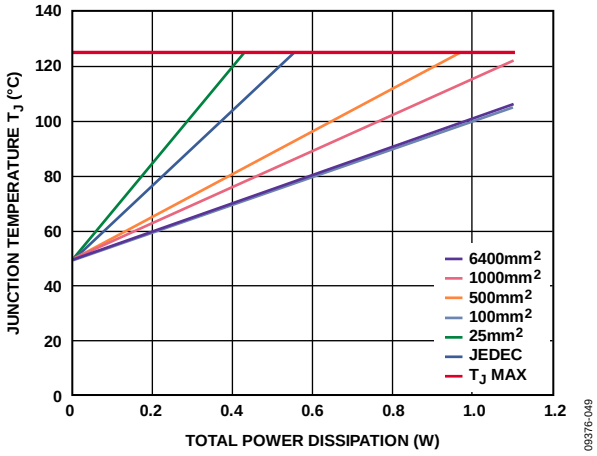

Figure 52. Junction Temperature vs. Total Power Dissipation, T_A = 50°C

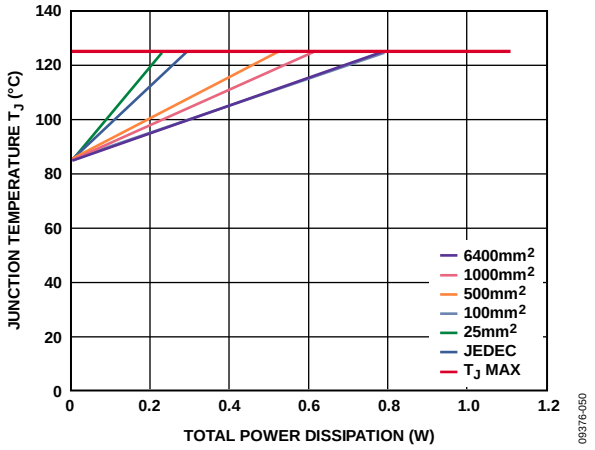

Figure 53. Junction Temperature vs. Total Power Dissipation, T_A = 85°C

In the case where the board temperature is known, use the thermal characterization parameter, Ψ_{JB}, to estimate the junction temperature rise (see Figure 54). Maximum junction temperature (T_J) is calculated from the board temperature (T_B) and power dissipation (P_D) using the following formula:

$$T_J = T_B + (P_D \times \Psi_{JB}) \quad (3)$$

The typical value of Ψ_{JB} is 18.2°C/W for the 8-lead LFCSP package.

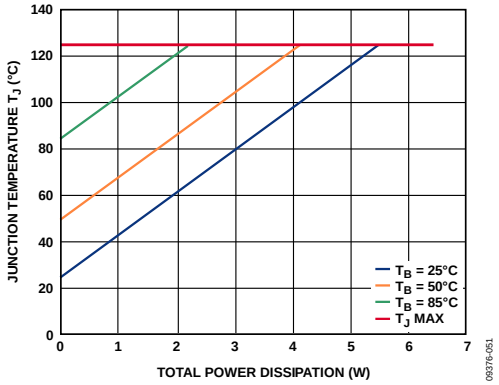

Figure 54. Junction Temperature vs. Total Power Dissipation and Board Temperature, T_A = 85°C

PRINTED CIRCUIT BOARD LAYOUT CONSIDERATIONS

Heat dissipation from the package can be improved by increasing the amount of copper attached to the pins of the ADP223. However, as shown in Table 6, a point of diminishing returns is eventually reached beyond which an increase in the copper size does not yield significant heat dissipation benefits.

Place the input capacitor as close as possible to the VIN and GND pins. Place the output capacitor as close as possible to the VOUTx and GND pins. The use of 0402 or 0603 size capacitors and resistors achieves the smallest possible footprint solution on boards where area is limited.

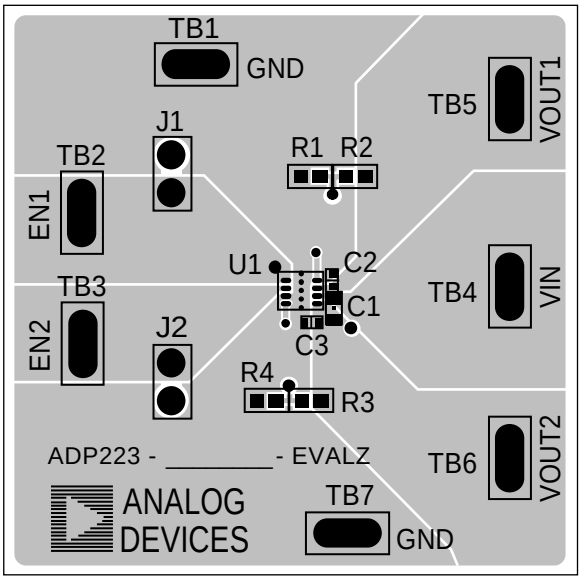

Figure 55. Example PCB Layout for the 8-Lead LFCSP

OUTLINE DIMENSIONS

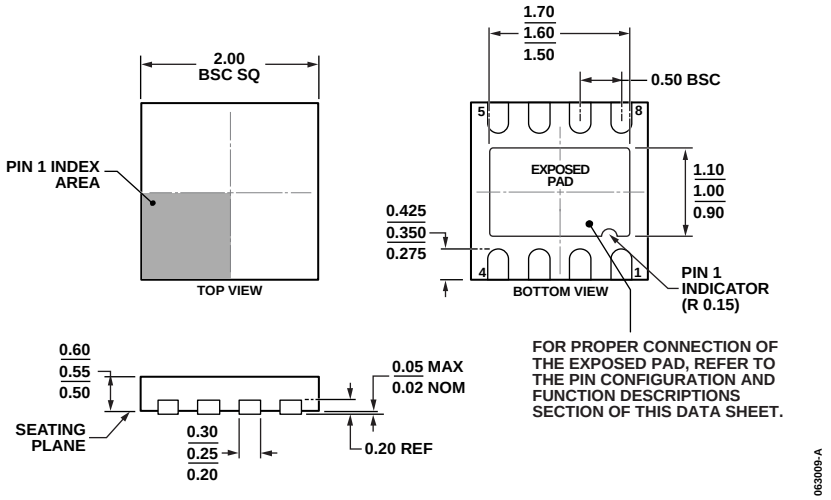

Figure 56. 8-Lead Lead Frame Chip Scale Package [LFCSP_UD]
2.00 mm × 2.00 mm Body, Ultra Thin, Dual Lead
(CP-8-10)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Output Voltage (V)	Package Description	Package Option	Branding
ADP223ACPZ-R7	−40°C to +125°C	Adjustable	8-Lead Lead Frame Chip Scale Package [LFCSP_UD]	CP-8-10	LJQ
ADP223CP-EVALZ		Adjustable	Evaluation Board		

[1] Z = RoHS Compliant Part.

D09376-0-4/11(0)