

# OVERVOLTAGE AND OVERCURRENT PROTECTION IC AND Li+ CHARGER FRONT-END PROTECTION IC

Check for Samples: [bq24314C](#)

## FEATURES

- Provides Protection for Three Variables:
  - Input Overvoltage, with Rapid Response in  $< 1 \mu\text{s}$
  - User-Programmable Overcurrent with Current Limiting
  - Battery Overvoltage
- 30V Maximum Input Voltage
- Supports up to 1.5A Input Current
- Robust Against False Triggering Due to Current Transients
- Thermal Shutdown
- Enable Input
- Status Indication – Fault Condition

- Available in Space-Saving Small 8 Lead 2x2 SON

## APPLICATIONS

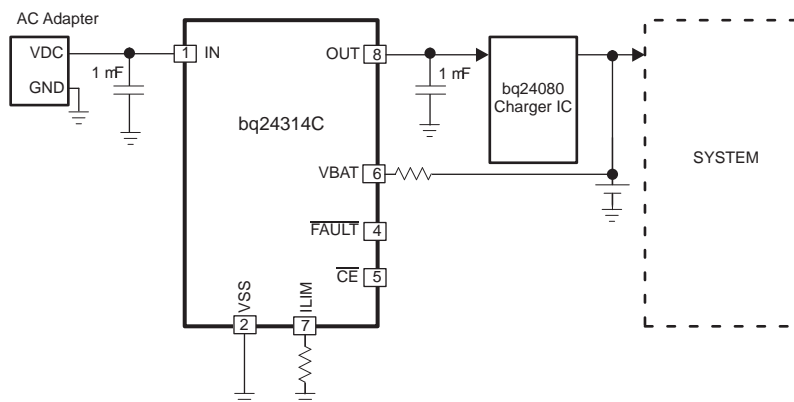
- Mobile Phones and Smart Phones
- PDAs
- MP3 Players
- Low-Power Handheld Devices
- Bluetooth™ Headsets

## DESCRIPTION

The bq24314C is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current, and the battery voltage. In case of an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable.

The IC can be controlled by a processor and also provides status information about fault conditions to the host.

## APPLICATION SCHEMATIC



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PowerPAD is a trademark of Texas Instruments.

Bluetooth is a trademark of Bluetooth SIG, Inc.



**RECOMMENDED OPERATING CONDITIONS**

over operating free-air temperature range (unless otherwise noted)

		<b>MIN</b>	<b>MAX</b>	<b>UNIT</b>
$V_{IN}$	Input voltage range	3	30	V
$I_{IN}$	Input current, IN pin		1.5	A
$I_{OUT}$	Output current, OUT pin		1.5	A
$R_{ILIM}$	OCP Programming resistor	15	90	k
$T_J$	Junction temperature	–40	125	°C



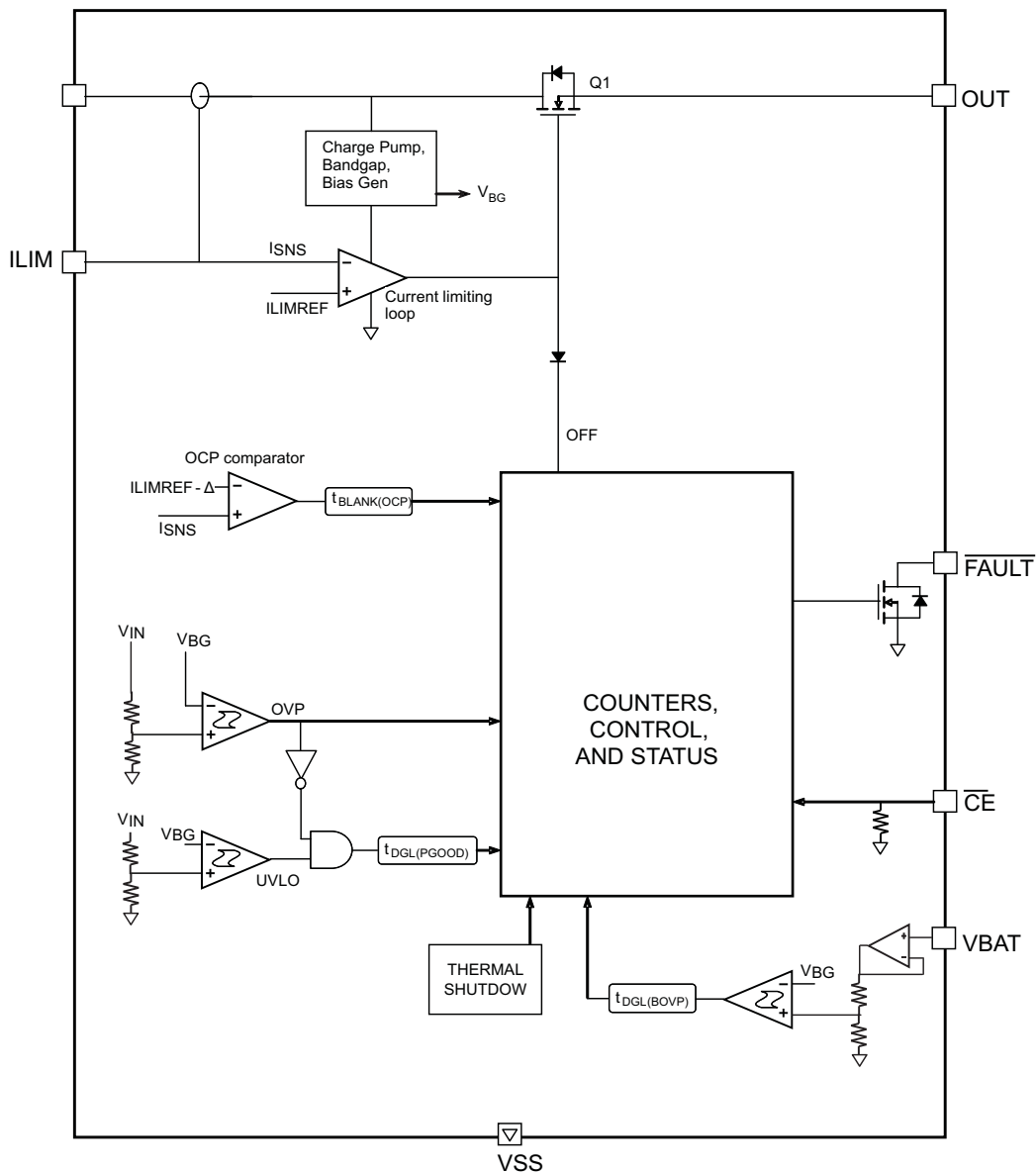


Figure 1. Simplified Block Diagram

## TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	DSG		
IN	1	I	Input power, connect to external DC supply. Connect external 1µF ceramic capacitor (minimum) to V <sub>SS</sub> .
OUT	8	O	Output terminal to the charging system. Connect external 1µF ceramic capacitor (minimum) to V <sub>SS</sub> .
VBAT	6	I	Battery voltage sense input. Connect to pack positive terminal through a resistor.
ILIM	7	I/O	Input overcurrent threshold programming. Connect a resistor to V <sub>SS</sub> to set the overcurrent threshold.
$\overline{\text{CE}}$	5	I	Chip enable input. Active low. When $\overline{\text{CE}}$ = High, the input FET is off. Internally pulled down.
$\overline{\text{FAULT}}$	4	O	Open-drain output, device status. $\overline{\text{FAULT}}$ = Low indicates that the input FET Q1 has been turned off due to input overvoltage, input overcurrent, battery overvoltage, or thermal shutdown.
VSS	2	–	Ground terminal
NC	3		These pins may have internal circuits used for test purposes. Do not make any external connections at these pins for normal operation.
Thermal PAD		–	There is an internal electrical connection between the exposed thermal pad and the V <sub>SS</sub> pin of the device. The thermal pad must be connected to the same potential as the V <sub>SS</sub> pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. The V <sub>SS</sub> pin must be connected to ground at all times.

DSG Package  
(Top View)

VSS

NC

### TYPICAL OPERATING PERFORMANCE

Test conditions (unless otherwise noted) for typical operating performance:  $V_{IN} = 5\text{ V}$ ,  $C_{IN} = 1\text{ }\mu\text{F}$ ,  $C_{OUT} = 1\text{ }\mu\text{F}$ ,  $R_{ILIM} = 25\text{ k}$ ,  $R_{BAT} = 100\text{ k}$ ,  $T_A = 25^\circ\text{C}$ ,  $V_{PU} = 3.3\text{V}$  (see Figure 20 for the Typical Application Circuit)

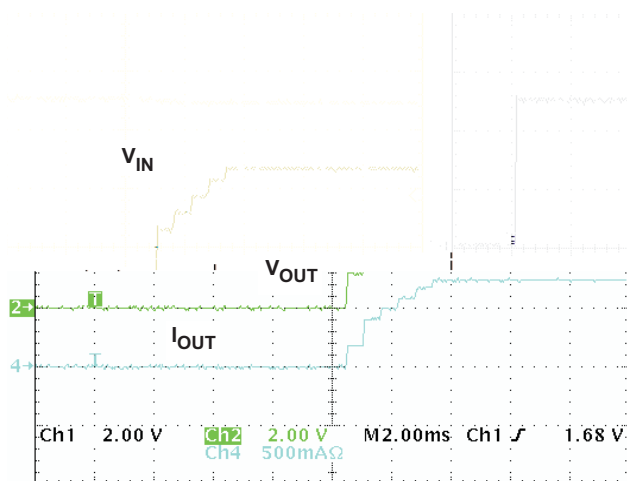


Figure 2. Normal Power-On Showing Soft-Start,  $R_{OUT} = 6.6$

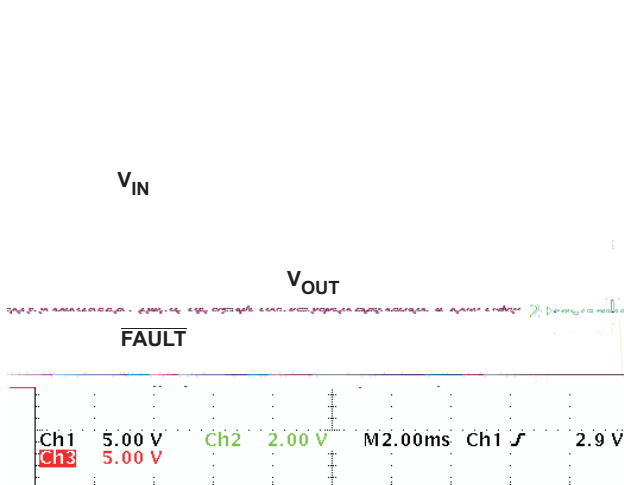


Figure 3. OVP at Power-On,  $V_{IN} = 0\text{V to }9\text{V}$ ,  $t_r = 50\mu\text{s}$

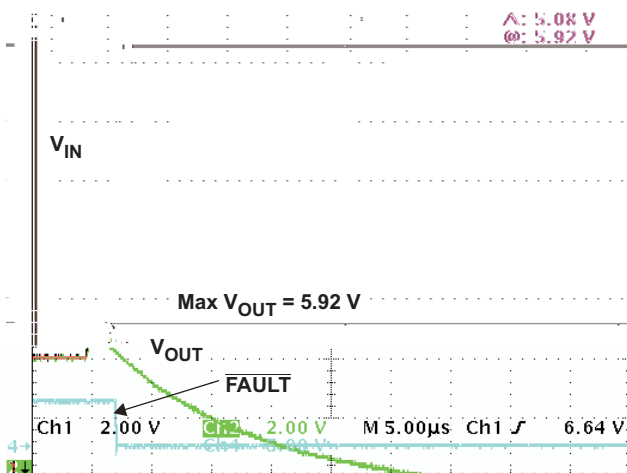


Figure 4. OVP Response for Input Step,  $V_{IN} = 5\text{V to }12\text{V}$ ,  $t_r = 1\mu\text{s}$

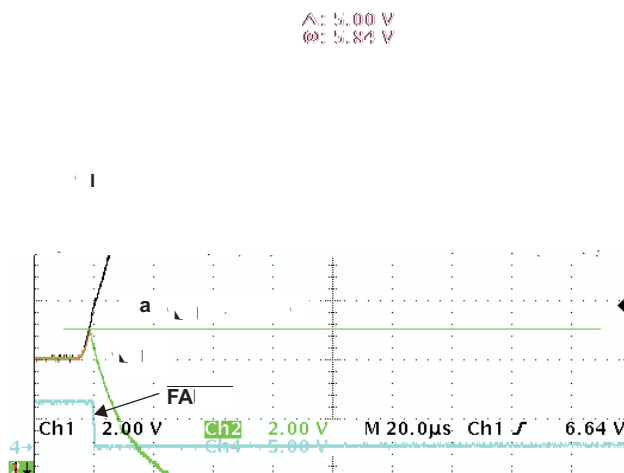


Figure 5. OVP Response for Input Step,  $V_{IN} = 5\text{V to }12\text{V}$ ,  $t_r = 20\mu\text{s}$

TYPICAL OPERATING PERFORMANCE (continued)

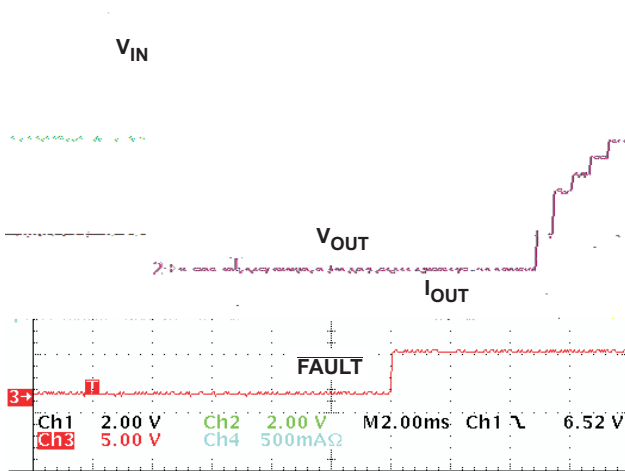


Figure 6. Recovery from OVP,  $V_{IN} = 7.5V$  to 5V,  $t_r = 400\mu s$

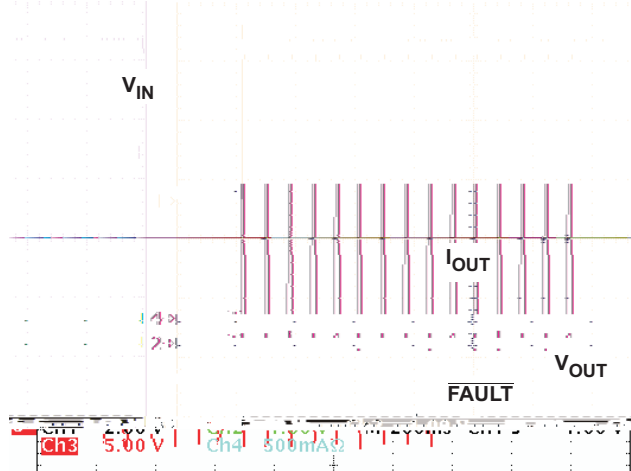


Figure 7. OCP, Powering Up into a Short Circuit on OUT Pin, OCP Counter Counts to 15 Before Switching OFF the Device

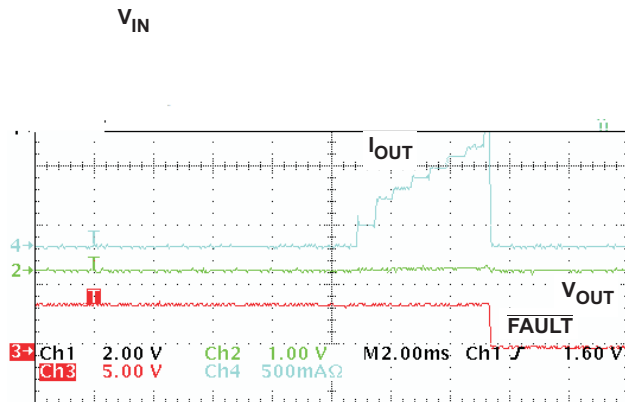


Figure 8. OCP, Zoom-in on the First Cycle of Figure 7

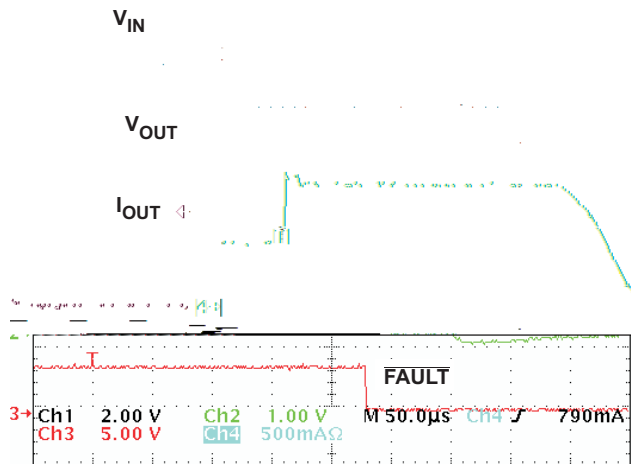


Figure 9. OCP,  $R_{OUT}$  Switches from 6.6 to 3.3, Shows Current Limiting and Soft-Stop

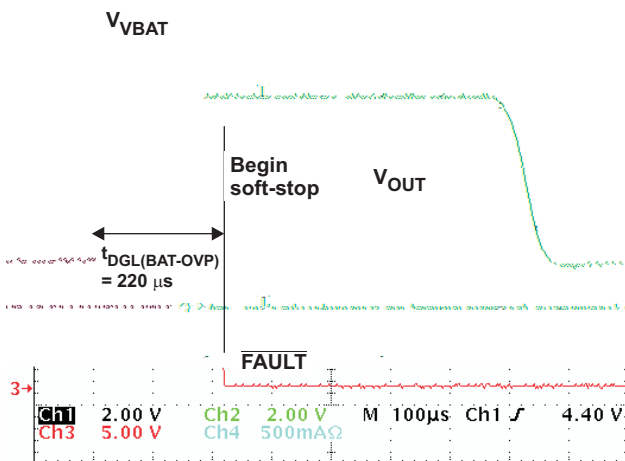


Figure 10. BAT-OVP,  $V_{VBAT}$  Steps from 4.2V to 4.4V, Shows  $t_{DGL(BAT-OVP)}$  and Soft-Stop

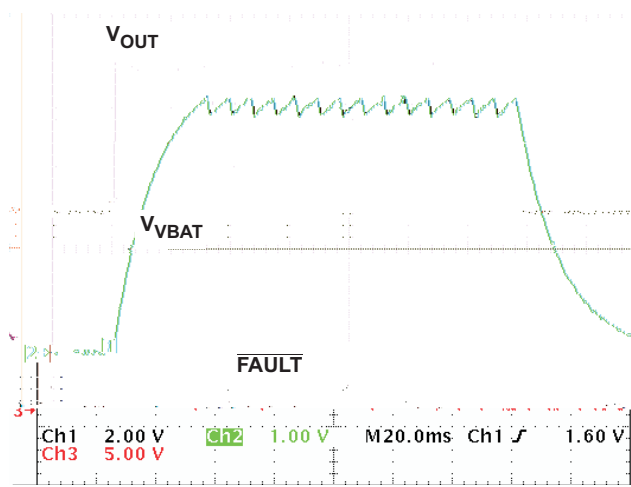


Figure 11. BAT-OVP,  $V_{VBAT}$  Cycles Between 4.1V and 4.4V, Shows BAT-OVP Counter



TYPICAL OPERATING PERFORMANCE (continued)

UNDERVOLTAGE LOCKOUT  
vs  
FREE-AIR TEMPERATURE

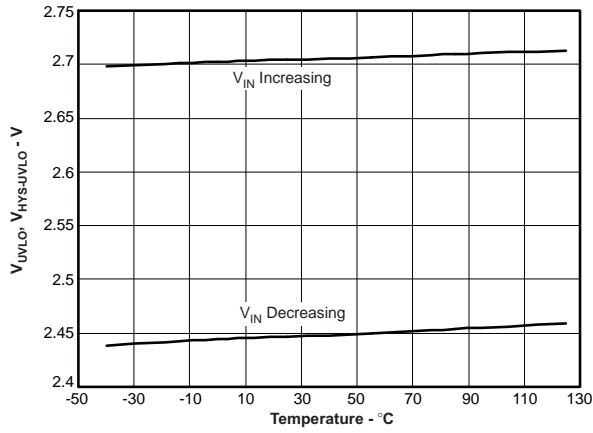


Figure 12.

DROPOUT VOLTAGE (IN to OUT)  
vs  
FREE-AIR TEMPERATURE

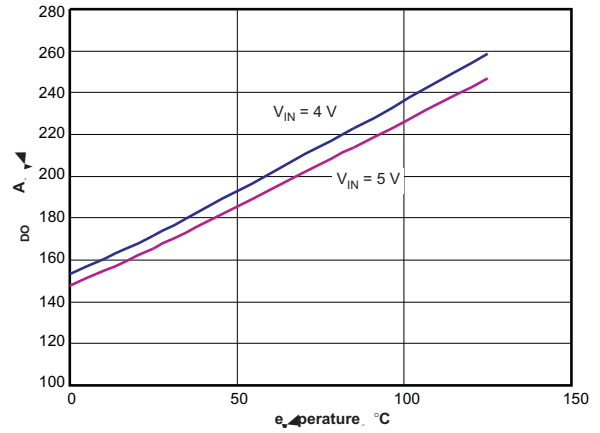


Figure 13.

OVERVOLTAGE THRESHOLD PROTECTION  
vs  
FREE-AIR TEMPERATURE

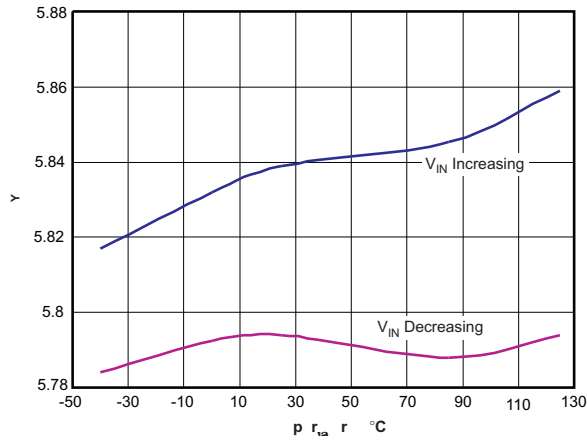


Figure 14.

INPUT OVERCURRENT PROTECTION  
vs  
ILIM RESISTANCE

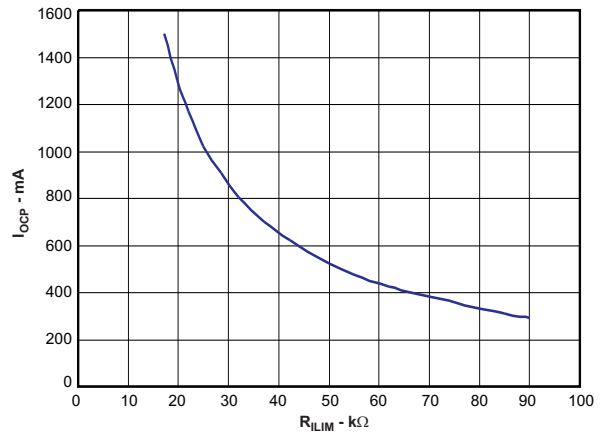


Figure 15.

**TYPICAL OPERATING PERFORMANCE (continued)**

**INPUT OVERCURRENT PROTECTION  
vs  
FREE-AIR TEMPERATURE**

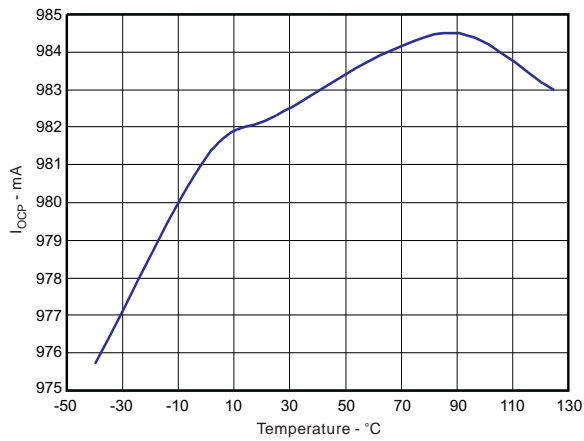


Figure 16.

**BATTERY OVERVOLTAGE PROTECTION  
vs  
FREE-AIR TEMPERATURE**



Figure 17.

**LEAKAGE CURRENT (VBAT Pin)  
vs  
FREE-AIR TEMPERATURE**

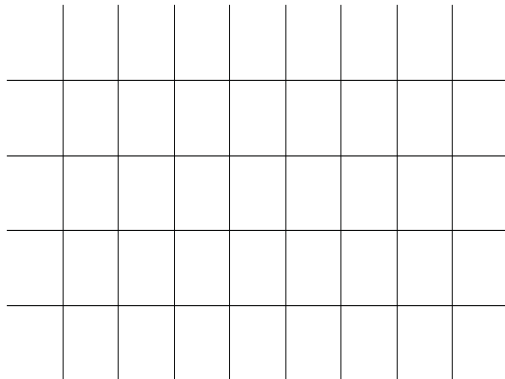


Figure 18.

**SUPPLY CURRENT  
vs  
INPUT VOLTAGE**

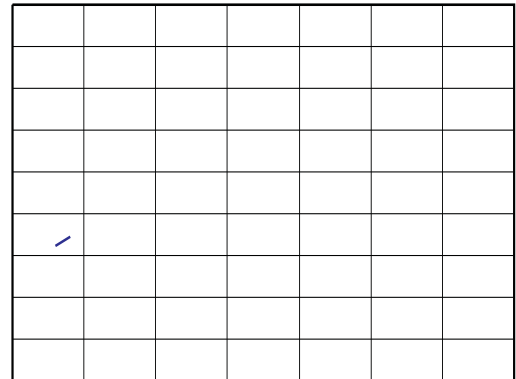


Figure 19.

## TYPICAL APPLICATION CIRCUIT

$V_{OVP} = 6.8V$ ,  $I_{OCP} = 1000mA$ ,  $BV_{OVP} = 4.45V$  (Terminal numbers shown are for the 2x2 DSG package)

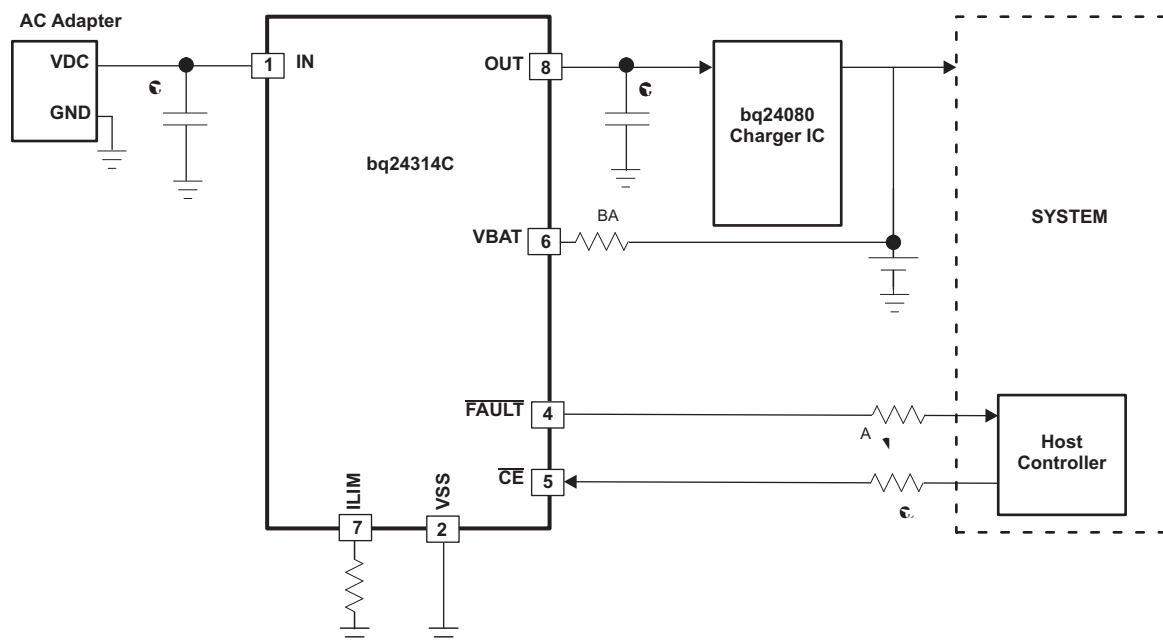


Figure 20.

## DETAILED FUNCTIONAL DESCRIPTION

The bq24314C is a highly integrated circuit designed to provide protection to Li-ion batteries from failures of the charging circuit. The IC continuously monitors the input voltage, the input current and the battery voltage. In case of an input overvoltage condition, the IC immediately removes power from the charging circuit by turning off an internal switch. In the case of an overcurrent condition, it limits the system current at the threshold value, and if the overcurrent persists, switches the pass element OFF after a blanking period. If the battery voltage rises to an unsafe level, the IC disconnects power from the charging circuit until the battery voltage returns to an acceptable value. Additionally, the IC also monitors its own die temperature and switches off if it exceeds 140°C. The input overcurrent threshold is user-programmable. The IC can be controlled by a processor, and also provides status information about fault conditions to the host.

### POWER DOWN

The device remains in power down mode when the input voltage at the IN pin is below the undervoltage threshold UVLO. The FET Q1 connected between IN and OUT pins is off, and the status output, FAULT, is set to Hi-Z.

### POWER-ON RESET

The device resets when the input voltage at the IN pin exceeds the UVLO threshold. All internal counters and other circuit blocks are reset. The IC then waits for duration  $t_{DGL(PGOOD)}$  for the input voltage to stabilize. If, after  $t_{DGL(PGOOD)}$ , the input voltage and battery voltage are safe, FET Q1 is turned ON. The IC has a soft-start feature to control the inrush current. The soft-start minimizes the ringing at the input (the ringing occurs because the parasitic inductance of the adapter cable and the input bypass capacitor form a resonant circuit). Figure 2 shows the power-up behavior of the device. Because of the deglitch time at power-on, if the input voltage rises rapidly to beyond the OVP threshold, the device will not switch on at all, instead it will go into protection mode and indicate a fault on the FAULT pin, as shown in Figure 3.

## OPERATION

The device continuously monitors the input voltage, the input current, and the battery voltage as described in detail in the following sections.

### Input Overvoltage Protection

If the input voltage rises above  $V_{OVP}$ , the internal FET Q1 is turned off, removing power from the circuit. As shown in [Figure 4](#) to [Figure 5](#), the response is very rapid, with the FET turning off in less than a microsecond. The  $\overline{\text{FAULT}}$  pin is driven low. When the input voltage returns below  $V_{OVP} - V_{hys(OVP)}$  (but is still above UVLO), the FET Q1 is turned on again after a deglitch time of  $t_{ON(OVP)}$  to ensure that the input supply has stabilized. [Figure 6](#) shows the recovery from input OVP.

### Input Overcurrent Protection

The overcurrent threshold is programmed by a resistor  $R_{ILIM}$  connected from the ILIM pin to VSS. [Figure 15](#) shows the OCP threshold as a function of  $R_{ILIM}$ , and may be approximated by the following equation:  $I_{OCP} = 25 \div R_{ILIM}$  (current in A, resistance in k $\Omega$ ), where  $R_{ILIM}$  must be between 15 k $\Omega$  and 90 k $\Omega$ .

If the load current tries to exceed the  $I_{OCP}$  threshold, the device limits the current for a blanking duration of  $t_{BLANK(OCP)}$ . If the load current returns to less than  $I_{OCP}$  before  $t_{BLANK(OCP)}$  times out, the device continues to operate. However, if the overcurrent situation persists for  $t_{BLANK(OCP)}$ , the FET Q1 is turned off for a duration of  $t_{REC(OCP)}$ , and the  $\overline{\text{FAULT}}$  pin is driven low. The FET is then turned on again after  $t_{REC(OCP)}$  and the current is monitored all over again. Each time an OCP fault occurs, an internal counter is incremented. If 15 OCP faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the  $\overline{\text{CE}}$  pin. [Figure 7](#) to [Figure 9](#) show what happens in an overcurrent fault.

To prevent the input voltage from spiking up due to the inductance of the input cable, Q1 is turned off slowly, resulting in a “soft-stop”, as shown in [Figure 9](#).

### Battery Overvoltage Protection

The battery overvoltage threshold  $BV_{OVP}$  is internally set to 4.45V. If the battery voltage exceeds the  $BV_{OVP}$  threshold, the FET Q1 is turned off, and the  $\overline{\text{FAULT}}$  pin is driven low. The FET is turned back on once the battery voltage drops to  $BV_{OVP} - V_{hys(Bovp)}$  (see [Figure 10](#) and [Figure 11](#)). Each time a battery overvoltage fault occurs, an internal counter is incremented. If 15 such faults occur in one charge cycle, the FET is turned off permanently. The counter is cleared either by removing and re-applying input power, or by disabling and re-enabling the device with the  $\overline{\text{CE}}$  pin. In the case of a battery overvoltage fault, Q1 is switched OFF gradually (see [Figure 10](#)).

### Thermal Protection

If the junction temperature of the device exceeds  $T_{J(OFF)}$ , the FET Q1 is turned off, and the  $\overline{\text{FAULT}}$  pin is driven low. The FET is turned back on when the junction temperature falls below  $T_{J(OFF)} - T_{J(OFF-HYS)}$ .

### Enable Function

The IC has an enable pin which can be used to enable or disable the device. When the  $\overline{\text{CE}}$  pin is driven high, the internal FET is turned off. When the  $\overline{\text{CE}}$  pin is low, the FET is turned on if other conditions are safe. The OCP counter and the Bat-OVP counter are both reset when the device is disabled and re-enabled. The  $\overline{\text{CE}}$  pin has an internal pulldown resistor and can be left floating. Note that the  $\overline{\text{FAULT}}$  pin functionality is also disabled when the  $\overline{\text{CE}}$  pin is high.

### Fault Indication

The  $\overline{\text{FAULT}}$  pin is an active-low open-drain output. It is in a high-impedance state when operating conditions are safe, or when the device is disabled by setting  $\overline{\text{CE}}$  high. With  $\overline{\text{CE}}$  low, the  $\overline{\text{FAULT}}$  pin goes low whenever any of these events occurs:

- Input overvoltage
- Input overcurrent
- Battery overvoltage
- IC Overtemperature

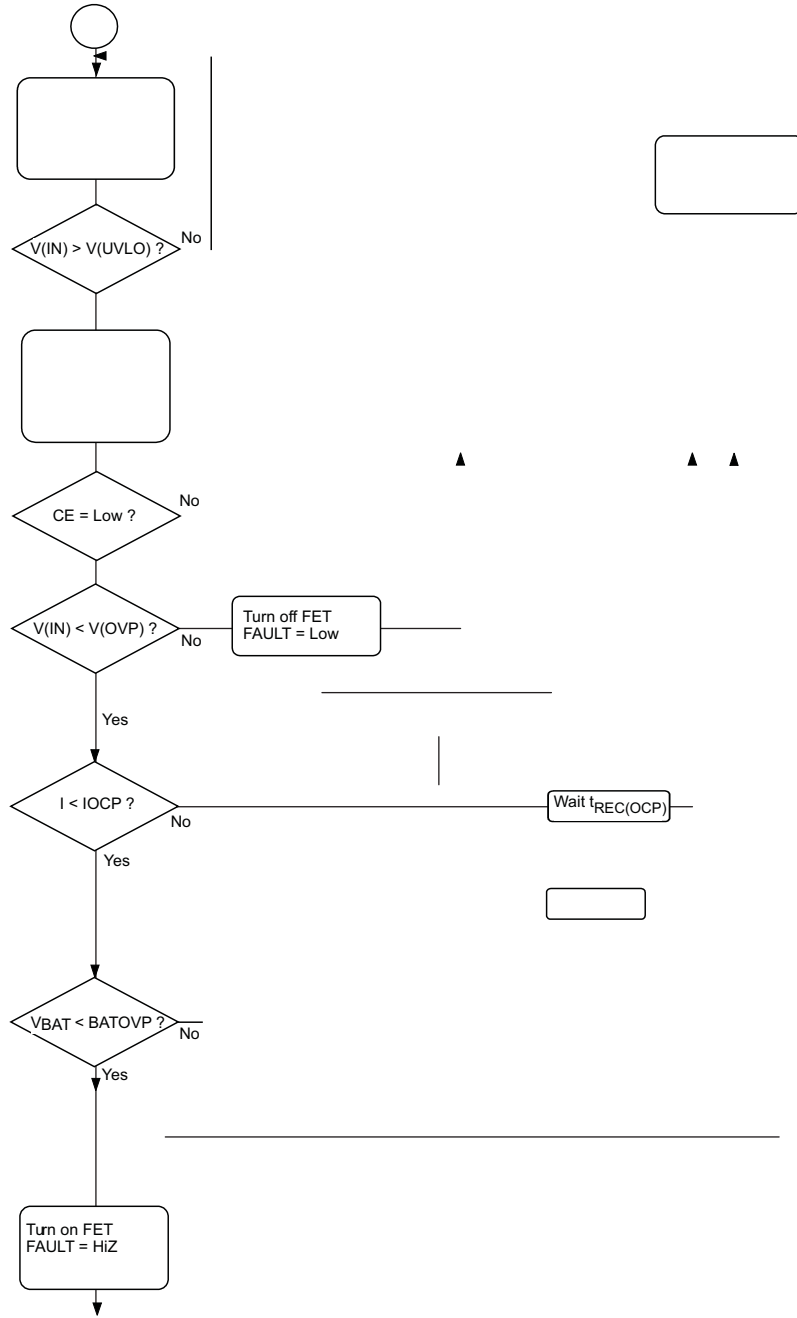


Figure 21. Flow Diagram

## APPLICATION INFORMATION (WITH REFERENCE TO [FIGURE 20](#))

### Selection of $R_{BAT}$

It is strongly recommended that the battery not be tied directly to the VBAT pin of the device, as under some failure modes of the IC, the voltage at the IN pin may appear on the VBAT pin. This voltage can be as high as 30V, and applying 30V to the battery in case of the failure of the bq24314C can be hazardous. Connecting the VBAT pin through  $R_{BAT}$  prevents a large current from flowing into the battery in case of a failure of the IC. In the interests of safety,  $R_{BAT}$  should have a very high value. The problem with a large  $R_{BAT}$  is that the voltage drop across this resistor because of the VBAT bias current  $I_{VBAT}$  causes an error in the  $BV_{OVP}$  threshold. This error is over and above the tolerance on the nominal 4.45V  $BV_{OVP}$  threshold.

Choosing  $R_{BAT}$  in the range 100k to 470k is a good compromise. In the case of an IC failure, with  $R_{BAT}$  equal to 100k, the maximum current flowing into the battery would be  $(30V - 3V) \div 100k = 246\mu A$ , which is low enough to be absorbed by the bias currents of the system components.  $R_{BAT}$  equal to 100k would result in a worst-case voltage drop of  $R_{BAT} \times I_{VBAT} = 1mV$ . This is negligible compared to the internal tolerance of 50mV on  $BV_{OVP}$  threshold.

If the Bat-OVP function is not required, the VBAT pin should be connected to VSS.

### Selection of $R_{CE}$ , $R_{FAULT}$ , and $R_{PU}$

The  $\overline{CE}$  pin can be used to enable and disable the IC. If host control is not required, the  $\overline{CE}$  pin can be tied to ground or left un-connected, permanently enabling the device.

In applications where external control is required, the  $\overline{CE}$  pin can be controlled by a host processor. As in the case of the VBAT pin (see above), the  $\overline{CE}$  pin should be connected to the host GPIO pin through as large a resistor as possible. The limitation on the resistor value is that the minimum  $V_{OH}$  of the host GPIO pin less the drop across the resistor should be greater than  $V_{IH}$  of the bq24314C  $\overline{CE}$  pin. The drop across the resistor is given by  $R_{CE} \times I_{IH}$ .

The  $\overline{FAULT}$  pin is an open-drain output that goes low during OV, OC, battery-OV, and OT events. If the application does not require monitoring of the  $\overline{FAULT}$  pin, it can be left unconnected. But if the  $\overline{FAULT}$  pin has to be monitored, it should be pulled high externally through  $R_{PU}$ , and connected to the host through  $R_{FAULT}$ .  $R_{FAULT}$  prevents damage to the host controller if the bq24314C fails (see above). The resistors should be of high value, in practice values between 22k and 100k should be sufficient.

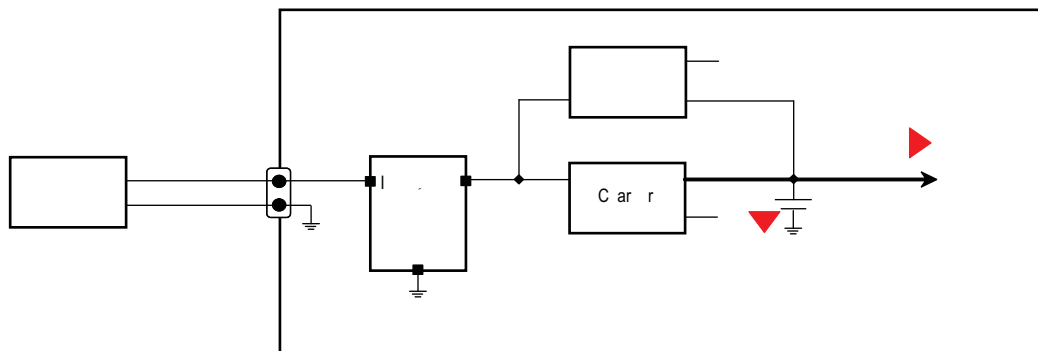
### Selection of Input and Output Bypass Capacitors

The input capacitor  $C_{IN}$  in [Figure 20](#) is for decoupling, and serves an important purpose. Whenever there is a step change downwards in the system load current, the inductance of the input cable causes the input voltage to spike up.  $C_{IN}$  prevents the input voltage from overshooting to dangerous levels. It is strongly recommended that a ceramic capacitor of at least 1 $\mu F$  be used at the input of the device. It should be located in close proximity to the IN pin.

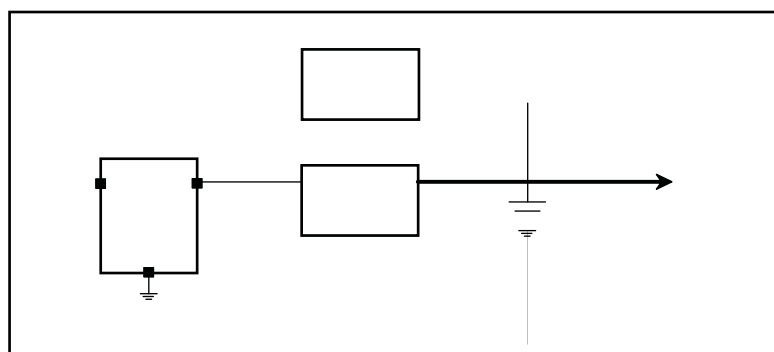
$C_{OUT}$  in [Figure 20](#) is also important: If a very fast (< 1 $\mu s$  rise time) overvoltage transient occurs at the input, the current that charges  $C_{OUT}$  causes the device's current-limiting loop to kick in, reducing the gate-drive to FET Q1. This results in improved performance for input overvoltage protection.  $C_{OUT}$  should also be a ceramic capacitor of at least 1 $\mu F$ , located close to the OUT pin.  $C_{OUT}$  also serves as the input decoupling capacitor for the charging circuit downstream of the protection IC.

### Powering Accessories

In some applications, the equipment that the protection IC resides in may be required to provide power to an accessory (e.g. a cellphone may power a headset or an external memory card) through the same connector pins that are used by the adapter for charging. [Figure 22](#) and [Figure 23](#) illustrate typical charging and accessory-powering scenarios:



**Figure 22. Charging - The Red Arrows Show the Direction of Current Flow**



**Figure 23. Powering an Accessory - The Red Arrows Show the Direction of Current Flow**

In the second case, when power is being delivered to an accessory, the bq24314C device is required to support current flow from the OUT pin to the IN pin.

If  $V_{OUT} > UVLO + 0.7V$ , FET Q1 is turned on, and the reverse current does not flow through the diode but through Q1. Q1 will then remain ON as long as  $V_{OUT} > UVLO - V_{hys(UVLO)} + R_{DS(on)} \times I_{ACCESSORY}$ . Within this voltage range, the reverse current capability is the same as the forward capability, 1.5A. It should be noted that there is no overcurrent protection in this direction.

### PCB Layout Guidelines:

- This device is a protection device, and is meant to protect down-stream circuitry from hazardous voltages. Potentially, high voltages may be applied to this IC. It has to be ensured that the edge-to-edge clearances of PCB traces satisfy the design rules for high voltages.
- The device uses SON packages with a PowerPAD™. For good thermal performance, the PowerPAD should be thermally coupled with the PCB ground plane. In most applications, this will require a copper pad directly under the IC. This copper pad should be connected to the ground plane with an array of thermal vias.
- $C_{IN}$  and  $C_{OUT}$  should be located close to the IC. Other components like  $R_{ILIM}$  and  $R_{BAT}$  should also be located close to the IC.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Peak Temp <sup>(3)</sup>	Samples (Requires Login)
BQ24314CDSGR	ACTIVE	WSON	DSG	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24314CDSGT	ACTIVE	WSON	DSG	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

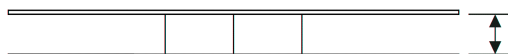
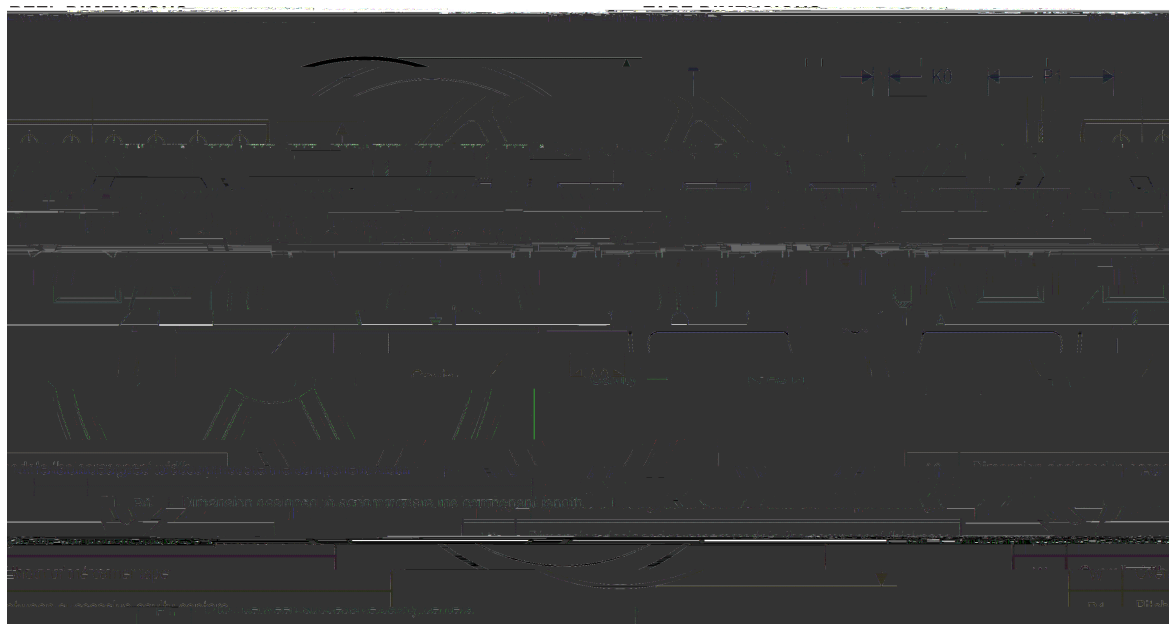
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to (continue) ( ) 62.5 (an8 ( ) 3 6.044001 Tm [(stf5 (TmWhere) ( ) (designed)75 .75- ) 2-8.75 (bed)derway) ( ) -8.7ts"5 (classifications,) ( ) wificatio(may) ( ) ificatio(not) ( ) ifica



## TAPE AND REEL INFORMATION



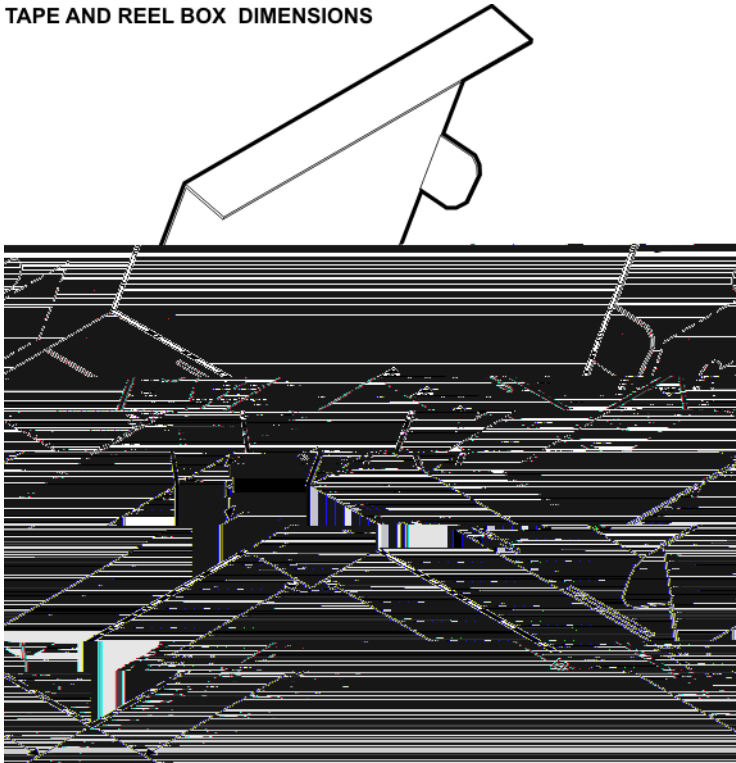
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### TAPE AND REEL INFORMATION

\*All dimensions are nominal

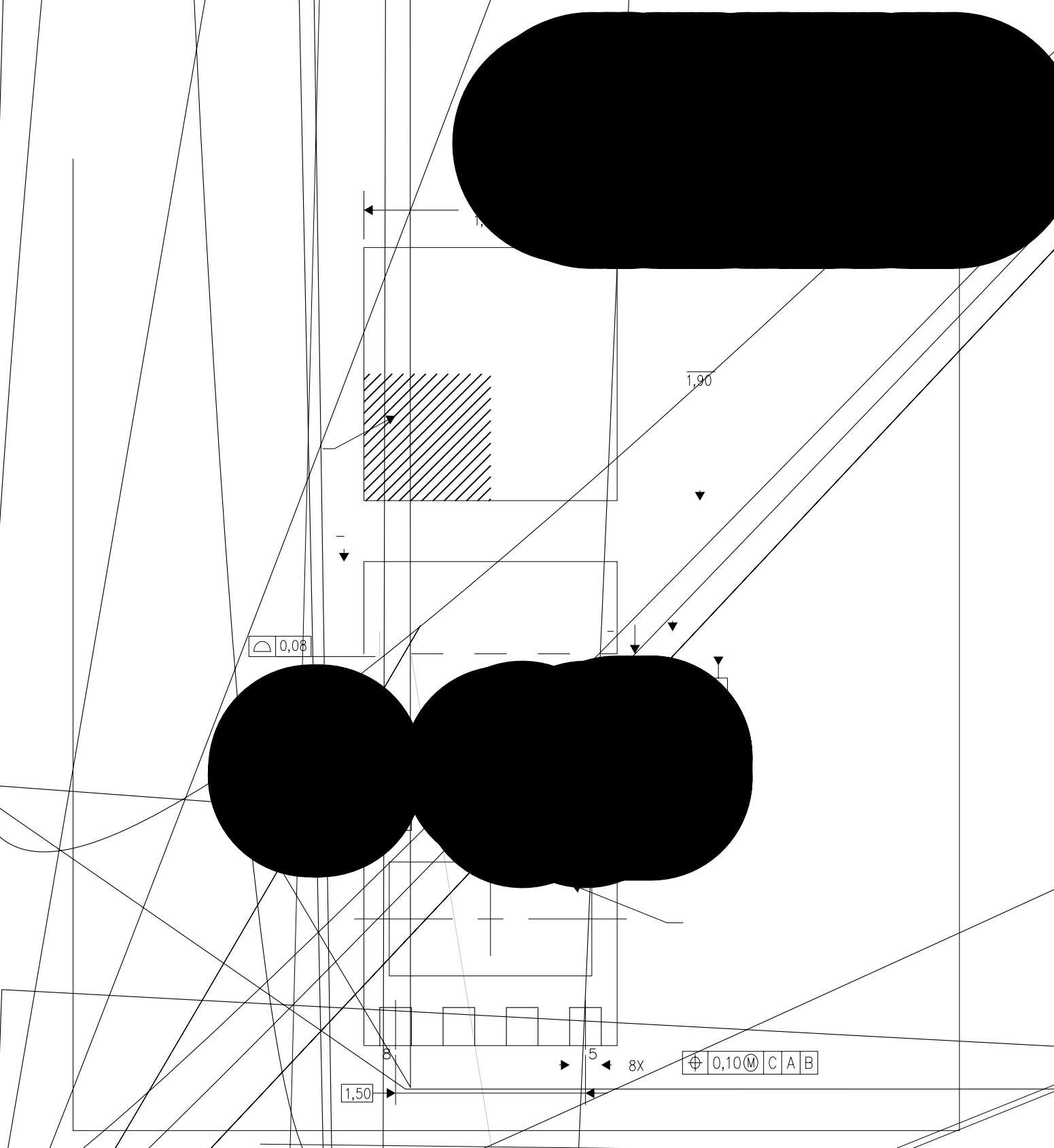
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24314CDSGR	WSON	DSG	8	3000	330.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
BQ24314CDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

## TAPE AND REEL BOX DIMENSIONS

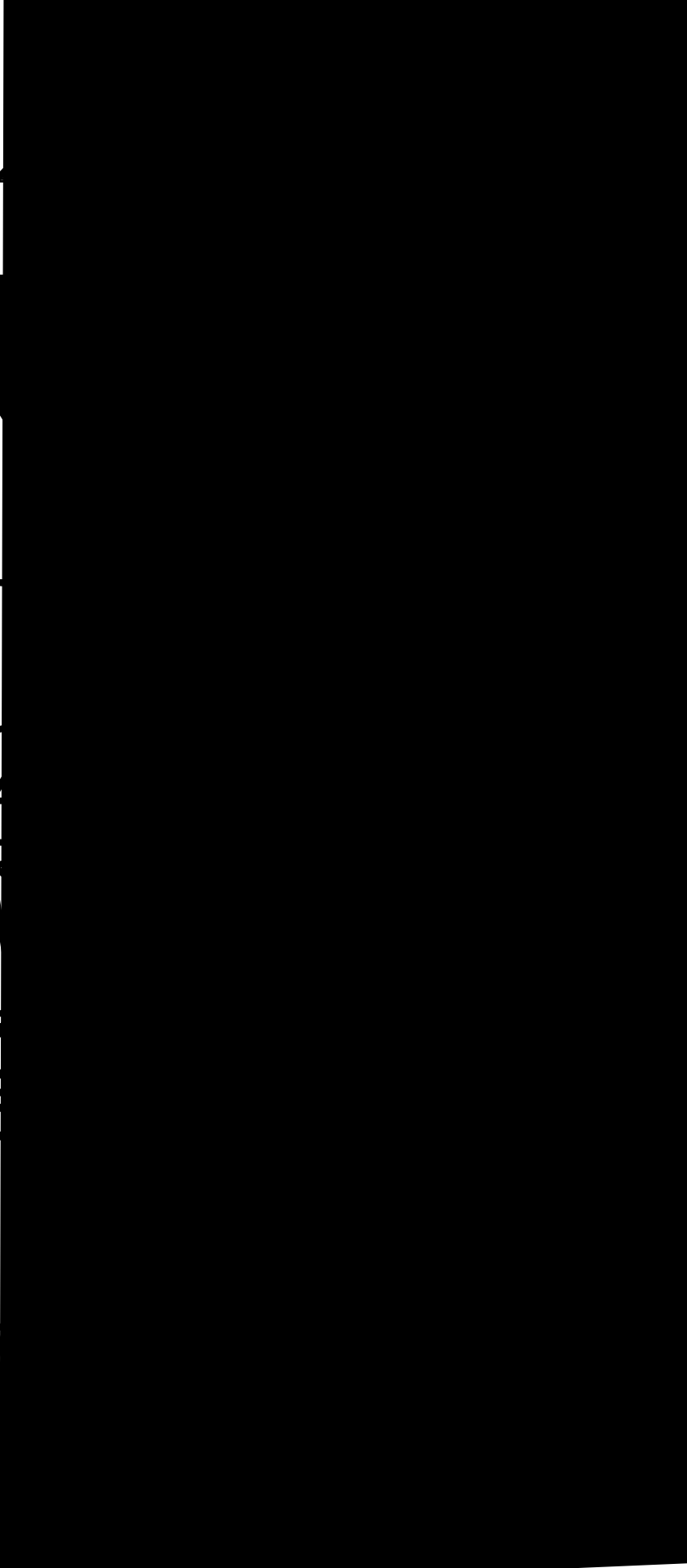
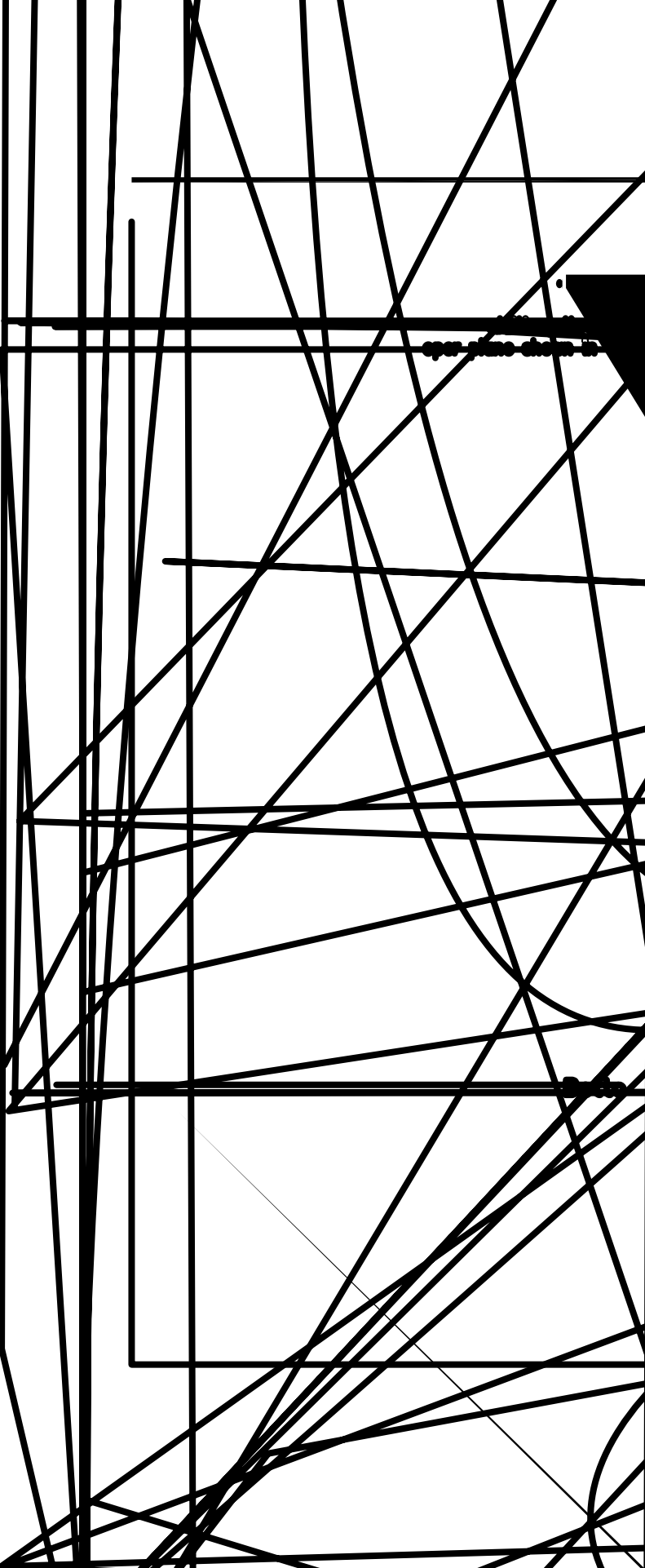


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24314CDSGR	WSON	DSG	8	3000	367.0	367.0	35.0
BQ24314CDSGT	WSON	DSG	8	250	210.0	185.0	35.0



- B. This drawing is subject to change with
- C. Quad FI
- ⚠ The package thermal pad must be soldered to the board for thermal and mechanical performance.
  - c thermal pad dimensions.



open flame chain is

IN MEN'S  
[www.1.com](http://www.1.com)

PASS

JS

6x0,5

x0,

2,2

2,2

(Note F)

Pad Geometry  
(Note C)

0,8

4208774/E 11/10

Refer to Application Note,

specific thermal information, via requirements

also rounding corners will offer better paste release. Customers sh

rs should contact their board fabrication site for so

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