LM9830

LM9830 36-Bit Color Document Scanner

Literature Number: SNOS444B

November 1998

National Semiconductor™

LM9830 36-Bit Color Document Scanner

General Description

The LM9830 is a complete document scanner system on a single IC. The LM9830 provides all the functions (CCD control, illumination control, analog front end, pixel processing function image data buffer/SRAM controller, microstepping motor controller, and EPP parallel port interface) necessary to create a high performance color scanner. The LM9830 scans images in 36 bit color, and has output data formats for 36 bits, 30 bits, and 24 bits.

The only additional active components required are an external SRAM for data buffering and power transistors for the stepper motor. Parallel port pass-through requires two additional TTL/CMOS logic ICs.

Applications

- Color Flatbed Document Scanners
- Color Sheetfed Document Scanners

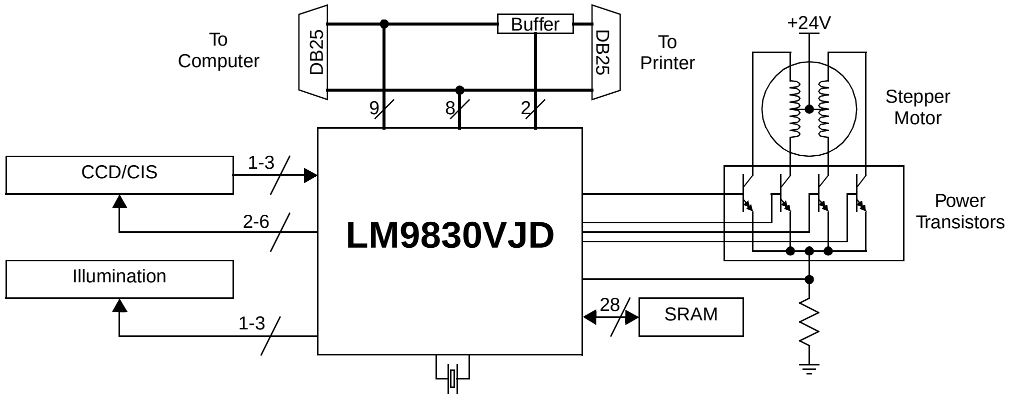
Features

- Scans at up to 6Mpixels/s (2M RGB pixels/sec).
- Digital Pixel Processing provides 300, 200, 150, 100, 75, and 50 dpi horizontal resolution from 300dpi sensor, and 600, 400, 300, 200, 150, 100, 75, and 50 dpi horizontal resolution from a 600dpi sensor.
- Provides 50-600dpi vertical resolution in 1 dpi increments.
- Pixel rate error correction for gain (shading) and offset errors.
- Output formats include 12 bit linear, 10 bit linear with shading and offset, or 8 bit gamma corrected, all with 12 bit accuracy.
- Multiple CCD clocking rates allows matching of CCD clock to scan resolution and pixel depth for maximum scan speed.
- Stepper motor control tightly coupled with buffer management to maximize data transfer efficiency.
- PWM stepper motor current control allows microstepping for the price of fullstepping.
- Supports 64k, 128k, or 256k x8 external SRAMs.
- Parallel Port interface supports EPP, PS2 (bidirectional), or SPP (nibble) modes of operation.
- Pixel depths of 1, 2, or 4 bits are packed into bytes for faster scans of line art and low pixel depth images.
- Supports 1 and 3 channel CIS and CCD devices.
- 3 (R, G, and B) user-programmable gamma correction tables.
- Able to transmit an arbitrary range of pixels to speed up scanning of smaller items (business cards, etc.) by zooming in on a subset of CCD pixels.
- Compatible with a wide range of color linear CCDs and Contact Image Sensors (CIS)
- Internal bandgap voltage reference.
- 100 pin TQFP package

Key Specifications

Analog to Digital Converter Resolution	12 Bits
Maximum Pixel Conversion Rate	6MHz
A4 Color 150dpi scan (typical, EPP Interface)	<10 seconds
A4 Color 300dpi scan (typical, EPP Interface)	<40 seconds
A4 Color 600dpi scan (typical, EPP Interface)	<160 seconds
Supply Voltage	+5V±10%
Power Dissipation (typical)	350mW

Scanner Block Diagram



Ordering Information

Commercial (0°C ≤ T_A ≤ +70°C)	Package
LM9830VJD	VJD100A 100 Pin Thin Quad Flatpac
LM9830VJDX	VJD100A 100 Pin Thin Quad Flatpac, Tape & Reel

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Absolute Maximum Ratings (Notes 1 & 2)

Positive Supply Voltage ($V^+=V_A=V_D=V_{DI/O}=V_{SRAM}$) With Respect to $GND=AGND=DGND=DGND_{I/O}=DGND_{SRAM}$	6.5V
Voltage On Any Input or Output Pin	-0.3V to V^++0.3V
Input Current at any pin (Note 3)	±25mA
Package Input Current (Note 3)	±50mA
Package Dissipation at T_A = 25°C	(Note 4)
ESD Susceptibility (Note 5)	
Human Body Model	1000V
Soldering Information	
Infrared, 10 seconds (Note 6)	235°C
Storage Temperature	-65°C to +150°

Operating Ratings (Notes 1 & 2)

Operating Temperature Range	$T_{MIN} \le T_A \le T_{MAX}$
LM9830VJD	$0°C \le T_A \le +70°C$
V_A Supply Voltage	+4.5V to +5.5V
V_D Supply Voltage	+4.5V to +5.5V
$V_{DI/O}$ Supply Voltage	+4.5V to +5.5V
$\|V_A-V_D\|$, $\|V_A-V_{DI/O}\|$, $\|V_A-V_{SRAM}\|$, $\|V_D-V_{DI/O}\|$, $\|V_D-V_{SRAM}\|$, $\|V_{DI/O}-V_{SRAM}\|$,	≤ 100mV
Input Voltage Range	-0.05V to V^+ + 0.05V

Electrical Characteristics

The following specifications apply for $AGND=DGND=DGND_{I/O}=DGND_{SRAM}=0V$, $V_A=V_D=V_{DI/O}=V_{SRAM}=+5.0V_{DC}$, $f_{CRYSTAL\ IN}$= 50MHz. **Boldface limits apply for $T_A=T_J=T_{MIN}$ to T_{MAX}**; all other limits $T_A=T_J$=25°C. (Notes 7, 8, & 12)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CCD/CIS Source Requirements for Full Specified Accuracy and Dynamic Range (Note 12)					
$V_{OS\ PEAK}$	Sensor's Maximum Output Signal Amplitude before LM9830 Analog Front End Saturation	Gain = 0.933 Gain = 3.0 Gain = 9.0	2.1 0.65 0.21		V V V
Full Channel Characteristics					
	Resolution with No Missing Codes			**12**	bits (min)
INL	Integral Non-Linearity Error (Note 11)		-1.1 +4.6	**-7** **+10**	LSB (min) LSB (max)
DNL	Differential Non-Linearity		-0.5 +0.7	**-0.9** **+2.0**	LSB (min) LSB (max)
C	Analog Channel Gain Constant (ADC Codes/V)	Includes voltage reference variation, gain setting = 1	2048	**1863** **2129**	LSB (min) LSB (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CCD Mode		4	**-21** **+34**	mV (min) mV (max)
V_{OS1}	Pre-Boost Analog Channel Offset Error, CIS Mode		12	**-15** **+38**	mV (min) mV (max)
V_{OS2}	Pre-PGA Analog Channel Offset Error		-30	**-58** **+8**	mV (min) mV (max)
V_{OS3}	Post-PGA Analog Channel Offset Error		-21	**-59** **+14**	mV (min) mV (max)
Coarse Color Balance PGA Characteristics (Configuration Registers 3B, 3C, and 3D)					
	Monotonicity			**5**	bits (min)
	G_0 (Minimum PGA Gain)	PGA Setting = 0	0.93	**.90** **.96**	V/V (min) V/V (max)
	G_{31} (Maximum PGA Gain)	PGA Setting = 31	3.05	**2.98** **3.15**	V/V (min) V/V (max)
	x3 Boost Gain	x3 Boost Setting On (bit B5 of Gain Register is set)	2.99	**2.86** **3.08**	V/V (min) V/V (max)
	Gain Error at any gain (Note 13)		±0.2	**±1.6**	% (max)

Electrical Characteristics (Continued)

The following specifications apply for $AGND=DGND=DGND_{I/O}=DGND_{SRAM}=0V$, $V_A=V_D=V_{DI/O}=V_{SRAM}=+5.0V_{DC}$, $f_{CRYSTAL\ IN}= 50MHz$. **Boldface limits apply for $T_A=T_J=T_{MIN}$ to T_{MAX}**; all other limits $T_A=T_J=25°C$. (Notes 7, 8, & 12)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Static Offset DAC Characteristics (Configuration Registers 38, 39, and 3A)					
	Monotonicity			**6**	bits (min)
	Offset DAC LSB size	PGA gain = 1	9.3	**5.8** **12.7**	mV (min) mV (max)
	Offset DAC Adjustment Range	PGA gain = 1	±290	**±270**	mV (min)
Analog Input Characteristics					
	Average OS_R, OS_G, OS_B Input Current	CDS Enabled, OS = $3.5V_{DC}$	±80		nA
	OS_R, OS_G, OS_B Input Current	CDS Disabled, OS = $3.5V_{DC}$	±24	**±30**	µA (max)
Internal Voltage Reference Characteristics					
$V_{BANDGAP}$	Voltage Reference Output Voltage		1.2		V
$V_{REF\ LO}$	Negative Reference Output Voltage		$V_{REF\ MID}-1.0$		V
$V_{REF\ MID}$	Midpoint Reference Output Voltage		$V_A/2.0$		V
$V_{REF\ HI}$	Positive Reference Output Voltage		$V_{REF\ MID}+1.0$		V

DC and Logic Electrical Characteristics

The following specifications apply for $AGND=DGND=DGND_{I/O}=DGND_{SRAM}=0V$, $V_A=V_D=V_{DI/O}=V_{SRAM}=+5.0V_{DC}$, $f_{CRYSTAL\ IN}= 50MHz$. **Boldface limits apply for $T_A=T_J=T_{MIN}$ to T_{MAX}**; all other limits $T_A=T_J=25°C$. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Digital Input Characteristics for DB0-DB7, D0-D7, $\overline{\text{STROBE}}$, $\overline{\text{AUTOFEED}}$, $\overline{\text{INIT}}$, $\overline{\text{SELECT IN}}$, PSENSE#1, PSENSE#2, MISC I/O #1, MISC I/O #2, CMODE					
$V_{IN(1)}$	Logical “1” Input Voltage	$V_{DI/O}=5.5V$		**2.0**	V (min)
$V_{IN(0)}$	Logical “0” Input Voltage	$V_{DI/O}=4.5V$		**0.8**	V (max)
I_{IN}	Input Leakage Current		±500		nA
C_{IN}	Input Capacitance		5		pF
Digital Output Characteristics for DB0-DB7, A0-A17, $\overline{\text{RD}}$, $\overline{\text{WR}}$ (SRAM Interface)					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{DI/O}=4.5V$, $I_{OUT}=-4mA$		**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{DI/O}=5.5V$, $I_{OUT}=8mA$		**0.4**	V (max)
Digital Output Characteristics for D0-D7, $\overline{\text{ERROR}}$, $\overline{\text{ACK}}$, BUSY, PE, SELECT (Parallel Port Interface)					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{DI/O}=4.5V$, $I_{OUT}=-4mA$		**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{DI/O}=5.5V$, $I_{OUT}=14mA$		**0.4**	V (max)
Digital Output Characteristics for MISC I/O #1, MISC I/O #2, A, B, $\overline{\text{A}}$, $\overline{\text{B}}$, TR1, TR2, ø1, ø2, RS, CP1, CP2, TRISTATE, $\overline{\text{LATCH}}$, $LAMP_R$, $LAMP_G$, $LAMP_B$					
$V_{OUT(1)}$	Logical “1” Output Voltage	$V_{DI/O}=4.5V$, $I_{OUT}=-4mA$		**2.4**	V (min)
$V_{OUT(0)}$	Logical “0” Output Voltage	$V_{DI/O}=5.5V$, $I_{OUT}=8mA$		**0.4**	V (max)

DC and Logic Electrical Characteristics

The following specifications apply for AGND=DGND=$DGND_{I/O}$=$DGND_{SRAM}$=0V, V_A=V_D=$V_{DI/O}$=V_{SRAM}=+5.0V_{DC}, $f_{CRYSTAL\ IN}$= 50MHz. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
CRYSTAL IN, CRYSTAL OUT Characteristics					
$XTAL_{OUT\ DC}$	CRYSTAL OUT Bias Level (Offset)		0.8		V
$XTAL_{OUT\ AC}$	CRYSTAL OUT Amplitude	$f_{CRYSTAL}$ = 50MHz	0.8		V_{P-P}
Power Supply Characteristics					
I_A	Analog Supply Current (V_A pins)	Operating Standby	64 0.75	**83** **0.95**	mA (max) mA (max)
$I_{D\ I/O}$	Digital I/O Supply Current ($V_{D\ I/O}$, V_D, and V_{SRAM} pins)	Operating Standby	40 5	**48** **6.5**	mA (max) mA (max)

AC Electrical Characteristics

The following specifications apply for AGND=DGND=$DGND_{I/O}$=$DGND_{SRAM}$=0V, V_A=V_D=$V_{DI/O}$=V_{SRAM}=+5.0V_{DC}, $f_{CRYSTAL\ IN}$= 50MHz, MCLK DIVIDER = 1.0 (unless otherwise noted), f_{MCLK} = $f_{CRYSTAL\ IN}$/MCLK DIVIDER, $f_{ADC\ CLK}$ = f_{MCLK}/8, C_L (databus loading) = 20pF/pin. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
		Parallel Port Address Write (Figure 1)			
t_{SETUP1}	D0-D7 (Address) valid to $\overline{\text{SELECT IN}}$ falling		-60	**-10**	ns (min)
t_{SETUP2}	$\overline{\text{STROBE}}$ falling edge to $\overline{\text{SELECT IN}}$ falling		-15	**-10**	ns (min)
$t_{\overline{SI}-B1}$	$\overline{\text{SELECT IN}}$ falling to BUSY rising		25	**40**	ns (max)
$t_{B-\overline{SI}}$	BUSY rising to $\overline{\text{SELECT IN}}$ rising		0	**20**	ns (min)
t_{HOLD1}	$\overline{\text{SELECT IN}}$ rising to $\overline{\text{STROBE}}$ rising		-45	**-15**	ns (min)
$t_{\overline{SI}-B2}$	$\overline{\text{SELECT IN}}$ rising to BUSY falling		33	**50**	ns (max)
t_{HOLD2}	D0-D7 (Address) hold time after BUSY falling		-10	**0**	ns (min)
		Parallel Port Data Write (Figure 2)			
t_{SETUP1}	D0-D7 valid or $\overline{\text{STROBE}}$ falling to $\overline{\text{SELECT IN}}$ falling		-60	**-10**	ns (min)
t_{SETUP2}	$\overline{\text{STROBE}}$ falling to $\overline{\text{AUTOFEED}}$ falling		-25	**-10**	ns (min)
$t_{\overline{AF}-B1}$	$\overline{\text{AUTOFEED}}$ falling to BUSY rising		34	**50**	ns (max)
$t_{B-\overline{AF}1}$	BUSY rising to $\overline{\text{AUTOFEED}}$ rising		0	**20**	ns (min)
t_{HOLD1}	$\overline{\text{AUTOFEED}}$ rising to $\overline{\text{STROBE}}$ rising		-40	**-10**	ns (min)
$t_{\overline{AF}-B2}$	$\overline{\text{AUTOFEED}}$ rising to BUSY falling	All Except Dataport Dataport	16 1.5 $t_{ADC\ CLK}$	**35** **3 $t_{ADC\ CLK}$**	ns (max) ns (max)
t_{HOLD2}	D0-D7 valid after BUSY falling		-10	**0**	ns (min)

AC Electrical Characteristics

The following specifications apply for AGND=DGND=$\text{DGND}_{\text{I/O}}$=$\text{DGND}_{\text{SRAM}}$=0V, V_A=V_D=$V_{\text{DI/O}}$=V_{SRAM}=+5.0V_{DC}, $f_{\text{CRYSTAL IN}}$= 50MHz, MCLK DIVIDER = 1.0 (unless otherwise noted), f_{MCLK} = $f_{\text{CRYSTAL IN}}$/MCLK DIVIDER, $f_{\text{ADC CLK}}$ = f_{MCLK}/8, C_L (databus loading) = 20pF/pin. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
Parallel Port 8 Bit Data Read (Figure 3)					
$t_{\overline{\text{AF}}\text{-B3}}$	$\overline{\text{AUTOFEED}}$ falling to BUSY rising	All Except Dataport Dataport	25 1.5 $t_{\text{ADC CLK}}$	**45** **3 $t_{\text{ADC CLK}}$**	ns (max) ns (max)
$t_{\text{EPP ACCESS}}$	D0-D7 valid before BUSY rising	(Note 14)	7	**-5**	ns (min)
$t_{\text{B-}\overline{\text{AF}}\text{2}}$	BUSY rising to $\overline{\text{AUTOFEED}}$ rising		1	**10**	ns (min)
$t_{\text{EPP HOLD}}$	$\overline{\text{AUTOFEED}}$ rising to D0-D7 Tri-State		20	**10** **27**	ns (min) ns (max)
$t_{\overline{\text{AF}}\text{-B4}}$	$\overline{\text{AUTOFEED}}$ rising to BUSY falling		3 t_{MCLK}	**4 t_{MCLK}**	ns (max)
Nibble Data Read (Figure 4)					
$t_{\overline{\text{AF}}\text{-B3}}$	$\overline{\text{AUTOFEED}}$ falling to BUSY rising	All Except Dataport Dataport	25 1.5 $t_{\text{ADC CLK}}$	**45** **3 $t_{\text{ADC CLK}}$**	ns (max) ns (max)
$t_{\text{NIB ACCESS1}}$	D4-D7 valid before BUSY rising		2	**-20**	ns (min)
$t_{\text{B-}\overline{\text{AF}}\text{2}}$	BUSY rising to $\overline{\text{AUTOFEED}}$ rising		1	**10**	ns (min)
$t_{\text{NIB ACCESS2}}$	D0-D3 valid after $\overline{\text{AUTOFEED}}$ rising		5	**15**	ns (max)
$t_{\overline{\text{AF}}\text{-B4}}$	$\overline{\text{AUTOFEED}}$ rising edge to BUSY falling		3 t_{MCLK}	**4 t_{MCLK}**	ns (max)
Microprocessor Mode (Figures 5, 6, and 7)					
$t_{\text{ALE SETUP}}$	D0-D7 (Address) valid before ALE falling		0	**6**	ns (min)
$t_{\text{ALE HOLD}}$	D0-D7 (Address) valid after ALE falling		2	**8**	ns (min)
t_{ALE}	ALE high time		2	**8**	ns (min)
$t_{\text{ALE-R/W}}$	ALE falling to $\overline{\text{CS}}$/$\overline{\text{RD}}$/$\overline{\text{WR}}$ falling (next operation)			**16**	ns (min)
$t_{\overline{\text{WR}}\text{ SETUP}}$	D0-D7 valid before $\overline{\text{WR}}$ rising		0	**6**	ns (min)
$t_{\overline{\text{WR}}\text{ HOLD}}$	D0-D7 valid after $\overline{\text{WR}}$ rising		2	**10**	ns (min)
$t_{\overline{\text{WR}}}$	$\overline{\text{WR}}$ pulse width		3	**10**	ns (min)
$t_{\overline{\text{RD}}\text{ ACCESS}}$	$\overline{\text{RD}}$ low to D0-D7 valid		22	**31**	ns (max)
$t_{\overline{\text{RD}}\text{ TRI-STATE}}$	$\overline{\text{RD}}$ high to D0-D7 Tri-State		20	**28**	ns (max)

AC Electrical Characteristics

The following specifications apply for AGND=DGND=$DGND_{I/O}$=$DGND_{SRAM}$=0V, V_A=V_D=$V_{DI/O}$=V_{SRAM}=+5.0V_{DC}, $f_{CRYSTAL\ IN}$= 50MHz, MCLK DIVIDER = 1.0 (unless otherwise noted), f_{MCLK} = $f_{CRYSTAL\ IN}$/MCLK DIVIDER, $f_{ADC\ CLK}$ = f_{MCLK}/8, C_L (databus loading) = 20pF/pin. **Boldface limits apply for T_A=T_J=T_{MIN} to T_{MAX}**; all other limits T_A=T_J=25°C. (Notes 7 & 8)

Symbol	Parameter	Conditions	Typical (Note 9)	Limits (Note 10)	Units (Limits)
SRAM Write Timing (Figure 8) - Typical Values Represent Worst Case Timing for Different MCLK Frequencies					
$t_{\overline{WR}\text{ F ADDR SETUP}}$	Address valid to $\overline{WR}$ falling		0.5 t_{MCLK} - 7ns	**3**	ns (min)
$t_{\overline{WR}\text{ R ADDR SETUP}}$	Address valid to $\overline{WR}$ rising		1.5 t_{MCLK} - 9ns	**21**	ns (min)
$t_{\overline{WR}\text{ DATA SETUP}}$	DB0-DB7 valid to $\overline{WR}$ rising		1 t_{MCLK} - 9ns	**11**	ns (min)
$t_{\overline{WR}}$	$\overline{WR}$ pulse width		1 t_{MCLK} - 5ns	**15**	ns (min)
$t_{\overline{WR}\text{ ADDR HOLD}}$	$\overline{WR}$ rising to Address data change		0.33 t_{MCLK} - 4ns	**2**	ns (min)
$t_{\overline{WR}\text{ DATA HOLD}}$	$\overline{WR}$ rising to DB0-DB7 data Tri-State		1	**4**	ns (max)
SRAM Read Timing (Figure 9) - Typical Values Represent Worst Case Timing for Different MCLK Frequencies					
$t_{\overline{RD}\text{ SETUP}}$	Address valid to DB0-DB7 data valid	4 slot mode	2 t_{MCLK} - 12ns	**28**	ns (max)
		8 slot mode (f_{MCLK} = 25MHz)	1 t_{MCLK} - 12ns		

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.

Note 2: All voltages are measured with respect to GND=AGND=DGND=$DGND_{I/O}$=$DGND_{SRAM}$=0V, unless otherwise specified.

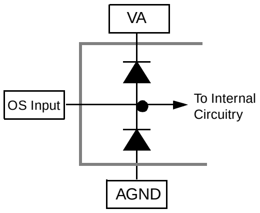
Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supplies (V_{IN}<GND or V_{IN}>V_A or V_D), the current at that pin should be limited to 25mA. The 50mA maximum package input current rating limits the number of pins that can simultaneously safely exceed the power supplies with an input current of 25mA to two.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by $T_J$max, Θ_{JA} and the ambient temperature, T_A. The maximum allowable power dissipation at any temperature is P_D = ($T_J$max - T_A) / Θ_{JA}. $T_J$max = 150°C for this device. The typical thermal resistance (Θ_{JA}) of this part when board mounted is 53°C/W.

Note 5: Human body model, 100pF capacitor discharged through a 1.5kΩ resistor.

Note 6: See AN450 “Surface Mounting Methods and Their Effect on Product Reliability” or the section titled “Surface Mount” found in any National Semiconductor Linear Data Book for other methods of soldering surface mount devices.

Note 7: Two diodes clamp the OS analog inputs to AGND and VA as shown below. This input protection, in combination with the external clamp capacitor and the output impedance of the sensor, prevents damage to the LM9830 from transients during power-up.



Note 8: For best performance, it is required that all supply pins be powered from the same power supply with separate bypass capacitors at each supply pin.

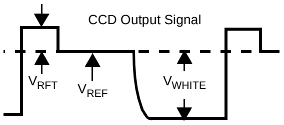
Note 9: Typicals are at T_J=T_A=25°C, $f_{CRYSTAL\ IN}$ = 50MHz, and represent most likely parametric norm.

Note 10: Tested limits are guaranteed to National's AOQL (Average Outgoing Quality Level).

Note 11: Integral linearity error is defined as the deviation of the analog value, expressed in LSBs, from the straight line that best fits the actual transfer function of the ADC.

Note 12: V_{REF} is defined as the CCD OS voltage for the reference period following the reset feedthrough pulse. V_{WHITE} is defined as the peak CCD pixel output voltage for a white (full scale) image with respect to the reference level, V_{REF} . V_{RFT} is defined as the peak positive deviation above V_{REF} of the reset feedthrough pulse. The maximum correctable range of pixel-to-pixel V_{WHITE} variation is defined as the maximum variation in V_{WHITE} (due to PRNU, light source intensity variation, optics, etc.) that the

LM9830 can correct for using its internal PGA.



Note 13: PGA Gain Error is the maximum difference between the measured gain for any PGA code and the ideal gain calculated by using the formula $\mathrm{Gain}_{PGA}\left(\frac{V}{V}\right) = G_0 + X\frac{\text{PGA code}}{32}$ where $X = (G_{31} - G_0)\frac{32}{31}$.

Note 14: Interaction with an actual parallel port load (C_{LOAD} > 200pF) can increase data settling time by as much as 100ns if the parallel port databus is precharged high. For this reason, it is recommended that the parallel port be driven to 0x00h by the PC when not in the reverse transfer phase. When reading coefficient data from register 6 (register 3 = 00000XX1 binary), the EPP handshaking generated by the host PC may be faster than the data can settle. For this reason it is recommended that software handshaking (“PS2” mode) be used when verifying coefficient data.

Timing Diagrams

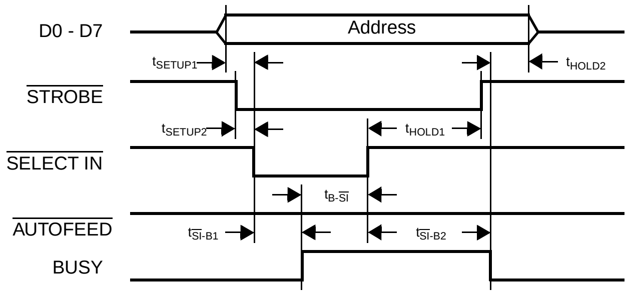

D0 - D7
Address
t_{SETUP1}
t_{HOLD2}
$\overline{STROBE}$
t_{SETUP2}
t_{HOLD1}
$\overline{SELECT\ IN}$
$t_{B\text{-}\overline{SI}}$
$\overline{AUTOFEED}$
$t_{\overline{SI}\text{-}B1}$
$t_{\overline{SI}\text{-}B2}$
BUSY

Figure 1: Parallel Port Address Write

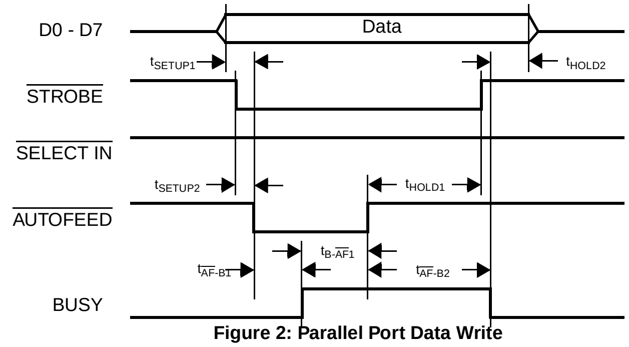

D0 - D7
Data
t_{SETUP1}
t_{HOLD2}
$\overline{STROBE}$
$\overline{SELECT\ IN}$
t_{SETUP2}
t_{HOLD1}
$\overline{AUTOFEED}$
$t_{B\text{-}\overline{AF}1}$
$t_{\overline{AF}\text{-}B1}$
$t_{\overline{AF}\text{-}B2}$
BUSY

Figure 2: Parallel Port Data Write

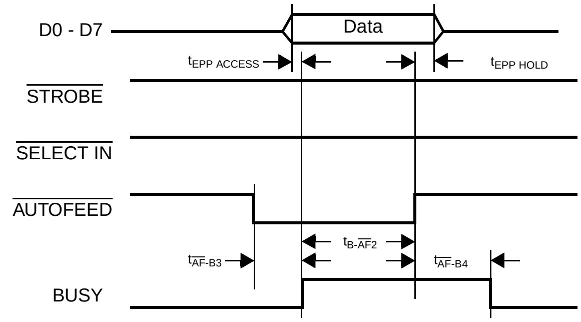

D0 - D7
Data
$t_{EPP\ ACCESS}$
$t_{EPP\ HOLD}$
$\overline{STROBE}$
$\overline{SELECT\ IN}$
$\overline{AUTOFEED}$
$t_{B\text{-}\overline{AF}2}$
$t_{\overline{AF}\text{-}B3}$
$t_{\overline{AF}\text{-}B4}$
BUSY

Figure 3: Parallel Port 8 Bit Data Read

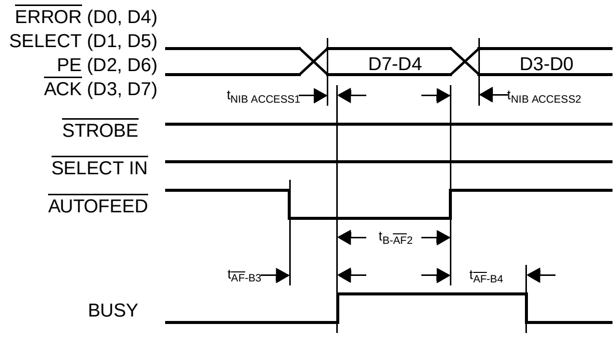

$\overline{ERROR}$ (D0, D4)
SELECT (D1, D5)
PE (D2, D6)
$\overline{ACK}$ (D3, D7)
D7-D4
D3-D0
$t_{NIB\ ACCESS1}$
$t_{NIB\ ACCESS2}$
$\overline{STROBE}$
$\overline{SELECT\ IN}$
$\overline{AUTOFEED}$
$t_{B\text{-}\overline{AF}2}$
$t_{\overline{AF}\text{-}B3}$
$t_{\overline{AF}\text{-}B4}$
BUSY

Figure 4: Parallel Port Nibble Data Read

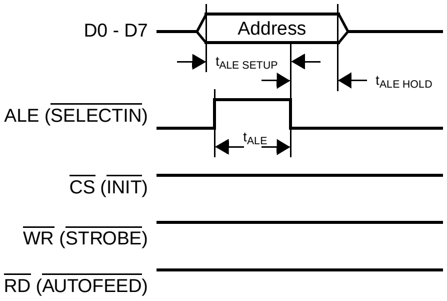
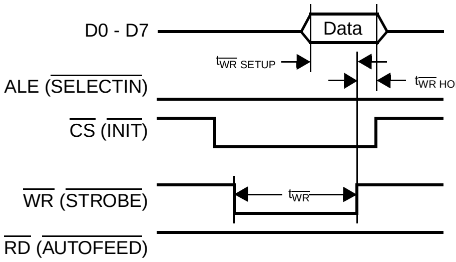
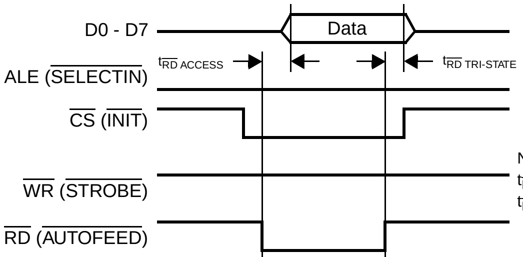

D0 - D7
Address
$t_{ALE\ SETUP}$
$t_{ALE\ HOLD}$
ALE ($\overline{\text{SELECTIN}}$)
t_{ALE}
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
$\overline{\text{WR}}$ ($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$ ($\overline{\text{AUTOFEED}}$)

Figure 5: μP Mode Address Latch


D0 - D7
Data
$t_{\overline{WR}\ SETUP}$
$t_{\overline{WR}\ HOLD}$
ALE ($\overline{\text{SELECTIN}}$)
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
$\overline{\text{WR}}$ ($\overline{\text{STROBE}}$)
$t_{\overline{WR}}$
$\overline{\text{RD}}$ ($\overline{\text{AUTOFEED}}$)

NOTE: $\overline{\text{CS}}$ and $\overline{\text{WR}}$ are ORed together.
$t_{\overline{WR}\ SETUP}$ and $t_{\overline{WR}\ HOLD}$ refer to the first rising edge of $\overline{\text{CS}}$ or $\overline{\text{WR}}$, whichever goes high first.

Figure 6: μP Mode Write


D0 - D7
Data
$t_{\overline{RD}\ ACCESS}$
$t_{\overline{RD}\ TRI\text{-}STATE}$
ALE ($\overline{\text{SELECTIN}}$)
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
$\overline{\text{WR}}$ ($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$ ($\overline{\text{AUTOFEED}}$)

NOTE: $\overline{\text{CS}}$ and $\overline{\text{RD}}$ are ORed together.
$t_{\overline{RD}\ ACCESS}$ begins when both $\overline{\text{CS}}$ and $\overline{\text{WR}}$ go low.
$t_{\overline{RD}\ TRI\text{-}STATE}$ begins when either $\overline{\text{CS}}$ or $\overline{\text{WR}}$ go high

Figure 7: μP Mode Read

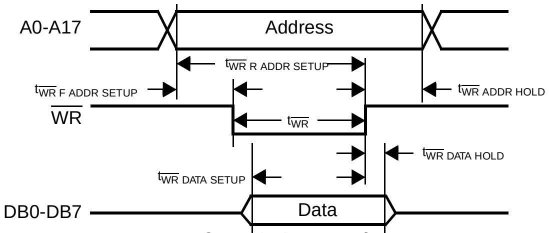
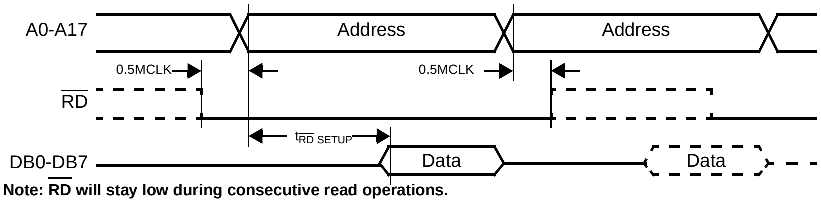

A0-A17
Address
$t_{\overline{WR}\ R\ ADDR\ SETUP}$
$t_{\overline{WR}\ F\ ADDR\ SETUP}$
$t_{\overline{WR}\ ADDR\ HOLD}$
$\overline{\text{WR}}$
$t_{\overline{WR}}$
$t_{\overline{WR}\ DATA\ HOLD}$
$t_{\overline{WR}\ DATA\ SETUP}$
DB0-DB7
Data

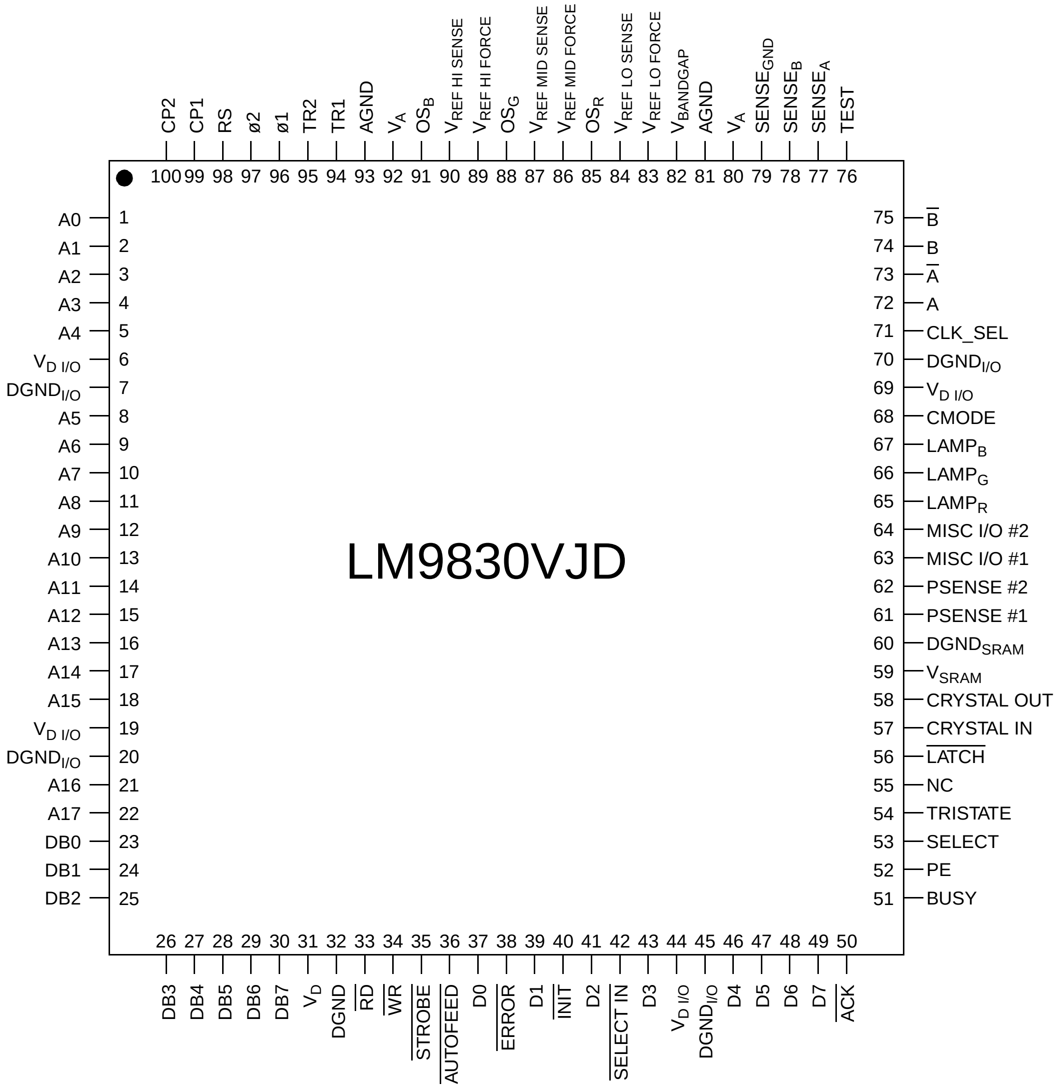
Figure 8: SRAM Write


A0-A17
Address
Address
0.5MCLK
0.5MCLK
$\overline{\text{RD}}$
$t_{\overline{RD}\ SETUP}$
DB0-DB7
Data
Data

Note: $\overline{\text{RD}}$ will stay low during consecutive read operations.

Figure 9: SRAM Read

Connection Diagram


LM9830VJD
1 A0
2 A1
3 A2
4 A3
5 A4
6 $V_{D\ I/O}$
7 $DGND_{I/O}$
8 A5
9 A6
10 A7
11 A8
12 A9
13 A10
14 A11
15 A12
16 A13
17 A14
18 A15
19 $V_{D\ I/O}$
20 $DGND_{I/O}$
21 A16
22 A17
23 DB0
24 DB1
25 DB2
26 DB3
27 DB4
28 DB5
29 DB6
30 DB7
31 V_D
32 DGND
33 $\overline{RD}$
34 $\overline{WR}$
35 $\overline{STROBE}$
36 $\overline{AUTOFEED}$
37 D0
38 $\overline{ERROR}$
39 D1
40 $\overline{INIT}$
41 D2
42 $\overline{SELECT\ IN}$
43 D3
44 $V_{D\ I/O}$
45 $DGND_{I/O}$
46 D4
47 D5
48 D6
49 D7
50 $\overline{ACK}$
51 BUSY
52 PE
53 SELECT
54 TRISTATE
55 NC
56 $\overline{LATCH}$
57 CRYSTAL IN
58 CRYSTAL OUT
59 V_{SRAM}
60 $DGND_{SRAM}$
61 PSENSE #1
62 PSENSE #2
63 MISC I/O #1
64 MISC I/O #2
65 $LAMP_R$
66 $LAMP_G$
67 $LAMP_B$
68 CMODE
69 $V_{D\ I/O}$
70 $DGND_{I/O}$
71 CLK_SEL
72 A
73 $\overline{A}$
74 B
75 $\overline{B}$
76 TEST
77 $SENSE_A$
78 $SENSE_B$
79 $SENSE_{GND}$
80 V_A
81 AGND
82 $V_{BANDGAP}$
83 $V_{REF\ LO\ FORCE}$
84 $V_{REF\ LO\ SENSE}$
85 OS_R
86 $V_{REF\ MID\ FORCE}$
87 $V_{REF\ MID\ SENSE}$
88 OS_G
89 $V_{REF\ HI\ FORCE}$
90 $V_{REF\ HI\ SENSE}$
91 OS_B
92 V_A
93 AGND
94 TR1
95 TR2
96 ø1
97 ø2
98 RS
99 CP1
100 CP2

Pin Descriptions

CCD Driver Signals

ø1	Digital Output. CCD/CIS clock signal, phase 1.
ø2	Digital Output. CCD clock signal, phase 2.
RS	Digital Output. Reset pulse for the CCD.
CP1	Digital Output. Clamp pulse for the CCD.
CP2	Digital Output. Clamp pulse for the CCD.
TR1, TR2	Digital Outputs. Transfer pulses for the CCD(CIS).

Analog I/O

OS_R, OS_G, OS_B	Analog Inputs. These inputs (for Red, Green, and Blue) should be tied to the sensor's output signal through DC blocking capacitors.
$V_{REF\ LO\ FORCE}$, $V_{REF\ LO\ SENSE}$	Analog Output/Input. Connect $V_{REF\ LO\ OUT}$ to $V_{REF\ LO\ IN}$ and bypass to AGND with a 0.05µF monolithic capacitor.
$V_{REF\ MID\ FORCE}$, $V_{REF\ MID\ SENSE}$	Analog Output/Input. Connect $V_{REF\ MID\ OUT}$ to $V_{REF\ MID\ IN}$ and bypass to AGND with a 0.05µF monolithic capacitor.
$V_{REF\ HI\ FORCE}$, $V_{REF\ HI\ SENSE}$	Analog Output/Input. Connect $V_{REF\ HI\ OUT}$ to $V_{REF\ HI\ IN}$ and bypass to AGND with a 0.05µF monolithic capacitor.
$V_{BANDGAP}$	Analog Output. Bypass to AGND with a 0.05µF monolithic capacitor.

General Digital I/O

CRYSTAL IN	Digital Input. This is the 50MHz (typical) master system clock.
CRYSTAL OUT	Digital Output. Used with CRYSTAL IN and an external crystal to form a crystal oscillator.
CLK_SEL	Digital Input. Should be tied to DGND for operation with an external crystal. To use an external TTL or CMOS clock source, tie CLK_SEL to $V_{D\ I/O}$ and drive the clock into the CRYSTAL OUT pin.

PC I/O

D0 (LSB) -D7 (MSB)	Digital Inputs/Outputs. This is the 8 bit data path between the LM9830 and the host computer.
$\overline{\text{STROBE}}$	Digital Input. $\overline{\text{WR}}$ signal in µP Mode.
$\overline{\text{AUTOFEED}}$	Digital Input. $\overline{\text{RD}}$ signal in µP Mode.
$\overline{\text{SELECTIN}}$	Digital Input. ALE signal in µP Mode.
$\overline{\text{INIT}}$	Digital Input. $\overline{\text{CS}}$ signal in µP Mode.
$\overline{\text{ACK}}$	Digital Output.
BUSY	Digital Output.
PE	Digital Output.
SELECT	Digital Output.
$\overline{\text{ERROR}}$	Digital Output.

Printer Passthrough

TRISTATE	Digital Output. Low when in printer passthrough mode, high when the LM9830 is active. Low when no power is applied to the LM9830.
$\overline{\text{LATCH}}$	Digital Output. High when in printer passthrough mode, low when the LM9830 is active. Tri-state when no power is applied to the LM9830.

Stepper Motor I/O

A, B, $\overline{\text{A}}$, $\overline{\text{B}}$	Digital Outputs. Pulses to stepper motor.
$SENSE_A$, $SENSE_B$	Analog Inputs. Current sensing for PWM winding current control.
$SENSE_{GND}$	Analog Input. Ground sense input for PWM winding current control.

Scanner Support I/O

PSense #1, PSense #2	Digital Inputs. Programmable, used for sensing paper, front panel switches, etc.
Misc I/O #1, Misc I/O #2	Digital Inputs/Outputs. Programmable, used for front panel switches, status LEDs, etc.
$LAMP_R$, $LAMP_G$, $LAMP_B$	Digital Outputs. Used to control R, G, and B LEDs of single output CIS, as well as brightness of CCFL.

External RAM I/O

DB0 (LSB) - DB7 (MSB)	Digital Inputs/Outputs. This is the 8 bit data path between the external RAM and the LM9830.
A0-A17	Digital Outputs. Address pins for up to 256k bytes external RAM.
$\overline{\text{RD}}$	Digital Output. Read signal to external RAM.
$\overline{\text{WR}}$	Digital Output. Write signal to external RAM.

Communication Mode

CMODE	Digital Input. Tie to DGND to operate in parallel port mode, or to $V_{D\ I/O}$ to operate in microprocessor compatible mode.

Test

TEST	Analog Output. This pin can be used to view the Sample Signal, Sample Reference, and Clamp Signals.

Analog Power Supplies

V_A	This is the positive supply pin for the analog supply. It should be connected to a voltage source of +5V and bypassed to AGND with a 0.1µF monolithic capacitor in parallel with a 10µF tantalum capacitor.
AGND	This is the ground return for the analog supply.

Digital Power Supplies	
V_D	This is the positive supply pin for the LM9830's digital circuitry. It should be connected to a voltage source of +5V and bypassed to DGND with a 0.1µF monolithic capacitor.
DGND	This is the ground return for V_D.
$V_{D\ I/O}$	This is the positive supply pin for the LM9830's external I/O. It should be connected to a +5V voltage source and bypassed to the closest $DGND_{I/O}$ pin with a 0.1µF monolithic capacitor.
$DGND_{I/O}$	This is the ground return for $V_{D\ I/O}$.
V_{SRAM}	This is the positive supply pin for the LM9830's internal SRAM sense amplifiers and crystal oscillator. It should be connected to a +5V voltage source and bypassed to $DGND_{SRAM}$ with a 0.1µF monolithic capacitor.
$DGND_{SRAM}$	This is the ground return for $V_{D\ SRAM}$.
Other	
NC	Do Not Connect. This pin should be left floating.

LM9830 Register Listing

(Registers in bold boxes are reset to that value on power-up. All register addresses are in hexadecimal. All other numbers are decimal unless otherwise noted.)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
IMAGE BUFFER (READ ONLY)										
00	**Pixel (Image) Data**	n	n	n	n	n	n	n	n	One byte of image data.
STATUS REGISTERS (READ ONLY)										
01	**Image Data Available In Buffer**	n	n	n	n	n	n	n	n	n kbytes of image data available (always read this register twice to make sure its value was not changing while it was being read)
02	**Paper Sensor #1 State** If this input is edge sensitive, reading this Status Register will clear it.								0	False
									1	True
	Paper Sensor #2 State If this input is edge sensitive, reading this Status Register will clear it.							0		False
								1		True
	Misc I/O #1 State If this input is edge sensitive, reading this Status Register will clear it.						0			False
							1			True
	Misc I/O #2 State If this input is edge sensitive, reading this Status Register will clear it.					0				False
						1				True
	Pause This bit indicates whether or not the scanner is currently paused due to a buffer full condition.				0					Normal State
					1					The scanner entered the pause/reverse cycle during the processing of this line.
	Powerdrop This bit is used to detect if the power supply has dipped below 3V since the last time this register was read. Reading this register clears this bit.			0						False: Power has not dipped below 3V since the last time this register was read
				1						True: Power *has* dipped below 3V since the last time the register was read
DATAPORT REGISTERS										
03	**DataPort Target**								0	Gamma Lookup Table
									1	Offset/Gain Coefficient Data (external SRAM)
	DataPort Target Color (Note: If using 1 Channel Mode A, the color for the gamma table is selected by register 26, bits 3 and 4, not this register)						0	0		Red
							0	1		Green
							1	0		Blue
							1	1		N/A
04	**DataPort Address - MSB**			R/W	a	a	a	a	a	Address of location to be read/written to. a = 0 to 1023 for gamma tables, 0 to 2729 for Offset/Gain Coefficient Data (300dpi), 0 to 5459 for Offset/Gain Coefficient Data (600dpi). Addresses greater than these are illegal. Bit D5 of register 4 indicates whether next operation will be a Read (D5=1) or a Write (D5=0)
05	**DataPort Address - LSB**	a	a	a	a	a	a	a	a	
06	**DataPort**	n	n	n	n	n	n	n	n	Data to be read from or written to the address of the currently selected Dataport Target. The DataPort Address is automatically incremented whenever one (Gamma) or two (Offset/Gain Coefficient Data) bytes are read from or written to this register.

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
COMMAND REGISTER										
07	**Command Register** This register is used to start and end a scan. It is also used to home the sensor in a flatbed scanner or eject the image in a sheetfed scanner.							0	0	Idle - Stops motor (A, B, A, B = 0), completes current line of data (if scanning). Note: CCD/CIS clocks continue clocking.
								0	1	High Speed Forward - Moves motor forward at a speed determined by the Fast Feed Step Size (registers 48 and 49).
								1	0	High Speed Reverse - Moves motor backward at a speed determined by the Fast Feed Step Size (registers 48 and 49).
								1	1	Start Scan - Resets the LM9830's data pointers and starts an image scan.
	Standby When this bit is set the crystal oscillator continues to run but all internal clock signals are frozen. The analog circuitry is turned off to reduce power consumption.						0			Operating
							1			Low Power Standby Mode
	Reset (Host must write a 1 then a 0 to enter and exit the reset state)					0				Normal Operation
						1				Resets the LM9830
MASTER CLOCK DIVIDER										
08	**MCLK Divider** This register sets the master clock frequency for the entire scanner. $f_{MCLK} = f_{CRYSTAL}$/MCLK_Divider $f_{ADC} = f_{MCLK}/8$			0	0	0	0	0	0	÷1.0
				0	0	0	0	0	1	÷1.5
				0	0	0	1	1	0	÷4
				a	a	a	a	a	a	÷ ((aaaaaa/2)+1)
				1	1	1	1	1	0	÷32.0
				1	1	1	1	1	1	÷32.5
HORIZONTAL RESOLUTION AND DATAMODE SETTINGS										
09	**Horizontal DPI Divider** This register determines the horizontal resolution of the scan. Scan resolution = Optical resolution divided by the Horizontal_DPI_Divider.						0	0	0	÷1
							0	0	1	÷1.5
							0	1	0	÷2
							0	1	1	÷3
							1	0	0	÷4
							1	0	1	÷6
							1	1	0	÷8
							1	1	1	÷12
	Pixel Packing This register determines how many bits in each byte of data are transmitted to the host when DataMode = 0				0	0				1 bit/pixel (1 bit grayscale/3 bit color)
					0	1				2 bits/pixel (2 bit grayscale/6 bit color)
					1	0				4 bits/pixel (4 bit grayscale/12 bit color)
					1	1				8 bits/pixel (8 bit grayscale/24 bit color)
	DataMode When DataMode = 0, the pixel data is fully processed, going through the Offset, Shading, Horizontal DPI Adjust, Gamma, and Pixel Packing blocks. When DataMode = 1, 10 bit data is extracted following the Horizontal DPI Adjust stage. Gamma and any other post processing must be done by the host. When DataMode = 1, Horizontal DPI Adjust = 0, and the Offset and Gain coefficients are set to 0, the 12 bit data straight from the ADC is transmitted. Offset, Shading, Gamma and any other post processing must be done by the host.			0						1, 2, 4, or 8 bit image data, as determined by the Pixel Size setting.
				1						10 bit image data - sent in 2 bytes: X X X X 9 8 7 6- 5 4 3 2 1 0 X X 12 bit image data - sent in 2 bytes: X X X X 11 10 9 8 - 7 6 5 4 3 2 1 0, Horizontal DPI Divider = 0.

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
RESERVED										
0A	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to this register
SENSOR CONFIGURATION										
0B	**Input Signal Polarity**								0	Negative (CCD Sensor)
									1	Positive (CIS Sensor)
	CDS On/Off							0		CDS Off
								1		CDS On
	Standard/Even Odd Sensor						0			Standard (1 pixels per Ø period)
							1			Even/Odd (2 pixels per Ø period)
	Sensor Resolution					0				300 dpi (pixels < 2731)
	(used only for SRAM coefficient allocation)					1				600 dpi (2730 < pixels < 5461)
	Line Skipping Color Phase Delay Part of the “n out of m” function, consisting of registers 0B (bits 4-7) 44, 45 (bit 5), and 5A.	n	n	n	n					n lines, n = 0-15
SENSOR CONTROL SETTINGS										
0C	**Ø1 Polarity**								0	Positive
									1	Negative
	Ø2 Polarity							0		Positive
								1		Negative
	RS Polarity						0			Positive
							1			Negative
	CP1 Polarity					0				Positive
						1				Negative
	CP2 Polarity				0					Positive
					1					Negative
	TR1 Polarity			0						Positive
				1						Negative
	TR2 Polarity		0							Positive
			1							Negative
0D	**Ø1 Active/Off**								0	Off
									1	Active
	Ø2 Active/Off							0		Off
								1		Active
	RS Active/Off						0			Off
							1			Active
	CP1 Active/Off					0				Off
						1				Active
	CP2 Active/Off				0					Off
					1					Active
	TR1 Active/Off			0						Off
				1						Active
	TR2 Active/Off		0							Off
			1							Active
	Number of TR Pulses	0								1 TR Pulse
		1								2 TR Pulses
0E	**TR Pulse Duration**					n	n	n	n	n+1 pixel periods (1-16)
	TR-Ø1 Guardband Duration	n	n	n	n					n pixel periods (0-15)
0F	**Optical Black Clamp Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
10	**Optical Black Clamp End**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
11	**Reset Pulse Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
12	**Reset Pulse Stop**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
13	**CP1 Pulse Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
14	**CP1 Pulse Stop**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
15	**CP2 Pulse Start**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
16	**CP2 Pulse Stop**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
17	**Reference Sample Position**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge
18	**Signal Sample Position**				n	n	n	n	n	pixel rate: n=0-23, line rate: n=0-7 MCLKs from Ø1 edge

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
19	**CIS TR1 Timing Mode**							0	0	Off - use standard CCD Timing
								0	1	CIS TR1 Timing Mode 1: TR1 pulse = exactly one Ø clock, starting at rising edge of Ø1
								1	0	CIS TR1 Timing Mode 2: TR1 pulse = exactly one Ø clock, TR1 centered around Ø1 high.
								1	1	N/A
	Fake Optical Black Pixels (for Dyna-type CIS sensors)						0			Off: Normal operation
							1			On: RS pulse held high during entire Optical Black period
RESERVED										
1A	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to this register
1B	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to this register
SENSOR PIXEL CONFIGURATION										
1C	**Optical Black Pixels Start**	n	n	n	n	n	n	n	n	n pixels (0 - 255)
1D	**Optical Black Pixels End**	n	n	n	n	n	n	n	n	n pixels (0 - 255)
1E	**Active Pixels Start - MSB**			n	n	n	n	n	n	n pixels (10 - 16383) This is where image data starts coming out of the sensor, and determines the pixel where offset and shading correction begins (pixel 0 in the DataPort)
1F	**Active Pixels Start - LSB**	n	n	n	n	n	n	n	n	
20	**Line End - MSB**			n	n	n	n	n	n	n pixels (0 - 16383) This selects the pixel count at which the current line is ended and the next line begins. This determines the integration time of one line.
21	**Line End - LSB**	n	n	n	n	n	n	n	n	
PIXEL DATA RANGE TO PROCESS										
22	**Data Pixels Start - MSB**			n	n	n	n	n	n	n pixels (**Active Pixels Start** - 16383) This selects the start of the range of pixels transmitted to the PC. This value must be >= **Active Pixels Start**
23	**Data Pixels Start - LSB**	n	n	n	n	n	n	n	n	
24	**Data Pixels End - MSB**			n	n	n	n	n	n	n pixels (**Data Pixels Start** - [**Line End** - 20]) This selects the end of the range of pixels transmitted to the PC. This value must be <= [**Line End** - 20]
25	**Data Pixels End - LSB**	n	n	n	n	n	n	n	n	

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
COLOR MODE SETTINGS										
26	**AFE Operation** 3 Channel or 1 Channel						0	0	0	3 Channel Pixel Rate Color
							0	0	1	3 Channel Line Rate Color
							1	0	0	1 Channel Mode A (1 Channel Grayscale)
							1	0	1	1 Channel Mode B (1 Channel Line Rate Color)
	1 Channel Mode A Channel Color (1 Channel Mode B always uses the Blue Channel)				0	0				Red
					0	1				Green
					1	0				Blue
					1	1				N/A
	TR$_{RED}$ (=TR1) position (3 Channel Line Rate Mode only)			0						1st TR pulse position (inside Ø1 high)
				1						2nd TR pulse position (inside Ø1 low)
	TR$_{GREEN}$ (=TR2) position (3 Channel Line Rate Mode only)		0							1st TR pulse position (inside Ø1 high)
			1							2nd TR pulse position (inside Ø1 low)
	TR$_{BLUE}$ (=CP2) position (3 Channel Line Rate Mode only)	0								1st TR pulse position (inside Ø1 high)
		1								2nd TR pulse position (inside Ø1 low)
27	**Integration Time Adjust** **(TR$_{RED}$ drop rate)** (3 Channel Line Rate Mode only)							0	0	Do not drop any TR$_{RED}$ pulses
								0	1	Drop 1 TR$_{RED}$ pulse (double integration time)
								1	0	Drop 2 TR$_{RED}$ pulses (triple integration time)
								1	1	N/A
	Integration Time Adjust **(TR$_{GREEN}$ drop rate)** (3 Channel Line Rate Mode only)					0	0			Do not drop any TR$_{GREEN}$ pulses
						0	1			Drop 1 TR$_{GREEN}$ pulse (double integration time)
						1	0			Drop 2 TR$_{GREEN}$ pulses (triple integration time)
						1	1			N/A
	Integration Time Adjust **(TR$_{BLUE}$ drop rate)** (3 Channel Line Rate Mode only)			0	0					Do not drop any TR$_{BLUE}$ pulses
				0	1					Drop 1 TR$_{BLUE}$ pulse (double integration time)
				1	0					Drop 2 TR$_{BLUE}$ pulses (triple integration time)
				1	1					N/A
RESERVED										
28	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to this register

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
ILLUMINATION SETTINGS										
29	**Illumination Mode** Controls the function of the 3 LAMP outputs, LAMP$_R$, LAMP$_G$, and LAMP$_B$ Mode 0 is the Off/Reset state. Mode 1 is typically used for CCFL lamps. Mode 2 is for color scanning with tri-color LEDs. Mode 3 is for grayscale scanning with tri-color LEDs.							0	0	LAMP$_R$ = LAMP$_G$ = LAMP$_B$ = 0V (Power-On/Reset Default)
								0	1	Illumination Mode 1 - LAMP$_R$ and LAMP$_B$ turn on every line, with their on and off points controlled by the Pixel Counter settings. LAMP$_G$ Output is continuous PWM pulse stream. (Figure 28) LAMP$_R$ and/or LAMP$_B$ may be set to stay on or off at all times by setting the LAMP Off or LAMP On settings (registers 2C-37) greater than the Line End value (registers 20 and 21).
								1	0	Illumination Mode 2 - LAMP$_R$, LAMP$_G$, LAMP$_B$ turn on sequentially at the line rate, with their on and off points controlled by Pixel Counter settings. (Figure 29)
								1	1	Illumination Mode 3 - LAMP$_R$, LAMP$_G$, LAMP$_B$ turn on every line, with their on and off points controlled by the Pixel Counter settings. (Figures 30 and 31)
2A	**LAMP$_G$ PWM - MSB** (Illumination Mode 1)					n	n	n	n	LAMP$_G$ output is a PWM pulse stream. Duty cycle is n/4095. Clock for counter is CRYSTAL IN, giving max output frequency of 12.2kHz for $f_{CRYSTAL\ IN}$ = 50MHz.
2B	**LAMP$_G$ PWM - LSB** (Illumination Mode 1)	n	n	n	n	n	n	n	n	
2C	**LAMP$_R$ On - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the LAMP$_R$ output goes high (if programmed)
2D	**LAMP$_R$ On - LSB**	n	n	n	n	n	n	n	n	
2E	**LAMP$_R$ Off - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the LAMP$_R$ output goes low (if programmed)
2F	**LAMP$_R$ Off - LSB**	n	n	n	n	n	n	n	n	
30	**LAMP$_G$ On - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the LAMP$_G$ output goes high (if programmed)
31	**LAMP$_G$ On - LSB**	n	n	n	n	n	n	n	n	
32	**LAMP$_G$ Off - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the LAMP$_G$ output goes low (if programmed)
33	**LAMP$_G$ Off - LSB**	n	n	n	n	n	n	n	n	
34	**LAMP$_B$ On - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the LAMP$_B$ output goes high (if programmed)
35	**LAMP$_B$ On - LSB**	n	n	n	n	n	n	n	n	
36	**LAMP$_B$ Off - MSB**			n	n	n	n	n	n	n pixels (1 - 16384) This selects the pixel count at which the LAMP$_B$ output goes low (if programmed)
37	**LAMP$_B$ Off - LSB**	n	n	n	n	n	n	n	n	
STATIC OFFSET AND GAIN SETTINGS FOR ANALOG FRONT END										
38	**Static Offset (Red)**			0	n	n	n	n	n	Offset = +n*9.3mV, n = 0 to 31
				1	n	n	n	n	n	Offset = -n*9.3mV, n = 0 to 31
39	**Static Offset (Green)**			0	n	n	n	n	n	Offset = +n*9.3mV, n = 0 to 31
				1	n	n	n	n	n	Offset = -n*9.3mV, n = 0 to 31
3A	**Static Offset (Blue)**			0	n	n	n	n	n	Offset = +n*9.3mV, n = 0 to 31
				1	n	n	n	n	n	Offset = -n*9.3mV, n = 0 to 31
3B	**Static Gain (Red)**			0	n	n	n	n	n	Gain = 0.93 + 0.067*n (V/V), n = 0 to 31
				1	n	n	n	n	n	Gain = 3(0.93 + 0.067*n) (V/V), n = 0 to 31
3C	**Static Gain (Green)**			0	n	n	n	n	n	Gain = 0.93 + 0.067*n (V/V), n = 0 to 31
				1	n	n	n	n	n	Gain = 3(0.93 + 0.067*n) (V/V), n = 0 to 31
3D	**Static Gain (Blue)**			0	n	n	n	n	n	Gain = 0.93 + 0.067*n (V/V), n = 0 to 31
				1	n	n	n	n	n	Gain = 3(0.93 + 0.067*n) (V/V), n = 0 to 31

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
DIGITAL PIXEL RATE OFFSET AND GAIN SETTINGS										
3E	**Multiplier Gain Range** Smaller gain ranges provide finer control. Larger gain ranges correct for larger shading errors.							0	0	1.5:1 (33%)
								0	1	2.0:1 (50%)
								1	0	3.0:1 (66%)
								1	1	Bypass Multiplier
	Offset/Gain data format						0			6 bits offset/10 bits gain
							1			8 bits offset/8 bits gain
	Multiplier Coefficient Source					0				Configuration Register 3F (Fixed)
						1				External SRAM
	Offset Coefficient Source				0					Configuration Register 40 and 41 (Fixed)
					1					External SRAM
3F	**Fixed Offset Coefficient**	n	n	n	n	n	n	n	n	Fixed Offset to use for calibration - 2MSBs are assumed to be 0 if using 6 bit offset format
40	**Fixed Multiplier Coefficient - MSB**							n	n	Fixed Gain to use for calibration - 2LSBs are assumed to be 0 if using 8 bit gain format
41	**Fixed Multiplier Coefficient - LSB**	n	n	n	n	n	n	n	n	
PARALLEL PORT SETTINGS										
42	**Communication Mode** (for reading data from any of the LM9830's registers) **Note: This register must be set appropriately before data can be read from the LM9830!**								0	8 bit Bidirectional/EPP
									1	4 bit Nibble
	Parallel Port Output Driver Current (I_{OL} and I_{OH} can be used to calculate rise and fall times into the load capacitance: rise/fall time approximately equals 5V*C/i)						0	0		I_{OL} = 5mA, I_{OH} = -6mA
							0	1		I_{OL} = 7mA, I_{OH} = -9mA
							1	0		I_{OL} = 9mA, I_{OH} = -12mA
							1	1		I_{OL} = 15mA, I_{OH} = -21mA
EXTERNAL SRAM SETTINGS										
43	**External SRAM Size**							0	0	64 kbytes (not recommended for 600dpi scanners)
								0	1	128 kbytes
								1	0	256 kbytes
								1	1	N/A
	SRAM Interface Output Driver Current (I_{OL} and I_{OH} can be used to calculate rise and fall times into the load capacitance: rise/fall time approximately equals 5V*C/i)					0	0			I_{OL} = 3.5mA, I_{OH} = -4mA
						0	1			I_{OL} = 6mA, I_{OH} = -7.5mA
						1	0			I_{OL} = 12mA, I_{OH} = -17mA
						1	1			I_{OL} = 21mA, I_{OH} = -32mA
	SRAM Bandwidth (8 Bit Data Mode) 8 slot mode should always be used to maximize performance. If the external SRAM is to slow to meet the $t_{\overline{RD}\ SETUP}$ requirement, the slower 4 SRAM accesses/ADC clock mode may be used.				0					4 SRAM accesses/ADC clock
					1					8 SRAM accesses/ADC clock (f_{MCLK} must be 25MHz or lower)
	Scanning Duplex (10/12 bit Data Mode) Full Duplex mode should always be used to maximize scan speed. If the external SRAM is to slow to meet the $t_{\overline{RD}\ SETUP}$ requirement, the slower Half Duplex mode may be used.			0						Full Duplex- Can transmit data while scanning (f_{MCLK} must be 25MHz or lower)
				1						Half Duplex - Can only transmit data when buffer is full or scan has been stopped

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
STEPPER MOTOR CONTROL SETTINGS 1										
44	**n (Line Skipping)** Part of the "n out of m" function, consisting of registers 0B (bits 4-7) 44, 45 (bit 5), and 5A.	t	t	t	t	t	t	t	t	n lines saved in SRAM for every m lines (register 5A) scanned, function bypassed if register value = 0. n (lines saved per m lines scanned) = 256 - t t = 256 - n If t = 0 then function is bypassed
45	**Full/Microstepping**								0	Full Step Mode
									1	MicroStepping Mode
	Current Sensing Phases = 0 for fullstepping = 1 for microstepping							0		1 Phase - No microstepping, just kickstart/stop functions
								1		2 Phases - necessary for microstepping
	Stepper Motor Phase A Polarity						0			Positive (A/B/$\overline{A}$/$\overline{B}$ Output high = winding energized)
							1			Negative (A/B/$\overline{A}$/$\overline{B}$ output low = winding energized)
	Stepper Motor Phase B Polarity					0				Positive (A/B/$\overline{A}$/$\overline{B}$ Output high = winding energized)
						1				Negative (A/B/$\overline{A}$/$\overline{B}$ output low = winding energized)
	A, B, $\overline{A}$, and $\overline{B}$ stepper motor status				**0**					A, B, $\overline{A}$, and $\overline{B}$ output pins in Tri-State
					1					A, B, $\overline{A}$, and $\overline{B}$ output pins active
	Line Skipping Phase Part of the "n out of m" function, consisting of registers 0B (bits 4-7) 44, 45 (bit 5), and 5A.			0						Red sensor data arrives before Green sensor
				1						Blue sensor data arrives before Green sensor
46	**Scanning Step Size - MSB**			n	n	n	n	n	n	The step size of one microstep while scanning, in units of pixel periods (minimum 2).
47	**Scanning Step Size - LSB**	n	n	n	n	n	n	n	n	
48	**Fast Feed Step Size - MSB**			n	n	n	n	n	n	The step size of one microstep while fast feeding, in units of pixel periods (minimum 2).
49	**Fast Feed Step Size - LSB**	n	n	n	n	n	n	n	n	
4A	**Fullsteps to Skip at Start of Scan - MSB**			n	n	n	n	n	n	When scan starts, paper is fed forward n full steps (0 - 16383) at highest speed. For "zooming" in flatbeds
4B	**Fullsteps to Skip at Start of Scan - LSB**	n	n	n	n	n	n	n	n	
4C	**Fullsteps to Scan after Paper Sensor #2 trips -MSB**			n	n	n	n	n	n	Adds a delay of n (0-16383) full steps between when Paper Sensor #2 trips and when the scanning bit is reset, terminating the scan/motor movement.
4D	**Fullsteps to Scan after Paper Sensor #2 trips -LSB**	n	n	n	n	n	n	n	n	
4E	**Pause scanning, stop/reverse motor**	n	n	n	n	n	n	n	n	Pause scan when buffer is n kbytes full
4F	**Resume scanning, start motor**	n	n	n	n	n	n	n	n	Resume scan when buffer is n kbytes full
50	**Full steps to reverse when buffer is full**			n	n	n	n	n	n	n (0-63) full steps (0 = do not reverse)
51	**Acceleration Profile (stopped)**							n	n	n (0-3) full step time units pause while stopped
	Acceleration Profile (25%)					n	n			n (0-3) full steps at 25% speed
	Acceleration Profile (50%)			n	n					n (0-3) full steps at 50% speed
52	**Default Phase Difference - MSB**	n	n	n	n	n	n	n	n	Used to calculate when motor resumes after reversing and stopping. 1 < n < 65535
53	**Default Phase Difference - LSB**	n	n	n	n	n	n	n	n	
54	**Lines to Process After Pause Scan Signal**						n	n	n	n (0-7) lines. This only applies if the motor doesn't reverse (reverse steps = 0).
	Lines to Discard after Resume Scan Signal			n	n	n				n (0-7) lines. This only applies if the motor doesn't reverse (reverse steps = 0). Should be set to same value as bits 0-2.
55	**Kickstart Steps** (fullstepping mode)						n	n	n	Motor gets maximum current for first n (0-7) full steps
	Hold Current Timeout	n	n	n	n	n				Full step time units (1-31), 0 = no hold current
56	**Stepper Motor PWM Frequency**	n	n	n	n	n	n	n	n	=CRYSTAL IN/(4*n) (0 < n < 256) =CRYSTAL IN/(4*256) (n = 0)
57	**Stepper Motor PWM Set Duty Cycle**			n	n	n	n	n	n	= n/64 (default = 0)

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
PAPER SENSOR SETTINGS										
58	**Paper Sensor #1 Polarity**								0	A low input on Paper Sensor #1 is True
									1	A high input on Paper Sensor #1 is True
	Paper Sensor #1: Level/Edge sensitive							0		Level sensitive: Paper Sensor #1 State bit (in Status Register) is set to a 1 if Paper Sensor #1 is currently True.
								1		Edge sensitive: Paper Sensor #1 State bit (in Status Register) is set to a 1 if Paper Sensor #1 has been True since the last time the Status Register was read.
	Paper Sensor #1: Stop Scan						0			Transitions on Paper Sensor #1 will not clear the scanning bit.
							1			A False - to - True transition on Paper Sensor #1 will clear the Command Register and stop the scan.
	Paper Sensor #2 Polarity					0				A low input on Paper Sensor #2 is True
						1				A high input on Paper Sensor #2 is True
	Paper Sensor #2: Level/Edge sensitive				0					Level sensitive: Paper Sensor #2 State bit (in Status Register) is set to a 1 if Paper Sensor #2 is currently True.
					1					Edge sensitive: Paper Sensor #2 State bit (in Status Register) is set to a 1 if Paper Sensor #2 has been True since the last time the Status Register was read.
	Paper Sensor #2: Stop Scan			0						Transitions on Paper Sensor #2 will not clear the scanning bit.
				1						A False - to - True transition on Paper Sensor #2 will clear the Command Register and stop the scan (after the number of lines specified in the **Fullsteps to Scan after Paper Sensor #2 trips** register).
MISC I/O PIN SETTINGS										
59	**Misc I/O #1: Input or Output**								$\boxed{0}$	The Misc I/O #1 pin is configured as an input.
									1	The Misc I/O #1 pin is configured as an output.
	Misc I/O #1: Polarity (if configured as an input)							0		A low input on Misc I/O #1 is True
								1		A high input on Misc I/O #1 is True
	Misc I/O #1: Level/Edge sensitive (if configured as an input)						0			Level sensitive: Misc I/O #1 State bit (in Status Register) is set to a 1 if Misc I/O #1 is currently True.
							1			Edge sensitive: Misc I/O #1 State bit (in Status Register) is set to a 1 if Misc I/O #1 has been True since the last time the Status Register was read.
	Misc I/O #1: Output State (if configured as an output)					0				The output of the Misc I/O #1 pin will be a logic low (0V).
						1				The output of the Misc I/O #1 pin will be a logic high (5V).
	Misc I/O #2: Input or Output				$\boxed{0}$					The Misc I/O #2 pin is configured as an input.
					1					The Misc I/O #2 pin is configured as an output.
	Misc I/O #2: Polarity (if configured as an input)			0						A low input on Misc I/O #2 is True
				1						A high input on Misc I/O #2 is True
	Misc I/O #2: Level/Edge sensitive (if configured as an input)		0							Level sensitive: Misc I/O #2 State bit (in Status Register) is set to a 1 if Misc I/O #2 is currently True.
			1							Edge sensitive: Misc I/O #2 State bit (in Status Register) is set to a 1 if Misc I/O #2 has been True since the last time the Status Register was read.
	Misc I/O #2: Output State (if configured as an output)	0								The output of the Misc I/O #2 pin will be a logic low (0V).
		1								The output of the Misc I/O #2 pin will be a logic high (5V).
STEPPER MOTOR CONTROL SETTINGS 2										
5A	**m (Line Skipping)** Part of the “n out of m” function, consisting of registers 0B (bits 4-7) 44, 45 (bit 5), and 5A.	m	m	m	m	m	m	m	m	n lines (register 44) saved in SRAM for every m lines scanned. m = 1 to 255. If m = 0 then function is bypassed

Address	Function	D7	D6	D5	D4	D3	D2	D1	D0	Value
TEST MODE SETTINGS										
5B	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to this register
5C	**ADC Output Code - MSB**					n	n	n	n	Used to force the input to the Offset Subtractor
5D	**ADC Output Code - LSB**	n	n	n	n	n	n	n	n	to a known value for digital tests
5E	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to this register for normal operation, modify bits 5 and 7 as shown below for test modes
	Offset Subtractor Input Select			0						The ADC is input to Offset Subtractor
				1						Registers 5C and 5D are input to Offset Subtractor
	CDS Signal	0								Normal Operation
		1								CDS signal is output on TEST pin
5F-6F	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to these registers
70	**Parallel Port Noise Filter**	0	1	1	1	0	0	0	0	Write 70 to this register
71-7F	**Reserved**	0	0	0	0	0	0	0	0	Write 00 to these registers

Applications Information

1.0 THEORY OF OPERATION

1.1 Overview

A scanner is composed of many different but tightly interconnected blocks (the analog front end and ADC, sensor clock generation, stepper motor control, data buffering, parallel port I/O, and others).

1.2 Signal Processing Overview

1.3 Scanner Support Functions Overview

2.0 Signal Processing Operation

2.1 ADC

The ADC is a 6MHz 12 bit pipelined architecture.

2.2 Pixel Rate Offset Correction Block

Two bytes are used to store the pixel rate offset and gain coefficients for each pixel. For CCDs, the split is usually 6 bits for offset and 10 bits for gain. For some CIS sensors with unusually large offsets, the offset correction range may be increased by changing the split to 8 bits for offset and 8 bits for gain. This split is determined by a bit in the configuration register.

A digital subtractor subtracts the 6 (or 8) bit offset word (corresponding to that pixel's offset error) from each pixel. The LSB of the offset word is the same size as the 10 bit LSB of the ADC (the two smallest 12 bit ADC output bits, D1 and D0, are not used with the offset subtractor). The coefficients are stored in the external RAM and accessed at the pixel rate.

The subtractor saturates at 0, i.e. if the coefficient to be subtracted is greater than the ADC output code, the result is an output of 0.

2.3 Pixel Rate Gain Correction Block

This is a digital multiplier that multiplies the output word from the subtractor by a 10 (or 8) bit digital correction coefficient corresponding to that pixel's gain error. The coefficients are stored in the external RAM and accessed at the pixel rate. When in 8 bit mode, the 8 bits correspond to the top 8 MSBs of the 10 bit digital correction coefficient word. The 10 bit LSBs of the input word are padded with 0s in 8 bit mode.

The multiplier saturates at 1023, i.e. if the result of the multiplication is greater than 1023, the multiplier output is 1023.

2.4 Pixel Processing Block

2.4.1 Pixel Processing In 8/24 Bit Mode

In the 8 and 10 bit output modes (for 24 and 30 bit color scans), this stage is where the optical resolution of the sensor is digitally reduced.

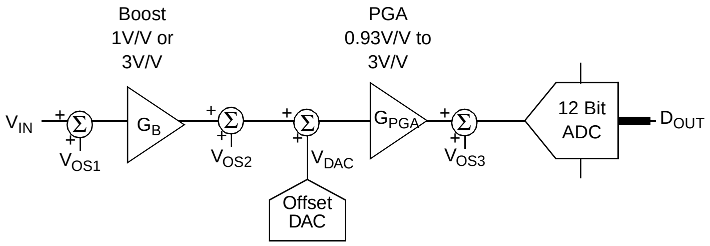
To maximize scanning speed and image quality at the popular resolutions of 400, 300, 200, 150, 100, 75, and 50 dpi, the resolution can be reduced inside the scanner, prior to the gamma correction stage. (Resolution in the vertical direction is controlled by the stepper motor speed.) This is done by averaging adjacent pixels. For example, to get 100 dpi from a 300dpi optical sensor, you would average 3 300dpi pixels:

$$\text{pixel}_{100\text{dpi}} = \frac{p_{n-2} + p_{n-1} + p_n}{3}$$

The number of pixels out of the Pixel Processing block is equal to the integer portion of the number of pixels in to the Pixel Processing block divided by the “Divide By” setting, from the table shown in Figure 11.

$$\text{Pixels}_{\text{OUT}} = \text{INT}\left(\frac{\text{Pixels}_{\text{IN}}}{\text{Divide By}}\right)$$

If there are not enough pixels at the end of a line to form a complete pixel, the last pixel will be eliminated. For example, if a line is 35 pixels wide and the Horizontal DPI setting is set to divide by 6, then the output of the Pixel Processing block will be 5 pixels (the integer portion of 35/6). The last 5 pixels will be discarded, since 6 pixels would be required to form a new pixel in this mode.



$$D_{OUT} = (((V_{IN} + V_{OS1})G_B + V_{DAC} + V_{OS2})G_{PGA} + V_{OS1})C$$

simplified, with all offsets = 0, this is:

$$D_{OUT} = (V_{IN}G_B + V_{DAC})G_{PGA}C$$

C is a constant that combines the gain error through the AFE, reference voltage variance, and analog voltage to digital code conversion into one constant. Ideally, C = 2048 codes/V (4096codes/2V). Manufacturing tolerances widen the range of C. See Electrical Specifications

Figure 10: Analog Front End (AFE) Model

This equation also applies to the divide by 1.5 function.

Divide By	DPI (600 DPI sensor)	DPI (300 DPI sensor)
1	600	300
1.5	400	200
2	300	150
3	200	100
4	150	75
6	100	50
8	75	37.5
12	50	25

Figure 11: Decreasing Horizontal Resolution

The output of this stage is sent through the gamma and pixel packing stages, resulting in output data formatted as shown in Figure 15.

2.4.2 Pixel Processing 10/30 Bit Mode

Scanning in 10 bit mode (30 bit color) supports the Horizontal DPI Divider function as well as the pixel rate shading and offset functions. The output data is formatted as shown in Figure 12 (X=mask out in software).

7	6	5	4	3	2	1	0	Order
X	X	X	X	9	8	7	6	First Byte
5	4	3	2	1	0	X	X	Second Byte

Figure 12: 10 Bit Mode Pixel Data Format

The software on the host PC must perform any gamma correction desired.

There are two variations on the 10 and 12 bit output modes: Full Duplex and Half Duplex, determined by bit 5 of Configuration Register 43. In the Full Duplex mode, there are 6 SRAM operations per pixel: offset data read, gain data read, pixel MSB write, pixel LSB write, pixel MSB read, pixel LSB read). Since there are 8 MCLKs per pixel, the writes take 2 MCLK periods and the reads take 1 MCLK period. This mode is preferred because it permits faster scanning, but it requires fast SRAM access.

The Half Duplex mode accommodates slower SRAM. In Half Duplex mode, the data in the SRAM can not be read by the host PC until the buffer is full. Therefore there are two phases to scanning data in the Half Duplex mode. The first is writing pixel data to SRAM using 4 operations/pixel (offset data read, gain data read, pixel MSB write, pixel LSB write). In this mode the read and write cycles will all be 2 MCLKs long. The second phase is reading the contents of the SRAM and sending them to the host PC. This read operation uses 2 MCLK read cycles/byte.

2.4.3 Pixel Processing: 12/36 Bit Mode

Scanning in 12 bit mode (36 bit color) can only be done at the optical resolution of the sensor, and the shading and offset functions can not be used. The Horizontal DPI Divider function must be set to 1 (register 09, bits 0-2 = 0) to get 12 bit data. The shading and offset functions must also be disabled (registers 3E, 3F, 40, and 41 all set to 0). The 10 bit pixel output from the multiplier is combined with the 2 12 bit LSBs from the ADC to recreate the 12 bit pixel. The output data is formatted as shown in Figure 13 (X=mask out in software).

7	6	5	4	3	2	1	0	Order
X	X	X	X	11	10	9	8	First Byte
7	6	5	4	3	2	1	0	Second Byte

Figure 13: 12 Bit Mode Pixel Data Format

The software on the host PC must perform all offset and shading correction, horizontal resolution adjustment, and gamma correction.

The 12 bit mode uses the same Full or Half Duplex options described in **2.4.2 Pixel Processing 10/30 Bit Mode**

2.5 Gamma Correction Tables

There are 3 gamma lookup tables for R, G, and B. The input to the table is the 10 bit pixel data coming from the previous stage (**2.4 Pixel Processing Block**). The output is the 8 bit gamma corrected pixel data. The tables are therefore 1K bytes x 8 bits in size. Each gamma table (red, green, and blue) can be loaded with any arbitrary user-defined transfer curve.

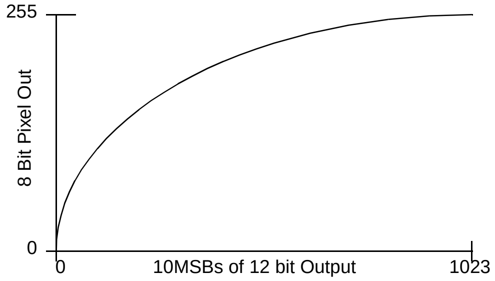


Figure 14: Gamma Table

The gamma tables are loaded through the dataport (see **5.1 The DataPort: Reading and Writing to Gamma, Offset, and Gain Memory**). In most LM9830 modes, the DataPort selects which color (Red, Green or Blue) gamma table will be read from or written to. In 1 Channel Mode A, the only gamma table that can be accessed is the gamma table for the 1 Channel Mode A color selected by bits 3 and 4 of register 26.

2.6 Pixel Packing/Thresholding Block

Some scans require only one bit per pixel (“line art” mode), others may need only 2 or 4 bits/pixel. To increase scanning speed for lower pixel depths, the LM9830 packs the desired MSBs of multiple pixels together, increasing the transmission speed to the host by a factor of 2, 4, or 8. Figure 15 shows how the pixels are packed together for 8, 4, 2, and 1 bit pixel depths. In Figure 15, “b” indicates the bit position (b7 = the most significant and b0 =

Pixel Depth	7	6	5	4	3	2	1	0
8	b7 p_0	b6 p_0	b5 p_0	b4 p_0	b3 p_0	b2 p_0	b1 p_0	b0 p_0
4	b7 p_0	b6 p_0	b5 p_0	b4 p_0	b7 p_1	b6 p_1	b5 p_1	b4 p_1
2	b7 p_0	b6 p_0	b7 p_1	b6 p_1	b7 p_2	b6 p_2	b7 p_3	b6 p_3
1	b7 p_0	b7 p1	b7 p_2	b7 p_3	b7 p_4	b7 p_5	b7 p_6	b7 p_7

Figure 15: Packing Multiple Pixels Into One Byte

the least significant bit) of the original 8 bit pixel data, and p_n indicates the original pixel sequence, i.e p_0, p_1, p_2, p_3...

If there are not enough unpacked pixels at the end of a line to complete the packed byte for transmission, that final byte is not sent.

The gamma table in **2.5 Gamma Correction Tables** allows the user to set the threshold of each transition for various line art or reduced pixel depth modes.

2.7 Line Buffer

The line buffer uses the external SRAM to store the pixel data at the fixed rate and send it back to the PC at an asynchronous, unpredictable, and non-constant rate.

This buffer is tightly coupled to the stepper motor (**3.0 Stepper Motor Controller**), and is responsible for stopping the motor before the buffer overflows and starting the motor again as the buffer nears empty.

If the scanner is generating pixel data faster than the PC can acquire it, the line buffer will start to fill up. As the buffer nears 100% full, the scan must be paused before it starts acquiring a line it cannot store because of lack of RAM. This Pause Threshold limit (register 4E) is programmable in 1 kbyte increments between 0 and 255 kbytes but should be no higher than 100% of the buffer RAM size minus 1 line of data (for single output CCDs and CIS) or 3 lines of data (for triple output CCDs and CIS). When this point is reached the buffer sends a command to the stepper motor controller to stop scanning. The remainder of the line being processed will continue being processed and be sent to the buffer. If the Lines To Process After Pause Scan Signal register (register 54) is greater than 0, then room for these additional lines need to be added into the Pause Threshold value calculation.

After a pause, the buffer will now transmit data to the PC until it hits the Resume Threshold limit (register 4F), which is also programmable in 1 kbyte increments between 0 and 256kbytes. When the Resume Threshold is reached, the Line Buffer sends the motor controller a command to resume.

Note that the scanner software on the host PC is responsible for ensuring that the Pause Threshold value is low enough to ensure that any data that comes after a pause request (the rest of the current line and any subsequent lines if register 54 bits 0-2 are greater than 0) will fit into the SRAM buffer size, which is equal to SRAM size - COEFFICIENT size.

The pause condition is reached when the number of bytes in the buffer is equal to the value in register 4E * 1024. The scan will resume when the number of bytes in the buffer is equal to (the value in register 4F * 1024 + 1023).

Since the external SRAM also contains the pixel gain and offset data (see **2.2 Pixel Rate Offset Correction Block** and **2.3 Pixel Rate Gain Correction Block**), the buffer is as large as the SRAM size minus the coefficient storage. Supported SRAM sizes are 64kbyte, 128kbyte, and 256kbyte. Coefficient data always takes up a total of 16kbytes for 300dpi sensors and 32kbytes for 600dpi sensors.

3.0 Stepper Motor Controller

The stepper motor controller sends a series of pulses to the stepper motor to move the paper past the sensor (sheetfed) or the sensor past the paper (flatbed). The speed at which the paper moves relative to the sensor, combined with the integration time of the image sensor, determines the effective vertical resolution (Lines Per Inch, or LPI).

The stepper motor is moved forwards and backwards by two signals, A and B, 90° out of phase with each other. The phase for the forward direction is set in Configuration Register 45.

The A and B signals are either squarewaves (in Full Step Mode, Figure 16), or a staircase approximation of a sine wave (in Microstep mode, Figures 18 and 19).

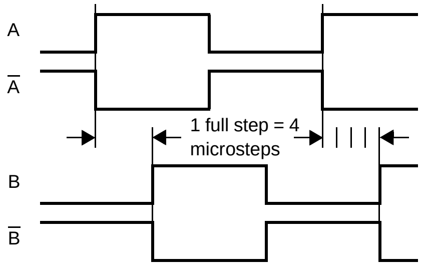


Figure 16: Stepper Motor Waveform - Full Stepping

The LM9830 always counts stepper motor steps in units of microsteps. A full step is equal to four microsteps. Even when the LM9830 is in Full Step Mode, it is counting in microsteps, and will increment the stepper motor (generating a full step) every four microsteps.

The microstep Step Size is defined in units of time. These units of time are pixel periods, as defined in the horizontal pixel counter. In the 3 channel pixel rate input mode, the pixel period is the $f_{ADC}/3$ (= $f_{MCLK}/24$). In the 3 channel line rate and 1 channel modes, the pixel period is equal to $f_{ADC}/3$ (= $f_{MCLK}/24$). The Step Size is stored in the **Scanning Step Size** configuration register as a 14 bit value. During normal operation, the stepper motor is advanced 1 microstep every Step Size pixel periods. The LPI can be calculated as follows:

$$\mathrm{LPI} = 4C\frac{\mathrm{StepSize}}{\mathrm{pixels/line}}$$

Where C = the number of full steps required to move the image one inch, pixels/line is the number of pixel periods it takes to scan one horizontal line (equivalent to the value stored in the **Line End** registers), and StepSize is the number of pixel periods/microstep

Whenever the stepper motor has been moving and then comes to a stop, the LM9830 waits for the time specified in the Hold Current Timeout register and then de-asserts the A, B, $\overline{A}$, and $\overline{B}$ outputs to cut power to the motor. When the stepper motor is not scanning or fast-feeding (Command = 00), A, B, $\overline{A}$, and $\overline{B}$ are de-asserted in all stepper modes.

There are two modes of stepper motor operation: fullstepping and microstepping.

3.1 Full Step Mode

In Full Step Mode the output is a pulse stream, as shown in Figure 16. The amplitude of the pulses is controlled by the output of the 2 bit DAC, shown in Figure 17.

Scan Mode	DAC Voltage
Starting from a dead stop	0.5V for number of steps specified in **Kickstart Steps** register (0-7). If register is 0 there is no kickstart current - movement begins at 0.35V.
Scanning	0.35V
Stopped	0.125V for number of steps specified in **Hold Current Timeout** register (0 - 31), 0V after time out. If register is 0 there is no hold current.

Figure 17: Full Step Current Control

3.2 MicroStep Mode

Microstepping is a technique of driving the stepper motor with a staircase approximation of a sine wave, as shown in Figure 18. This technique maximizes the torque of a given motor, resulting in a higher maximum speed. In addition, it increases the resolution of the stepper motor. If a stepper motor moves 3.6° per full step, microstepping can create positions inside the 3.6°: 1.8°, 0.9°, or 0.45°, for example. This increases the maximum vertical resolution of the scanner. Microstepping also results in quieter motor movement.

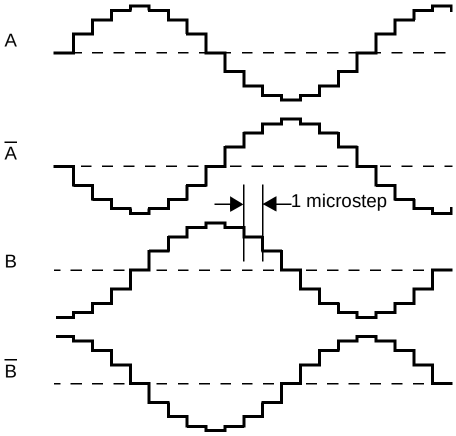


Figure 18: Bipolar Microstepping Waveform

The amplitude of the microstepped sine wave is controlled by the output of the stepper motor DAC (Figure 19). The current in the stepper motor winding is measured as a voltage across the sense resistor, and the transistor drive signals are pulse width modulated (PWM) to force the average current through the winding equal to V_{DAC}/R_{SENSE}. Register 56 controls the frequency of the PWM, and Register 57 controls the minimum time the driver is on every period. Register 57 should be set as short as possible, the driver only needs to be on long enough to mask any transient noise generated by the driver transistor turning on.

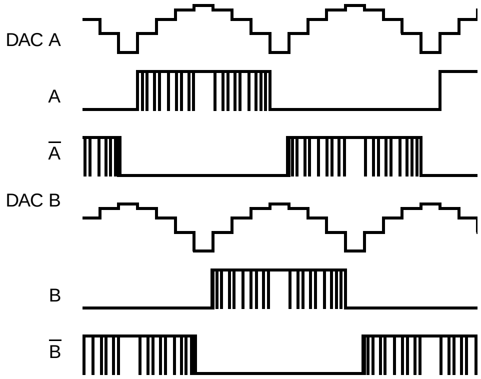


Figure 19: Stepper Motor Waveform - LM9830 Signals

Figure 20 shows the LM9830's DAC voltages. The peak current through the stepper motor winding will be $0.5V/R_{SENSE}$. The table index is incremented every microstep (StepSize pixel periods).

Table Code	A (B)	$\overline{A}$ ($\overline{B}$)	DAC Voltage
0	0	0	N/A
1	1	0	0.191V
2	1	0	0.353V
3	1	0	0.462V
4	1	0	0.500V
-0	0	0	N/A
-1	0	1	0.191V
-2	0	1	0.353V
-3	0	1	0.462V
-4	0	1	0.500V

Figure 20: Microstepping Current Control

3.3 Pause Behavior - Non-Reversing Mode

When the **Full Steps to Reverse When Buffer is Full** register is 0, the stepper motor simply stops moving when the Pause signal is received, as shown in Figure 21. The line of data currently being processed (section "a" in Figure 21) will continue to be processed and stored in SRAM. Additional lines may be digitized and stored as well, depending on the number programmed in the **Lines to Process After Pause Scan Signal** register (Figure 22). This value is different for different scanner designs and should be empirically set to the value that minimizes the spacial distortion created by the motor slowing down and stopping.

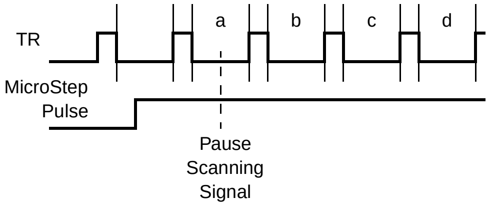


Figure 21: Stepper Motor Stopping

Value	Additional Lines to Store in SRAM
0	0(a only)
1	1 (a and b)
2	2 (a, b and c)
...	...
7	7

Figure 22: Lines to Process after Pause Scan Signal Register

When the Resume Scan signal is received, the stepper motor controller waits the appropriate number of pixel periods after the next TR pulse and then starts stepping again at the normal rate. The first new line transmitted is determined by the **Lines to Discard After Resume Scan Signal** register. The discard value must be the same as the value in the **Lines to Process After Pause Scan Signal** register.

Value	First Line to Transmit After Pause
0	b
1	c
2	d
...	...
7	i

Figure 23: Lines to Discard After Resume Scan Signal Register

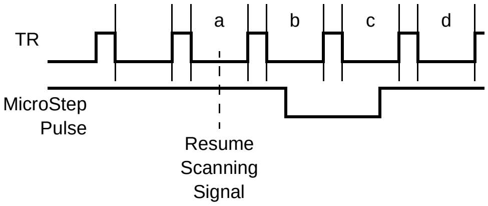


Figure 24: Stepper Motor Resuming

3.4 Pause Behavior - Reversing Mode

If the **Full Steps to Reverse When Buffer is Full** register is >0, then the Reversing Mode is enabled.

The Reversing Mode eliminates spacial distortion due to the pausing of a scan. When the Pause Scan signal is received, the line currently being processed is completed and stored in RAM (line “b” in Figure 25). When the scan resumes, ideally the LM9830 would send out lines “c” and after under the exact same speed and positional conditions the scanner was in before the scan stopped (as indicated by the dotted line in Figure 25).

When the Pause Scan signal is received, the LM9830 sends out the remainder of the line currently being read from the CCD (line b), and stores the offset (in pixel periods) between the last TR pulse and the last step. It then stops, reverses, stops, and waits for the Resume Scan signal. Once Resume Scan is asserted, the motor controller waits for the previously stored number of pixels periods, then starts moving forward again, maintaining the same phase relationship between the TR pulse and the stepper motor control signals. The result is as if the stepper motor had never paused.

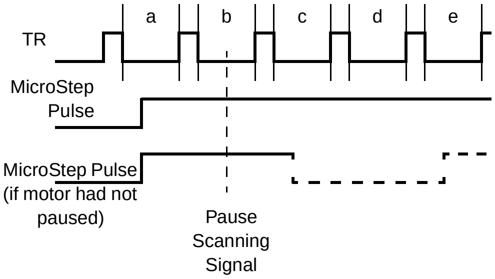


Figure 25: Reversing - The Goal

Stopping, reversing, and resuming forward motion all follow the curve programmed in the **Acceleration Profile** configuration register. There are 3 segments (Stopped, 25%, and 50%), and the number in each register indicates the number of full steps to stay at that acceleration. A value of 0 indicates that that segment is to be skipped. For example, a value of 0 in all three registers would mean that the motor would instantly reverse when the buffer is full, then instantly stop after going back the specified number of lines.

Speed Register	DAC output
Stop (x = 0 to 3)	x = number of full step clocks to wait before reversing motor.
25% (y = 0 to 3)	y = number of full steps at 25% of final speed. Full step period = 4 full step clocks.
50% (z = 0 to 3)	z = number of full steps at 50% of final speed. Full step period = 4 full step clocks.

Figure 26: Acceleration Profile Settings

This acceleration profile is used any time the motor is started, stopped, or reversed.

The acceleration profile for stopping, reversing, stopping, and going forward again is this:

- Full speed forward (1 step = #pixels in **Scanning Step Size** register) until the Pause Scanning signal is received.
- 50% speed forward for z steps (1 step = 2* #pixels in **Scanning Step Size** register)
- 25% speed forward for y steps (1 step = 4*#pixels in **Scanning Step Size** register)
- Stopped for x microsteps (= #pixels in **Scanning Step Size** register).
- 25% speed backward for y steps (1 step = 4*#pixels in **Scanning Step Size** register)
- 50% speed backward for z steps (1 step = 2* #pixels in **Scanning Step Size** register)
- Full speed backward (1 step = #pixels in **Scanning Step Size** register) for number of steps in the **Steps to Reverse** register
- 50% speed backward for z steps (1 step = 2* #pixels in **Scanning Step Size** register)
- 25% speed backward for y steps (1 step = 4*#pixels in **Scanning Step Size** register)

- Paused until a Resume Scan signal is received. During the hold current timeout period, the DAC output is held at 0.125V (the hold current) for FullStep mode, or the DAC outputs are held as they were prior to stopping for the microstep mode. After the hold current timeout period, output drivers A, B, $\overline{A}$, and $\overline{B}$ are deasserted.
- Wait for Resume Scan signal
- Wait for correct number of pixel periods to resynchronize stepper motor with sensor timing.
- 25% speed forward for y steps (1 step = 4*#pixels in **Scanning Step Size** register)
- 50% speed forward for z steps (1 step = 2* #pixels in **Scanning Step Size** register).
- Full speed forward (1 step = #pixels in **Scanning Step Size** register), with TR pulses synchronized to same the position on image that they would have been had scanner not stopped.

The **Lines to Process After Pause Scan Signal**/**Lines to Discard After Resume Scan Signal** register is not used in reversing mode.

3.5 Fast Feed Step Size Register

When the motor is being moved quickly (**Paper Feed to End**/**Paper Feed to Beginning** command or **Steps to Skip at Start of Scan** register), the microstep period comes from this register.

For all other motor movement, the step size is given in the **Scanning Step Size** register.

3.6 Stepper Motor Current Control Using PWM

There is an option to use Pulse Width Modulation of the current in the stepper motor to increase high speed torque, optimize efficiency, and allow use of a lower current, less expensive motor. Precisely controlling the current in the motor provides several benefits. In Full Step Mode, the motor can start moving faster and overcome inertia by increasing the current to the motor to 100% when it is starting from a dead stop. After a programmable number of steps, the inertia is overcome and the current can be reduced to 66% to reduce heat in the stepper motor (allowing a less expensive motor to be used). When stopping the stepper motor, the current is increased to 100% for a short time to overcome the forward momentum, then the motor is held in position with a low-level standby current of 30-40%. If the motor is motionless for more than the Hold Current Timeout period, the current goes to 0%.

In microstepping mode, the PWM is used to approximate a sine wave as shown in Figure 18.

The current control is accomplished by measuring the average motor winding current through a sense resistor to ground, comparing it to a reference voltage, and PWMing the motor driver transistor to force the current to be equal to the reference current. See the **Stepper Motor Current Controller Block Diagram** at the end of this document.

4.0 Scanner Support Functions

4.1 Illumination Control Block

Scanner systems require an illumination source to supply the light to the image being scanned. This source may be white (typically a fluorescent lamp), or red, green, and/or blue LEDs. There are four illumination modes in the LM9830:

Illumination Mode	Description
0	LAMP$_R$, LAMP$_G$, LAMP$_B$ outputs = 0. This is the power-on default.
1	Scanning with white light: LAMP$_R$ and LAMP$_B$ controlled by LAMP On/Off pointers in horizontal pixel counter (as in Mode 3), LAMP$_G$ is a PWM pulse stream
2	Scanning with 3 LEDs in color: LAMP$_R$ turns on for Red lines LAMP$_G$ turns on for Green lines LAMP$_B$ turns on for Blue lines
3	Scanning with 3 LEDs in gray: LAMP$_R$ turns on for all lines LAMP$_G$ turns on for all lines LAMP$_B$ turns on for all lines

Figure 27: Illumination Modes

In Illumination Mode 1, the lamp connected to the LAMP$_R$ pin is controlled by the LAMP$_R$ On/Off settings in the configuration register. The LAMP$_B$ output (if used) is controlled the same way. If the lamp is supposed to be on all the time, then the On setting should be set to a number between 0 and the value in the Line End register, and the Off register should be set to a number greater than the value in the Line End register. Conversely, if the lamp is supposed to be off all the time, then the On setting should be set to a number greater than the value in the Line End register, and the Off register should be set to a number between 0 and the value in the Line End register. The LAMP$_G$ output is a Pulse-Width-Modulated pulse stream whose duty cycle is controlled by the value in the PWM register (0-4095). The duty cycle is therefore equal to the register value/4096. The PWM counter is clocked with the CRYSTAL IN frequency so the output frequency is CRYSTAL IN/4096 (12.2kHz with a 50MHz clock). This PWM output can be used to control the brightness of a fluorescent lamp.

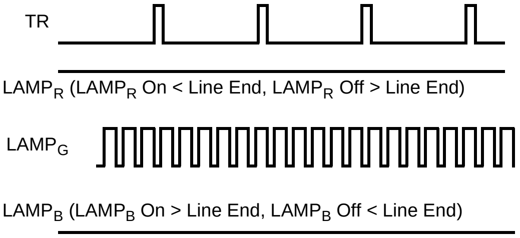

TR
LAMP$_R$ (LAMP$_R$ On < Line End, LAMP$_R$ Off > Line End)
LAMP$_G$
LAMP$_B$ (LAMP$_B$ On > Line End, LAMP$_B$ Off < Line End)

Figure 28: Illumination Mode 1

In Illumination Mode 2 (which is typically used in conjunction with **1 Channel Mode B**), the LAMP$_R$, LAMP$_G$, and LAMP$_B$ outputs are cycled through sequentially, one line at a time. An internal color counter keeps track of the color of the line to be integrated, and takes that color's LAMP output high when the pixel counter reaches the value stored in that color's LAMP On register (Configuration Registers 2C-37). If the On value is greater than the value in the Line End register, then that lamp never turns on. That color's LAMP output goes low when the pixel counter reaches that color's Off value. If the Off value is greater than the value in the Line End register, then the pixel counter will never reach the Off value and the lamp will always stay on. Illumination Mode 2 timing is shown in Figure 29, and in slightly more detail in Figure 41.

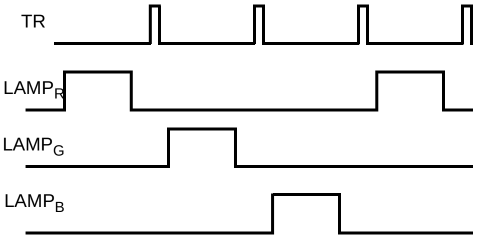


Figure 29: Illumination Mode 2

Illumination Mode 3 is similar to Illumination Mode 2, except that the LAMP outputs for all three colors are turned on and off every line. Illumination Mode 3 timing is shown in Figures 30 and 31.

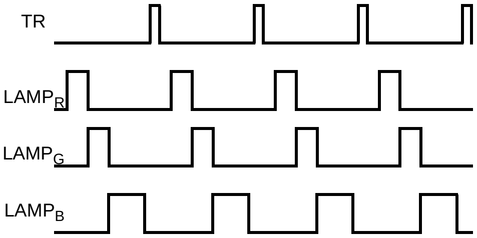


Figure 30: Illumination Mode 3 (grayscale)

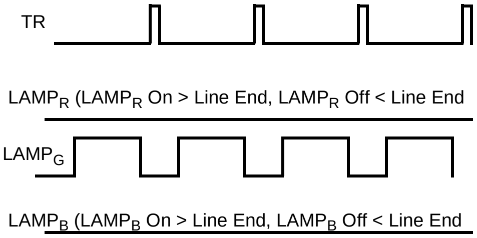

TR
LAMP$_R$ (LAMP$_R$ On > Line End, LAMP$_R$ Off < Line End
LAMP$_G$
LAMP$_B$ (LAMP$_B$ On > Line End, LAMP$_B$ Off < Line End

Figure 31: Illumination Mode 3 (green only)

These modes are in operation whenever the chip is powered on and not in standby mode. For example, the LAMP outputs in Figures 29 and 30 keep pulsing whether the LM9830 is in the Idle, Paper Feed, or Scanning states. This eliminates light amplitude variations due to the lamp/LEDs warm-up characteristics. Since the LAMP pulses are synchronized to the TR pulse, which is determined by the horizontal pixel counter, this means that the pixel counter is constantly running, and any new scans can only be started by waiting for the next new line (the next Red line in the case of Illumination Mode 2).

4.2 CCD/CIS Control Block

This function generates the clock signals necessary to control a CCD or CIS sensor. The LM9830 features:

- Independent control over the polarity (inverting or noninverting) of the input stage to accommodate CIS or CDS signals.
- Ability to turn off CDS. When CDS is on, traditional CDS is performed. When CDS is off, the signal is sampled at the Sample Signal point, but the internal reference is used for the Sample Reference voltage (not a point on the input signal itself).
- The CP1 output supplies the CP pulse needed on some popular Toshiba CCDs. This looks and acts just like another, independent RS pulse.
- A CP2 output is another independent pixel rate pulse that (if needed) can be programmed to supply an additional clock.
- CCD clock signals RS, CP1, CP2 are reset when Line Ends
- The internal Clamp signal is reset with Optical Black Pixels End.
- TR1 and TR2 pulse widths are always the same width, as determined by Register 0E.
- The TR-Ø1 guardband may be equal to 0, causing TR and Ø1 to go high simultaneously and low simultaneously (Figure 32). This is a requirement of some Canon CIS sensors.

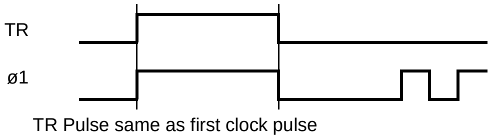


Figure 32: TR-Ø1Guardband Can Be Equal To 0

- CIS TR1 Timing Mode 1. In this mode the TR1 pulse is exactly one Ø clock long, occurring on the rising edge of Ø1. The TR1 pulse width and guardband settings are ignored. For Dyna CIS.

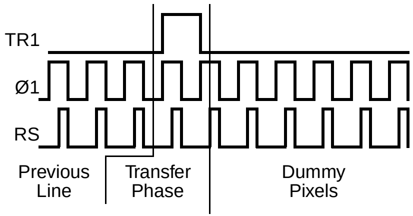


Figure 33: CIS TR1 Timing Mode 1

- CIS TR1 Timing Mode 2. In this mode the TR pulse is again equal to 1 Ø period, but now it is centered around Ø1. The TR pulse width and guardband settings are ignored. For Canon CIS.

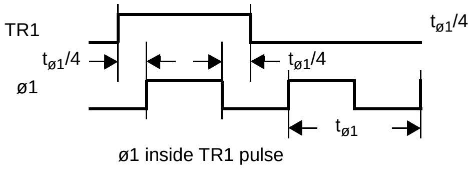


Figure 34: CIS TR1 Timing Mode 2

- To prevent sensor saturation, the LM9830 is always clocking the CCD/CIS, except when it is in Reset or Standby (Register 7 bit 2 or 3 = 1).
- There is a bit for **Fake Optical Black Pixels** (register 19, bit 2). This is used with Dyna CIS sensors. In this mode, the RS output pulses once inside the TR1 pulse, then is held high until the end of the optical black pixels. The TR1 pulse is extended until

the trailing edge of the first RS pulse. This mode works for TR1 only, under all TR1 settings (normal and CIS TR1 Timing modes 1 and 2).

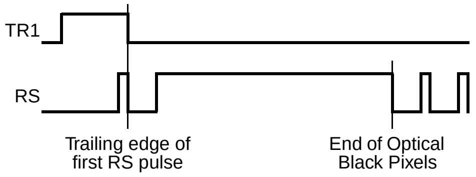

TR1
RS
Trailing edge of first RS pulse
End of Optical Black Pixels

Figure 35: Fake Optical Black Pixels

4.3 AFE Operation

The LM9830 supports the following operation modes, controlled by registers 26 and 27:

- 3 Channel Pixel Rate Mode. In this mode all three channels are converted with the multiplexer in front of the ADC switching at the ADC conversion rate, producing interleaved RGB data that is transferred to RAM. The ADC runs at MCLK/8, each channel's pixel rate is MCLK/24. Each color has its own offset and gain coefficients. This mode typically uses Illumination Mode 1.

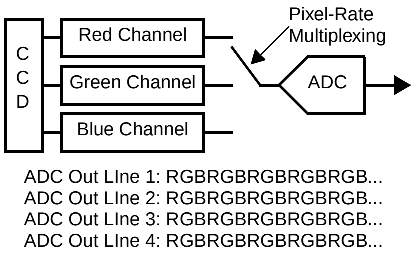

C
C
D
Red Channel
Green Channel
Blue Channel
Pixel-Rate Multiplexing
ADC
ADC Out LIne 1: RGBRGBRGBRGBRGB...
ADC Out LIne 2: RGBRGBRGBRGBRGB...
ADC Out LIne 3: RGBRGBRGBRGBRGB...
ADC Out LIne 4: RGBRGBRGBRGBRGB...

Figure 36: 3 Channel Pixel Rate Mode

- 3 Channel LIne Rate Mode. In this mode all three channels are converted with the multiplexer in front of the ADC switching at the line rate, producing a line of Red data, followed by a line of Green data, followed by a line of Blue data, etc. that is transferred to RAM. The selected channel and the ADC both run at MCLK/8. Each color has its own offset and gain coefficients. This mode typically uses Illumination Mode 1.

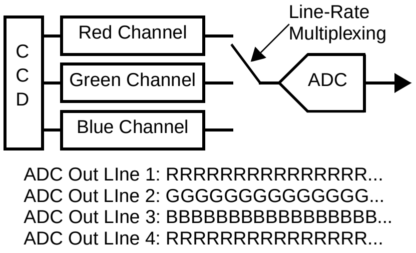

C
C
D
Red Channel
Green Channel
Blue Channel
Line-Rate Multiplexing
ADC
ADC Out LIne 1: RRRRRRRRRRRRRRR...
ADC Out LIne 2: GGGGGGGGGGGGGG...
ADC Out LIne 3: BBBBBBBBBBBBBBBB...
ADC Out LIne 4: RRRRRRRRRRRRRRR...

Figure 37: 3 Channel Line Rate Mode

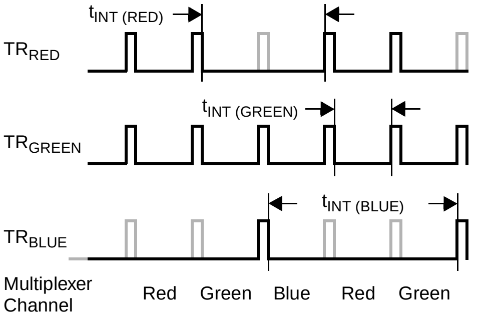

$t_{INT (RED)}$
TR_{RED}
$t_{INT (GREEN)}$
TR_{GREEN}
$t_{INT (BLUE)}$
TR_{BLUE}
Multiplexer Channel
Red
Green
Blue
Red
Green

Figure 38: 3 Channel Line Rate TR Pulse Timing

In the 3 Channel Line Rate Mode three TR pulses are generated. TR_{RED} is the TR1 output, TR_{GREEN} is the TR2 output, and TR_{BLUE} is the CP2 output. In this mode TR pulses for a particular color can be “skipped”, increasing the integration time for that color. In the example shown in Figure 38, the red channel sees 2 times the integration time of the green channel, and the blue channel sees 3 times the integration time of the green channel. Each channel can be independently programmed to drop 0, 1, or 2 TR pulses.

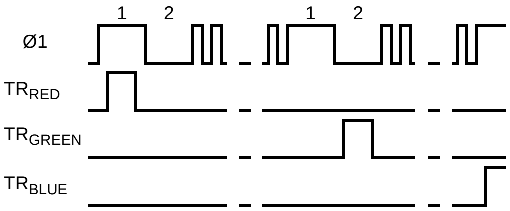

1
2
1
2
Ø1
TR_{RED}
TR_{GREEN}
TR_{BLUE}

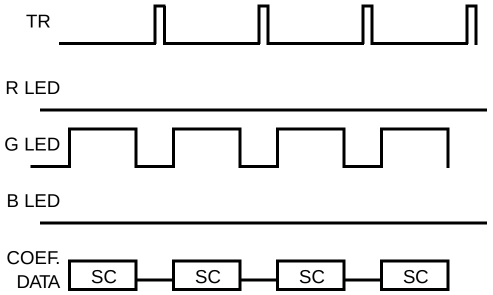
Figure 39: 3 Channel Line Rate Mode with 2 TR Pulse Positions

Each color's TR pulse can be programmed to occur in position 1 (inside Ø1 high) or position 2 (inside Ø1 low), as shown in Figure 39.

- 1 Channel Mode. In this mode only one of the three channels is being converted. That channel and the ADC are clocked at MCLK/8. The channel is chosen in the configuration register.

There are two variations of 1 Channel Mode:

- 1 Channel Mode A: Uses the selected channel's offset and gain coefficients for all lines. This mode typically uses Illumination Mode 3.



SC = selected channel (=green in this example)

Figure 40: 1 Channel Mode A

- 1 Channel Mode B: This mode uses a sensor tied to the Blue OS input only. Illumination is switched in RGBRGB pattern at the line rate. Each color has own digital offset and gain coefficients as well as static Gain and Offset data. Note that there is a one line delay between when a line is exposed to a color and when pixels of that color are clocked out of the sensor. For example, the Green LEDs should be on while you are clocking out Red pixels. This mode typically uses Illumination Mode 2.

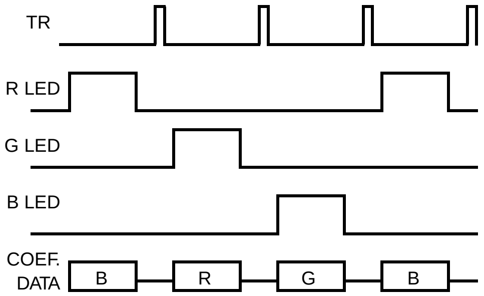


Figure 41: 1 Channel Mode B

4.4 External SRAM Interface

The external 8 bit SRAM is used for line buffering and coefficient data. For 300 dpi, 16kbytes (2729 pixels * 16 bits/pixel * 3 colors = 16kbytes) are used for offset and gain coefficients. For 600 dpi, 32Kbytes (5460 pixels * 16 bits/pixel * 3 colors = 32kbytes) are used for offset and gain coefficients. The rest is used for the circular image data buffer.

The LM9830 supports three SRAM sizes: 64K, 128K, and 256K.

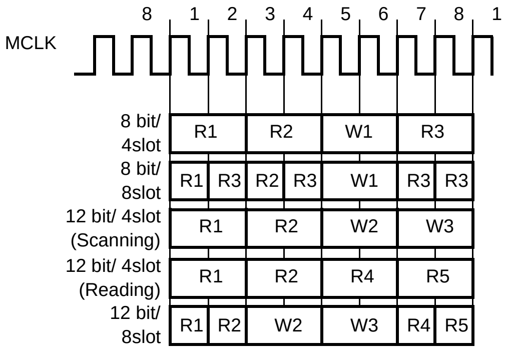
The 64K mode uses addresses A0-A15. To allow two 32k x 8 SRAMs to function as one 64k x 8 SRAM, address bit A16 is the inverse of address bit A15. This allows A15 and A16 to be used as $\overline{CS}$ pins for the two 32k x 8 SRAMs. The 64K mode is only recommended for use with 300dpi optical sensors. 64K (32K coefficients/32K image data buffer) is not enough SRAM for 600dpi sensors.

The 128K mode uses addresses A0-A16. To allow two 64k x 8 SRAMs to function as one 128k x 8 SRAM, address bit A17 is the inverse of address bit A16. This allows A16 and A17 to be used as $\overline{CS}$ pins for the two 64k x 8 SRAMs.

The 256K mode uses addresses A0-A17.

There are 4 SRAM access modes: 8 bit/4 slot, 8bit/8 slot, 12 bit/4 slot (half duplex 12 bit), 12 bit/8 slot (full duplex 12 bit). The 4 slot modes are lower bandwidth and can be used with slower SRAM, while the 8 slot modes provide higher system performance.

Figure 42 indicates the relative bandwidth used in each mode.



R1: Offset Coefficient read
R2: Gain Coefficient read
R3: 8 bit pixel data read (to host)
R4: 12 bit pixel data read, MSB (to host)
R5: 12 bit pixel data read, LSB (to host)
W1: 8 bit Pixel Data Write
W2: 12 bit pixel data write, MSB
W3: 12 bit pixel data write, LSB

Figure 42: SRAM Access Modes

The ADC and the first stage of the digital processing block always run at the pixel rate, which is 1/8 of the MCLK frequency. The offset correction data and the gain correction coefficient data must be provided at the pixel rate.

In the 8 bit/4 slot mode, each 8 bit correction data RAM access takes 2 MCLKs. The 8 bit write from the pixel processing block takes 2 MCLKs. 8 bit reads from SRAM to the host also take 2 MCLKs. Note that in this mode, the maximum rate pixel data can be stored in SRAM is also the maximum rate pixel data can be read and transmitted to the host. In configurations where the host I/O can not constantly receive data at the pixel rate, the SRAM buffer may fill up even if the host is capable of burst reads at rates much greater than the pixel rate.

To reduce or eliminate buffer full conditions, there is a higher bandwidth 8 bit/8 slot mode where all RAM read accesses take 1 MCLK cycle. In this mode there are 4 slots where data can be read and sent to the host, allowing the buffer to be emptied up to 4 times faster than it is being filled. Combined with an intelligent scanner driver routine, this mode will reduce or eliminate the number of times a scanner has to stop during a scan. *This mode is only guaranteed to work when the MCLK frequency is 25MHz or lower.*

To calibrate the scanner, or to actually scan an image and send the raw 12 bit data back to the PC, additional modes are required to transmit the 12 bit pixel data through the 8 bit interface. The 12 bit/4 slot (or half duplex) mode does this by storing the 12 bit data as a high byte (the 4 MSBs of the 12 bit word) and a low byte (the 8 LSBs of the 12 bit word). The timing is similar to the 8 bit/4 slot scenario, except that the slot normally allocated to sending data to the host is now given to writing the second half of the 12 bit word to SRAM. *In this mode you can not transmit data to the host while scanning.* To read the data out of RAM, you must either write to the command register to stop scanning (this is typically how it would be done during calibration), or wait until the buffer fills up (how it would typically be done during a raw 12 bit image scan).

To improve the performance of this mode, there is also a 12 bit/8 slot (full duplex) mode available. In this mode coefficient reads take 1 MCLK each (a total of 2 MCLKs). The high and low bytes of the 12 bit word are each read from RAM and transmitted to the host in 1 MCLK cycle. To slightly reduce the speed requirements of SRAM, the high and low byte writes to RAM are given 2 MCLKs each. This allows the host to read pixel data from the SRAM while scanning, dramatically reducing the time required to scan versus using the half duplex mode.

To minimize EMI and on-chip noise, the SRAM output drivers (A0-A17, DB0-DB7, and $\overline{RD}$ and $\overline{WR}$) have four output current settings, 0-3. The output current level is set by bits 2 and 3 of Configuration Register 43.

Current Setting	I_{OL} (mA)	I_{OH} (mA)	t_F (ns) 20pF	t_R (ns) 20pF
0	3.5	-4	29	25
1	6	-7.5	17	13
2	12	-17	8	6
3	21	-32	5	3

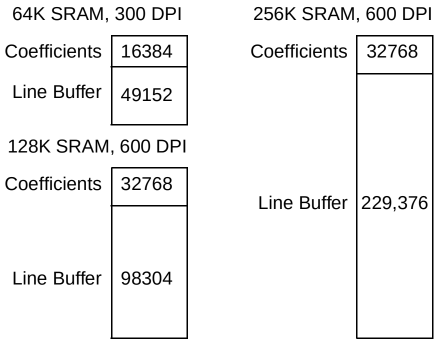


Figure 43: Typical Memory Maps for External SRAM

4.5 Misc. I/O

These four pins are used for paper sensing, LED displays, user start buttons, etc.

Two pins are dedicated inputs: Paper Sensor #1 and Paper Sensor #2. The other two pins, Misc I/O #1 and Misc I/O #2, can be configured as inputs or outputs.

The state of each pin, True or False (1 or 0), is reflected in the Status Register.

These are the configurable aspects of these I/O pins:

- The polarity of the input. If this bit is set to a 1 (Active High), a high level on that input pin will produce a True reading (1) in the Status Register. If this bit is set to a 0 (Active Low), a low level on that input pin will produce a True reading (1) in the Status Register.
- Level or Edge Sensitive. If this bit is set to 0 (Level Sensitive), the Status Register will reflect the current state at that sensor input pin. If this bit is set to 1 (Edge Sensitive), the Status Register for that input will be True (1) if there were any False to True transitions at that sensor input pin since the last time the Status Register was read. Reading the status register clears the state of all the edge sensitive inputs to False (0).
- Paper Sensor #1 can be programmed to stop the scan (by clearing the Scanning bit) when its state (as reflected in the Status Register) changes from False to True. This is useful in flatbeds to prevent the motor from trying to step past the limits of travel of the system. In sheetfed systems, Paper Sensor #1 can be used to detect whether or not the user has inserted a document to be scanned.
- Paper Sensor #2 can be programmed to stop the scan (by clearing the Scanning bit) and change its bit in the Status Register to True a programmable number of lines after its input pin changes state from False to True. In sheetfed scanners this is useful if the paper sensor is located *before* the scanner array, where the sensor will change states before all of the paper has been scanned. For flatbed scanners this sensor can be used to detect the home position.
- The Misc I/O 1 and Misc I/O 2 pins can have their outputs set to +5V or 0V by writing a 1 or a 0 to the appropriate register.

4.6 The Brains

This is the master control section that keeps track of the position of the CCD pixel going through the analog front end, the color of that line of CCDs (for single output CCD illumination control), the stepper motor, and all other system coordination.

5.0 Communicating with the LM9830

Everything on the LM9830 (configuration registers, image data, coefficient data, and gamma tables) is accessed through the Configuration Register. Configuration Register I/O is done through two steps. The first step is to write the address (0 through 7F) of the configuration register to be read from or written to. The second access is the data operation (a read or a write) for that address. The address only needs to be written once. After an address is written, any number of reads and/or writes may be made to that address.

Registers 0, 1, and 2 are read-only registers. Writing to these addresses may affect various counters inside the LM9830 and should therefore be avoided. All of the remaining configuration registers can be read from and written to using this protocol.

5.1 The DataPort: Reading and Writing to Gamma, Offset, and Gain Memory

Because the gamma table and the shading and offset correction blocks of RAM are very large, the LM9830 uses an indexed method of reading and writing them, called the DataPort. Four addresses in the Configuration Register are used to implement this mode, as shown in Figure 44.

Configuration Register Address	Name	Bits
3	DataPort Target/ Color	b3- b0
4	DataPort Address (MSB)	b12 - b8

Figure 44: DataPort

Configuration Register Address	Name	Bits
5	DataPort Address (LSB)	b7 - b0
6	DataPort	b7 - b0

Figure 44: DataPort

The DataPort allows the user to select a memory block (gamma, gain coefficient, or offset coefficient) and color (red, green, or blue) to be read from or written to, by writing to Configuration Register Address 3.

The starting address of that block (usually 0) is written into the DataPort Address register (at Configuration Register Addresses 4 and 5). Bit D5 of register 4 should also be set to a 0 or a 1 to indicate whether the DataPort will be read from (D5 = 1) or written to (D5 = 0) in subsequent operations. This is required so the LM9830 can prefetch the data for faster access. The DataPort Address is automatically incremented after every byte of Gamma data read/written, or every 2 bytes of Offset/Shading data read/written (since an Offset/Shading word is 2 bytes wide).

Once the memory block, color, and starting address is written, a series of reads or writes to the DataPort will read from or fill up that selected memory block at maximum speed.

Registers 4 and 5 should always be (re)written to after register 3 has been changed.

5.1.1 DataPort Type and Color

These 3 bits determine which memory block (gamma or gain/offset coefficients, Figure 45) and which color of that memory block (red, green, or blue, Figure 46) is to be read from or written to. There is one exception to this: when operating the LM9830 in 1 Channel Mode A, the color is determined by the contents of Register 26, bits 3 and 4.

7	6	5	4	3	2	1	0	Type
-	-	-	-	-	-	-	0	Gamma
-	-	-	-	-	-	-	1	Offset & Gain

Figure 45: DataPort Target Pointer

7	6	5	4	3	2	1	0	Color
-	-	-	-	-	0	0	-	Red
-	-	-	-	-	0	1	-	Green
-	-	-	-	-	1	0	-	Blue
-	-	-	-	-	1	1	-	Undefined

Figure 46: DataPort Color Pointer

5.1.2 DataPort Address

This 13 bit register (at Configuration Register addresses 4 and 5) determines what the starting address is for the read/write operation. *This address is automatically incremented after each read/write operation to the actual DataPort.* For the gamma table the range is 0 to 1023. For the Gain and Offset Coefficients this range is 0 (corresponding the first valid pixel as programmed in the Valid Pixels Start register) to 2729 (the maximum number of image pixels for a 300dpi sensor) or 5460 (the maximum number of image pixels for a 600dpi sensor). If reads or writes continue past 1023, 2729, or 5460, the DataPort address counter wraps back around to 0 and continues counting. Note that for Gain and Offset Coefficients it takes 2 read/write operations to increment the address counter, because Gain and Offset Coefficients are stored as a 2 byte word.

5.1.3 DataPort

This 8 bit register (at Configuration Register address 6) is where the data is sequentially read from or written to. Gamma data is 8 bits wide. Since offset data may be 6 or 8 bits wide and gain correction data may be 10 or 8 bits wide, these bytes need to be combined before they are transmitted. For a 6/10 offset/gain bit split, the format is shown in Figure 47:

7	6	5	4	3	2	1	0	Type
O5	O4	O3	O2	O1	O0	G9	G8	First Byte
G7	G6	G5	G4	G3	G2	G1	G0	Second Byte

Figure 47: DataPort Target Pointer (6/10 split)

The first byte = Offset * 4 + INT(Gain/256), and

The second byte = Gain AND 255.

An 8/8 offset/gain split is more obvious:

7	6	5	4	3	2	1	0	Type
O7	O6	O5	O4	O3	O2	O1	O0	First Byte
G7	G6	G5	G4	G3	G2	G1	G0	Second Byte

Figure 48: DataPort Target Pointer (8/8 split)

If the offset/gain split is changed from 8/8 to 6/10, or from 6/10 to 8/8, the offset and gain coefficients must be re-calculated and resent to the LM9830.

In Gamma mode, the DataPort address counter is automatically incremented after a byte is read from or written to register 6. In Gain/Offset mode, the DataPort address counter is automatically incremented after two bytes are read from or written to register 6.

Reading and writing the DataPort should only be done when the LM9830 is not scanning.

6.0 The Parallel Port Interface

The primary interface of the LM9830 is a PC compatible parallel port interface. This communication mode is selected by tying the CMODE pin to DGND. There are two operational parallel port modes for reading data: Nibble Mode (for compatibility with the maximum number of existing PCs) and EPP (for maximum speed on newer machines). In addition, the LM9830 supports a printer passthrough function that allows an LM9830-based scanner to be inserted between a PC and a printer.

6.1 The Parallel Port Pins

The parallel port on a standard PC has a total of 17 I/O lines: 8

data lines and 9 signaling lines. Additionally, the parallel port passthrough function requires another set of the 9 control signals. The LM9830 databus and control signals are tied to the PC's parallel port. To support a parallel port passthrough function, the LM9830's control outputs are tri-stated to allow the printer to communicate with the PC when in passthrough mode. When the LM9830 is active, the printer is disabled by tri-stating all control I/O between the printer and the LM9830/PC control bus. A more detailed description of the parallel port passthrough function is provided on the full page drawing labelled **Printer Passthrough Block Diagram** near the end of this document.

Name	**Direction**	**LM9830 Default**
Parallel Port Databus		
D0-D7	From (To) PC	TriState
PC Control Signals		
STROBE	From PC	Input
AUTOFEED	From PC	Input
INIT	From PC	Input
SELECT IN	From PC	Input
ACK	To PC	High
BUSY	To PC	Low
PE	To PC	Low
SELECT	To PC	Low
ERROR	To PC	High
Printer Passthrough Signals		
TRISTATE	To External Buffer	Low
LATCH	To External Latch	Low

Figure 49: Printer Port Pin Description

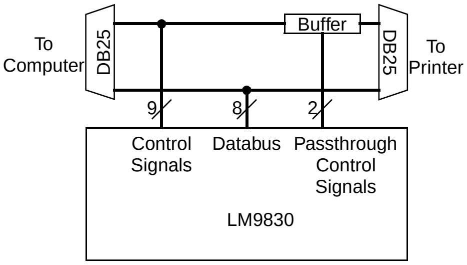


Figure 50: Printer Passthrough Overview

To minimize EMI and on-chip noise, the Parallel Port output drivers (D0-D7 and the 9 control/status output signals) have four output current settings, 0-3. The output current level is set by bits 1 and 2 of Configuration Register 42.

Current Setting	**I_{OL} (mA)**	**I_{OH} (mA)**	**t_F (ns) 200pF**	**t_R (ns) 200pF**
0	5	-6	200	167
1	7	-9	143	111
2	9	-12	111	83
3	15	-21	67	48

For maximum compatibility and reliability, the "3" setting is recommended. "0" - "2" can be used to reduce EMI and on-chip noise if the final system (customer's PC and associated peripherals and cables) can tolerate it.

6.2 Finding the LM9830

The LM9830 powers up in the Transparent mode. In order to communicate with the LM9830, the host must send a specific sequence of data on the databus without changing any of the 4 control signal lines. The LM9830 looks for the sequence 99 66 CC 33 on D0-D7.

Each state (99, 66, CC, and 33) must be held for a minimum of 4 MCLK cycles. After a power on reset status, the MCLK divider is set to divide-by 4. This means that each state must be held for 16 CRYSTAL IN cycles. For a 50MHz external clock, this means that each state must be held for a minimum of 16*20ns = 320ns. If the MCLK divider is programmed to a different value and the LM9830 goes transparent, the minimum time required to wake up the LM9830 will change. The equation for the length of time each state must be held is:

$$t = 4(t_{CLK\_IN})(MCLK\_DIVIDER)$$

The assumption is that this sequence will not occur at random without any of the 4 control pins violating their static requirement (STROBE high, the other three static).

When in the transparent mode with a clock applied, the LM9830 constantly monitors the databus for a transition to 99. If 99 is detected, the LM9830 looks for 66. If 66 is detected, the LM9830 looks for CC. If CC is detected, the LM9830 looks for 33.

If 33 is detected, the LM9830 exits transparent mode.

When the LM9830 exits the Transparent mode it takes the TRISTATE pin high to disconnect the printer control signals to the PC, and the $\overline{\text{LATCH}}$ signal low to latch and hold the current state of the four control signals going to the printer. The 5 control lines going back to the host change to their deasserted states:

$\overline{\text{ERROR}}$ = high

$\overline{\text{ACK}}$ = high

BUSY = low

PE = low

SELECT = low

At this point the LM9830 software driver can attempt to write to and read from the configuration register to confirm the presence/non-presence of the LM9830. Please note that register 42 must be written correctly to allow the LM9830 to respond in the desired communication mode (8 bit or nibble).

6.3 Selecting EPP or Nibble Mode I/O

Now that the LM9830 has been detected, the Host can start talking to it. The host PC always writes to the LM9830 using 8 bit words. For reading data, the LM9830 can communicate in either 8 bit (Bidirectional or EPP) or 4 bit (Nibble) modes, as determined by the state of register 42, bit 0. This bit has no power-on default and must be set to a 0 or a 1 before data can be read from the LM9830.

6.4 Returning to Transparency Mode Without LM9830 Reset

The host can return the LM9830 to Transparency Mode by taking the $\overline{\text{INIT}}$ pin low and then high again. Approximately 2 - 3 MCLKs after the rising edge of $\overline{\text{INIT}}$, the $\overline{\text{LATCH}}$ pin will go high, the TRISTATE pin will go low, and the LM9830 will tristate its D0-D7 and control line outputs. This will make the LM9830 transparent, but will not change its operation state. If it was scanning, idling, or fast feeding, the LM9830 will continue scanning, idling, or fast feeding.

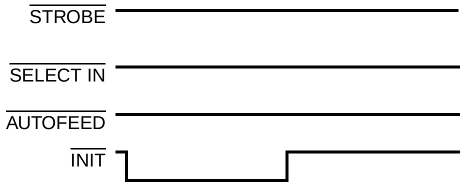


Figure 51: LM9830 Transparent without Reset

6.5 Returning to Transparency Mode with LM9830 Reset

The host can return the LM9830 to Transparency Mode and reset the LM9830 by taking the INIT, AUTOFEED, SELECT_IN, and STROBE pins low and then high again. Approximately 2 - 3 MCLKs after the rising edge of INIT, the LATCH pin will go high, the TRISTATE pin will go low, and the LM9830 will tristate its D0-D7 and control line outputs. This will reset the LM9830 as well as make it transparent.

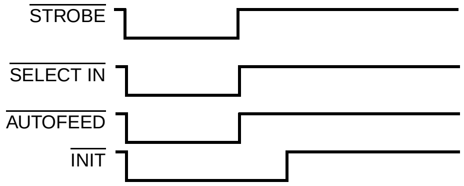


Figure 52: LM9830 Transparent with Reset

6.6 Writing to the Configuration Register (Parallel Port)

The timing for writing to the LM9830 (sending data from the PC to the LM9830) is shown in Figure 53. This is EPP timing, and it is used for all parallel port Writes, even when in Nibble Mode (Nibble Mode is only used to send data from the peripheral to the host).

The write consists of two cycles, an address write cycle that tells the LM9830 which address is going to be written to, and a data write cycle that transmits the data to be stored in that address. The handshaking is as follows:

- The host takes STROBE low, indicating that the next operation is a write.
- The host puts data on D0-D7.
- The host takes SELECT IN low to indicate that the data is valid.
- The LM9830 latches the data and indicates that the data has been latched by taking BUSY high.
- The host responds and brings SELECT IN and STROBE high.
- The LM9830 responds to the rising edge of SELECT IN by taking BUSY low.

This completes the address write cycle. The LM9830 is now prepared for a byte write to the location contained in the address byte. The handshaking for the data write is basically identical, except AUTOFEED is used to latch the data instead of SELECT.

To write large quantities of data to a particular address, the address only has to be written once. All data write operations will write to the last address written. This is useful for writing DataPort (register 06) data.

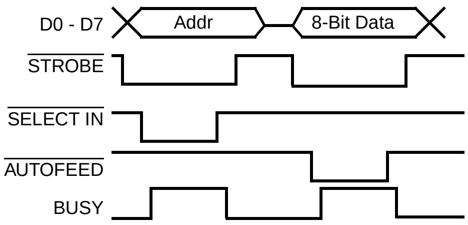


Figure 53: Writing to the Configuration Register

6.7 Reading From The Configuration Register (Parallel Port)

The procedure for reading the configuration register is different for the EPP and Nibble Modes.

6.7.1 EPP Mode Configuration Register Read

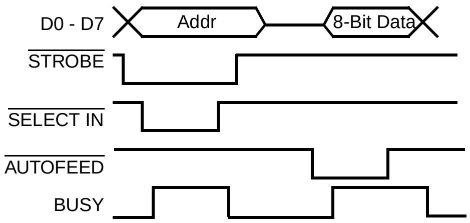


Figure 54: Reading from the Configuration Register (EPP)

An EPP read is shown in Figure 54. The handshaking for the address write cycle of a read is identical to the address cycle for a write. The data read cycle is as follows:

- The host maintains STROBE high, indicating that the next operation is a read.
- The host tristates D0-D7
- The host takes AUTOFEED low to request data from the LM9830.
- The LM9830 places the data on the bus.
- The LM9830 takes BUSY high to indicate the data is valid.
- The host latches the data and responds by taking AUTOFEED high.
- The LM9830 tristates the bus.
- The LM9830 takes BUSY low to indicate the cycle is complete and it is ready for another cycle.

To read large quantities of data from a particular address, the address only has to be written once. All data read operations will read from the last address written. This is useful for reading pixel (register 00) and DataPort (register 06) data.

6.7.2 Nibble Mode Configuration Register Read

This is not the traditional application of “Nibble Mode”, it is more efficient and lower cost variation. The first half of the cycle is an EPP address write, followed by a Nibble Mode read. Also, BUSY is used for handshaking and ACK for a databit, eliminating the problems caused by the hardware inversion of BUSY on the PC, as well as allowing BUSY to perform roughly the same function it does in EPP mode.

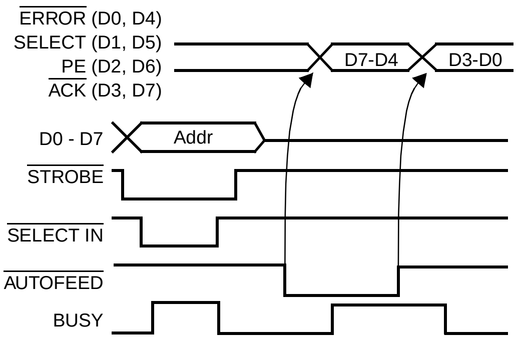

$\overline{\text{ERROR}}$ (D0, D4)
SELECT (D1, D5)
PE (D2, D6)
$\overline{\text{ACK}}$ (D3, D7)
D7-D4
D3-D0
D0 - D7
Addr
$\overline{\text{STROBE}}$
$\overline{\text{SELECT IN}}$
$\overline{\text{AUTOFEED}}$
BUSY

Figure 55: Reading from the Configuration Register (Nibble Mode)

An EPP read is shown in Figure 55. The handshaking for the address cycle of a read is identical to the address cycle for a write. The data cycle is as follows:

- The host takes $\overline{\text{STROBE}}$ high, indicating that the next operation is a read.
- The host tristates D0-D7
- The host takes $\overline{\text{AUTOFEED}}$ low to request the first nibble from the LM9830.
- The LM9830 places the first nibble on the $\overline{\text{ERROR}}$, SELECT, PE, and $\overline{\text{ACK}}$ pins.
- The LM9830 takes BUSY high to indicate the nibble is valid.
- The host latches the nibble on or after the rising edge of BUSY.
- The host takes $\overline{\text{AUTOFEED}}$ high to request the second nibble from the LM9830.
- The LM9830 places the second nibble on the $\overline{\text{ERROR}}$, SELECT, PE, and $\overline{\text{ACK}}$ pins.
- The LM9830 takes BUSY low to indicate the nibble is valid.
- The host latches the nibble on or after the falling edge of BUSY.

Additional nibble reads will read from the last latched address (useful for reading pixel data or the DataPort).

7.0 The Microprocessor Compatible Interface

In this interface the part is written to like a standard µP peripheral, with $\overline{\text{RD}}$ ($\overline{\text{AUTOFEED}}$), $\overline{\text{WR}}$ ($\overline{\text{STROBE}}$), $\overline{\text{CS}}$ ($\overline{\text{INIT}}$), ALE ($\overline{\text{SELECTIN}}$), and an 8 bit databus (D0-D7). This interface would be used in a system where another interface (perhaps SCSI or FireWire) was desired. Using the LM9830 in this application in a DMA mode is relatively easy and efficient, because large blocks of image data can easily be read through a series of $\overline{\text{RD}}$s.

To enter the µP interface mode, the CMODE pin should be tied to V_D.

7.1 Writing to the Configuration Register (µP Mode)

The Configuration Register address is latched on the falling edge of ALE. Data is written to that address on the rising edge of $\overline{\text{WR}}$.

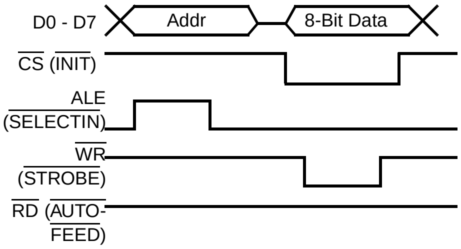

D0 - D7
Addr
8-Bit Data
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
ALE
($\overline{\text{SELECTIN}}$)
$\overline{\text{WR}}$
($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$ ($\overline{\text{AUTO-FEED}}$)

Figure 56: Writing to the Configuration Register (µP)

7.2 Reading From The Configuration Register (µP Mode)

The address is latched as in the previous example. For all modes except DataPort operations, the LM9830 transmits the data at that address on the following read. Additional nibble reads will read from the last latched address (useful for reading pixel data).

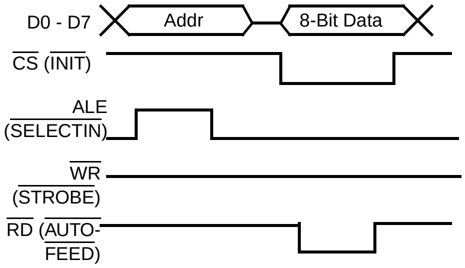

D0 - D7
Addr
8-Bit Data
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
ALE
($\overline{\text{SELECTIN}}$)
$\overline{\text{WR}}$
($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$ ($\overline{\text{AUTO-FEED}}$)

Figure 57: Reading from the Configuration Register (µP mode, except DataPort)

7.3 Writing Data to the DataPort (µP Mode)

The DataPort is used to write the gamma table and the offset/gain coefficients to the LM9830 in a continuous stream. First, write to register 3 to set what the data is (gamma or offset/gain) and what color (red, green, or blue) the data is for. Then write to registers 4 and 5 to set the initial address (usually 0), and the R/W mode (W in this example). To write data to the DataPort, send the Data address (6) to the DataPort followed by a serial stream of data as shown in Figure 58. The DataPort Address stored in registers 4 and 5 will be automatically incremented after every write (if writing gamma data) or every second write (if writing offset/gain coefficient words).

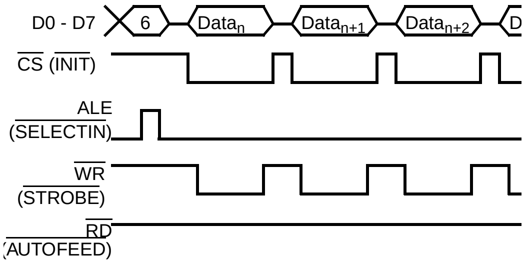

D0 - D7
6
Data_n
Data_{n+1}
Data_{n+2}
D
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
ALE
($\overline{\text{SELECTIN}}$)
$\overline{\text{WR}}$
($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$
($\overline{\text{AUTOFEED}}$)

Figure 58: Writing to the Configuration Register (µP)

7.4 Reading Data from the DataPort (µP Mode)

The gamma table and offset/gain coefficients can also be read from the LM9830 in a continuous stream. First, write to register 3 to set what the data is (gamma or offset/gain) and what color (red, green, or blue) the data is for. Then write to registers 4 and 5 to set the initial address (usually 0), and the R/W mode (R in this case). To read data from the DataPort, the DataPort address (6) needs to be inserted before every read to prefetch the data from the external SRAM. The timing is shown in Figure 59. Note that this applies *only* to offset and gain coefficient reads; the gamma table may be read with or without the additional address writes. The DataPort Address stored in registers 4 and 5 will be automatically incremented after every read (if reading gamma data) or every second read (if reading offset/gain coefficient words).

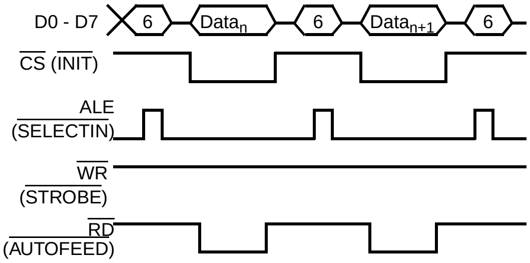

D0 - D7
6
Data_n
6
Data_{n+1}
6
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
$\overline{\text{ALE (SELECTIN)}}$
$\overline{\text{WR}}$
($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$
($\overline{\text{AUTOFEED}}$)

Figure 59: Reading Gain and Offset Coefficients through the DataPort (µP mode)

8.0 Scanning

8.1 Start Scanning - Initiating an Image Scan

An image scan is started by setting the Scanning bit in the Configuration Register. The LM9830 will move the paper forward the number of steps specified in the Stepper Motor Configuration register and begin scanning. Scanning ends when the host writes a new command to the command register (Idle, Paper Feed to Start or Paper Feed to End) or when Paper Sensor #1 or Paper Sensor #2 changes state (if programmed to do so).

The line buffer is reset when the Scanning bit is SET, not when it is cleared. The host can continue to read stored data out of the line buffer after a scan has stopped.

The LM9830 pixel data is read from configuration register address 00. To read pixel data, the host should latch address 00 into the LM9830's address pointer. Subsequent reads from the host will read the next byte of pixel data stored in the line buffer. Here are examples of two consecutive image data reads in the three possible interface modes:

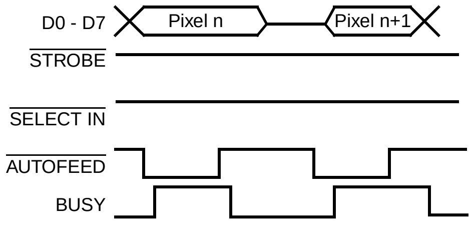

D0 - D7
Pixel n
Pixel n+1
$\overline{\text{STROBE}}$
$\overline{\text{SELECT IN}}$
$\overline{\text{AUTOFEED}}$
BUSY

Figure 60: Reading Pixel Data (EPP)

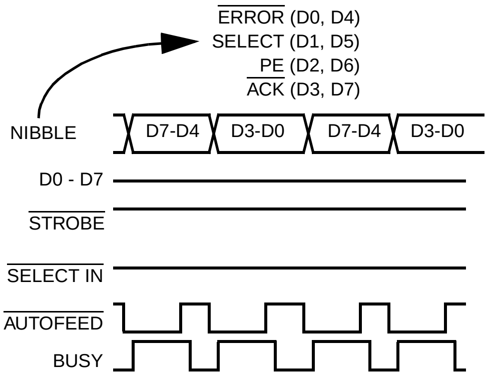

$\overline{\text{ERROR}}$ (D0, D4)
SELECT (D1, D5)
PE (D2, D6)
$\overline{\text{ACK}}$ (D3, D7)
NIBBLE
D7-D4
D3-D0
D7-D4
D3-D0
D0 - D7
$\overline{\text{STROBE}}$
$\overline{\text{SELECT IN}}$
$\overline{\text{AUTOFEED}}$
BUSY

Figure 61: Reading Pixel Data (Nibble Mode)

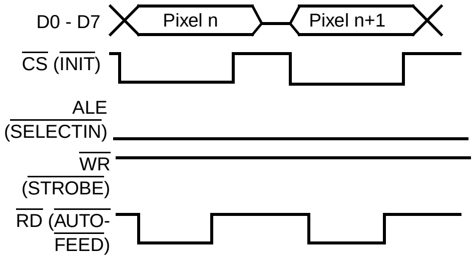

D0 - D7
Pixel n
Pixel n+1
$\overline{\text{CS}}$ ($\overline{\text{INIT}}$)
$\overline{\text{ALE (SELECTIN)}}$
$\overline{\text{WR}}$
($\overline{\text{STROBE}}$)
$\overline{\text{RD}}$ ($\overline{\text{AUTO-FEED}}$)

Figure 62: Reading Pixel Data (µP)

Image data can flow as fast as possible from the LM9830 to the host, but can be interrupted at any time (by latching a different address) to read the LM9830's status registers, abort the scan, etc.

If for some reason you want to pause the scan for some length of time and resume later, do NOT reset the Scanning bits (return to Idle). Simply stop reading pixel data. When the buffer fills up, the LM9830 will automatically stop scanning and turn off power to the stepper motor (when the delay goes beyond the time specified in the **Hold Current Timeout** register).

The last byte of every line is the status byte (register 02). If the line just transmitted was the beginning of a stepper motor pause or reverse cycle, the **Pause** bit is set. For scanners unable to reverse, this feature potentially allows the software to correct images distorted by motor starting/stopping.

8.2 Reconstructing the Image Data Received By the PC

When reconstructing an image from the stream of data received from the LM9830, it is useful to know the format of the data. The LM9830 does not perform deinterleaving on the pixel data, it comes out exactly as the sensor sends it. Deinterleaving and other processing must be performed on the host PC.

For a single output CCD/CIS that outputs one line of data with colors alternating at the line rate, the output format is:

$R_1, R_2, R_3, R_4, \ldots, R_{n-2}, R_{n-1}, R_n$ (line m)

$G_1, G_2, G_3, G_4, \ldots, G_{n-2}, G_{n-1}, G_n$ (line m + 1)

$B_1, B_2, B_3, B_4, \ldots, B_{n-2}, B_{n-1}, B_n$ (line m + 2)

For a triple output CCD/CIS that outputs 3 lines of data (each x pixels apart in the vertical direction) with colors alternating at the line rate, the output would be:

$R_1, G_1, B_1, R_2, G_2, B_2, \ldots, R_{n-1}, G_{n-1}, B_{n-1}, R_n, G_n, B_n$

with the Red data representing line m, the Green data representing line m-x, and the Blue data representing line m-2x.

The length of a line of image data sent to the PC depends on several factors:

- The number of physical pixels in the sensor, equal to (1 + Valid Pixel End - Valid Pixel Start), which we will call Valid Pixels,
- The horizontal resolution set in the configuration register,
- The pixel depth (1, 2, 4, or 8 bits), and

When scanning with the horizontal resolution equal to the optical resolution (300dpi or 600dpi) at an 8 bit pixel depth, the number of bytes in a line is equal to the number of Valid Pixels (or three times the number of Valid Pixels, if R, G, and B are interleaved).

If the horizontal resolution is set to a number below the optical resolution, the number of bytes in a line is equal to:

$$\text{Bytes/Line} = \text{Valid Pixels}\frac{\text{Horizontal Resolution}}{\text{Optical Resolution}}$$

If the pixel depth is reduced from 8 to 4, 2, or 1 bits, the bytes per line will also decrease:

$$\text{Bytes/Line} = \text{Valid Pixels}\frac{\text{Bits/Pixel}}{8}\frac{\text{Horizontal Resolution}}{\text{Optical Resolution}}$$

since multiple pixels are being packed into one byte. For a 4 bit pixel, there are 2 pixels/byte, for a 2 bit pixel, there are 4 pixels/byte, and for a 1 bit pixel, there are 8 pixels/byte.

The scanner software on the host must strip the status byte from the end of each line before reconstructing the image.

8.2.1 Reconstructing 12 bit Image Data Received By the PC

The 12 bit Data Mode is a special one for the LM9830. In the 12 bit Data Mode the horizontal resolution is always equal to the optical resolution, the gamma correction is bypassed, and the Pixel Packing stage is bypassed.

Each pixel is stored in the SRAM and transmitted to the PC in two bytes, a high byte containing the 4 bit MSB of the pixel (format 0 0 0 0 B11 B10 B9 B8), and a low byte containing the 8 bit LSB.

This mode is used to acquire 12 bit data for accurate gain and offset calibration, and for applications requiring maximum resolution data without gamma correction.

8.3 High Speed Forward

When register 07 is set to a 1, the LM9830 moves the motor forward at maximum speed (determined by the fast feed stepsize, registers 48 and 49) until either one of the Paper Sensor inputs becomes True (if that sensor has been properly programmed to interrupt scanner movement). Paper Sensor #2 can be used to cause a delayed stop. If the **FullSteps to Scan after Paper Sensor #2 trips** register is greater than 0, motor movement will continue for the programmed number of full steps. This can be used to eject paper in sheetfed scanners.

8.4 High Speed Reverse

When register 07 is set to a 2, the LM9830 moves the motor backwards at maximum speed (determined by the fast feed stepsize, registers 48 and 49) until either one of the Paper Sensor inputs becomes True (if that sensor has been properly programmed to interrupt scanner movement). The **FullSteps to Scan after Paper Sensor #2 trips** register is not used in the High Speed Reverse mode. This function is generally used to home the sensor in flatbed scanning applications.

8.5 Short Example of a Scan

- PC sends Daisy Chain Protocol Sequence to take the LM9830 out of Transparent mode.
- The LM9830 responds and shuts off printer
- PC writes to Configuration Register establishing EPP or Nibble Mode for sending data from the LM9830 to PC
- PC configures the LM9830 by writing to the configuration registers
- If no calibration data for the scanner is found in the PC, or if the user has requested a new calibration, the PC has the LM9830 scan a calibration image, then calculates the calibration coefficients for the scanner.
- PC transmits the calibration information to the LM9830 (this step can be skipped if power to the LM9830 has been maintained since the last time the calibration data was sent).
- If a sheetfed, the PC now polls the LM9830 status registers to see if there is any paper inserted. If a flatbed, it moves the scan head to the home position.
- The PC sets the Scanning bit in the Configuration Register.
- The PC sends a series of reads to the LM9830 (Figures 60-62) and gets a byte of pixel data for each read. The PC should be keeping track of exactly how many bytes there will be in an image and simply receive data until then, but the capability exists for it to read from any Configuration Register at this time, including the status bits for the 4 multipurpose inputs (paper sensors, user buttons, etc.) and the number of image data bytes available in the buffer. The PC can also write to any register, including the register containing the Scanning bit. If this bit is cleared, the scan is aborted.
- PC reads data until scan is complete or aborted.
- PC writes to Configuration Register and clears Scanning bit.
- If this is a flatbed scanner, the PC should now send a “return to start of page” command. For a sheetfeeder, it can send a “fast forward to end of page” command if needed.
- Turn off the lights, complete any other shutdown activities.
- PC sends command to put the LM9830 back in Transparent mode.

9.0 Master Clock Source

The timing for the entire chip comes from the CRYSTAL OUT pin. This clock is immediately divided down by the MCLK divider (register 08), and the divided output is MCLK (Master CLOCK). The MCLK divider range is from 1.0 to 32.5 in steps of 0.5. A configuration register code of 0 divides the clock by 1.0, while a code of 63 divides the clock by 32.5. With a 48MHz crystal, this provides an MCLCK range of 1.48MHz to 48MHz and a corresponding ADC conversion rate of 184kHz to 6.00MHz. This divider can be used to closely match the output data rate to the PC’s input data rate, minimizing scan time.

MCLK is used to clock the vast majority of the LM9830’s circuits. CRYSTAL OUT is used in a few subsections where the highest possible clock speed is required (such as the PWM pulse generator for the light source and the stepper motors).

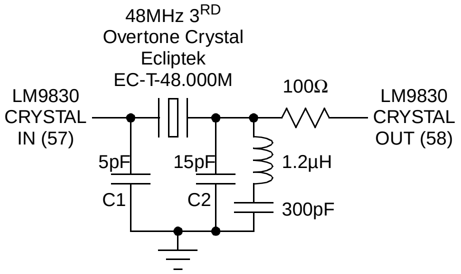


Figure 63: Crystal Oscillator Circuit

To use the LM9830's crystal oscillator feature, tie CLK_SEL (pin 71) to $DGND_{I/O}$. Figure 63 shows the recommended loading circuit and values for the 48MHz oscillator. The total capacitance on the CRYSTAL IN node (including PCB capacitance and C1) should be less than or equal to 10pF.

To drive the LM9830 with an external clock, tie CLK_SEL (pin 71) to $V_{D\ I/O}$, tie CRYSTAL_IN to $DGND_{I/O}$, and drive the TTL or CMOS-level clock signal into CRYSTAL_OUT (pin 58).

10.0 Power-On/Reset

When the LM9830 is powered up, a power-on reset signal will force the RESET and the STANDBY bits high. These bits can also be controlled through the configuration register.

When the RESET bit is high, the following applies:

The LM9830 enters Transparent mode if using parallel port interface (CMODE = 0).

All state machines are reset. Reset does not affect the values in the configuration registers (except for those indicated with black boxes in the Configuration Register table), or the contents of the gamma RAM or external SRAM.

The STANDBY bit is set by the power on reset signal or by writing to bit 2 of configuration register 07.

11.0 Standby Mode Conditions

The STANDBY bit is set on power-on.

When the STANDBY bit is high, the following applies:

External I/O (whether in Parallel Port or Microprocessor mode) continues to function (in order to enter and exit Standby Mode).

All stepper motor outputs are tri-stated.

The 50MHz oscillator continues to run, but MCLK is turned off inside the LM9830.

Analog blocks are turned off to minimize power consumption.

12.0 Misc. Questions and Answers

Q Where is calibration done?
A Calibration is done on the host computer.

Q Does the LM9830 support 400dpi sensors?
A Yes. Use the 600dpi mode, and understand that the available horizontal resolutions will be 400, 267, 200, 133, 100, 67, 50, and 33.

13.0 General Notes and Troubleshooting Tips

If the LM9830 is reset during a scan (Command register > 0), the gamma table data may be corrupted. Always stop scanning (by setting Command register to 0) and wait 10 ms before resetting the LM9830.

Some of the CCD signals (RS, CP1, and CP2) can have a small pulse when line_end occurs. Line_end resets these signals and depending on how they are programmed to go on and off, line_end can chop off the signal before its programmed off time.

If printer power is off, the printer may short the parallel databus to ground, causing scanner data to be forced to all zeros.

In full duplex modes, the host must read exactly (full - empty) kbytes from buffer - too few and the LM9830 won't resume scanning, too many and the LM9830 will output garbage. The full duplex is mode is not recommended.

The PAUSE bit in the status byte transmitted at the end of a line represents whether or not a PAUSE REQUEST is currently pending. This status byte is assembled at the "Line End" point in time for the line of pixel data just stored in RAM. This signal changes back to 0 when a RESUME REQUEST is made by the Brain. (The signal is actually a PAUSE/RESUME REQUEST.)

The PAUSE bit in the status byte at address 02 in the configuration register represents whether or not a PAUSE has actually occurred.

Registers 4 and 5 only autowrap to 0 from their highest possible legal address. If an address higher than the highest address is written, it will continue to increment (not wrap to 0), and unknown operation may occur. This can not happen unless the host writes an illegal address to the dataport.

The absolute distance between reference sample and signal sample must be 2 MCLKs or greater.

The range of values for the Optical Black (registers 0F and 10), Reset Pulse (11 and 12), CP1 pulse (13 and 14), CP2 pulse (15 and 16), Reference Sample (17), and Signal Sample (18) settings depend on the rate of the pixel data coming from the sensor.

Mode	Pixel Rate	Registers 0F to 18 Range
Pixel Rate Modes	**MCLK/24**	**0 - 23**
Line Rate Modes	**MCLK/8**	**0 - 7**

Register 1 may change state while being read. Always read it twice in succession to make sure you don't get erroneous data.

Always make sure line length (data pixels end - data pixels start) is >= the horizontal divider. For example, if you are dividing by 12, the line length must be >=12.

The Line End (registers 20 and 21) setting must be programmed as follows relative to the Data Pixels End (registers 24 and 25) setting:

Line End must be >= Data Pixels End + 20

The Data Pixels Start (registers 22 and 23) setting must be >=the Active Pixels Start (registers 1E and 1F) setting.

The MCLK frequency is 25MHz maximum for 12 bit full duplex mode or 8 bit/8 slot mode.

Data reads in 12 bit half duplex mode can not be done while scanning.

The correct Default Phase Difference (registers 52 and 53) must be set for a scan to restart properly following a pause in the scanning. See the LM9830 software for information on setting the DPD register.

Attempting to read out the last pixels transferred into the SRAM may cause the parallel port line buffer to underrun. Always make sure there is at least 1K in buffer (register 01 >= 2) before reading image data.

The number of fullsteps skipped at the start of a scan may be one less than the Fullsteps to Skip at Start of Scan (registers 4A and 4B) setting.

The Scanning Step Size (registers 46 and 47) and Fast Feed Step Size (registers 48 and 49) settings must be > 2.

When reverse is enabled, the LM9830 always stops on Red (line rate color). When reverse is disabled, it will stop on any color.

The value in CR01 is reset by “start of scan reset” sos_reset. sos_reset is asserted near the first line-end after a scan command is written (CR07=03). So if there is a residual value in CR01, it will remain there for up to one line after a scan command is written. CR07=08 (between scans) will reset CR01.

Some counters (register 01, notably), are not reset by the start of a new scan until the first line has been scanned. For this reason the chip should be briefly reset (register 07 = 08h) prior to a scan.

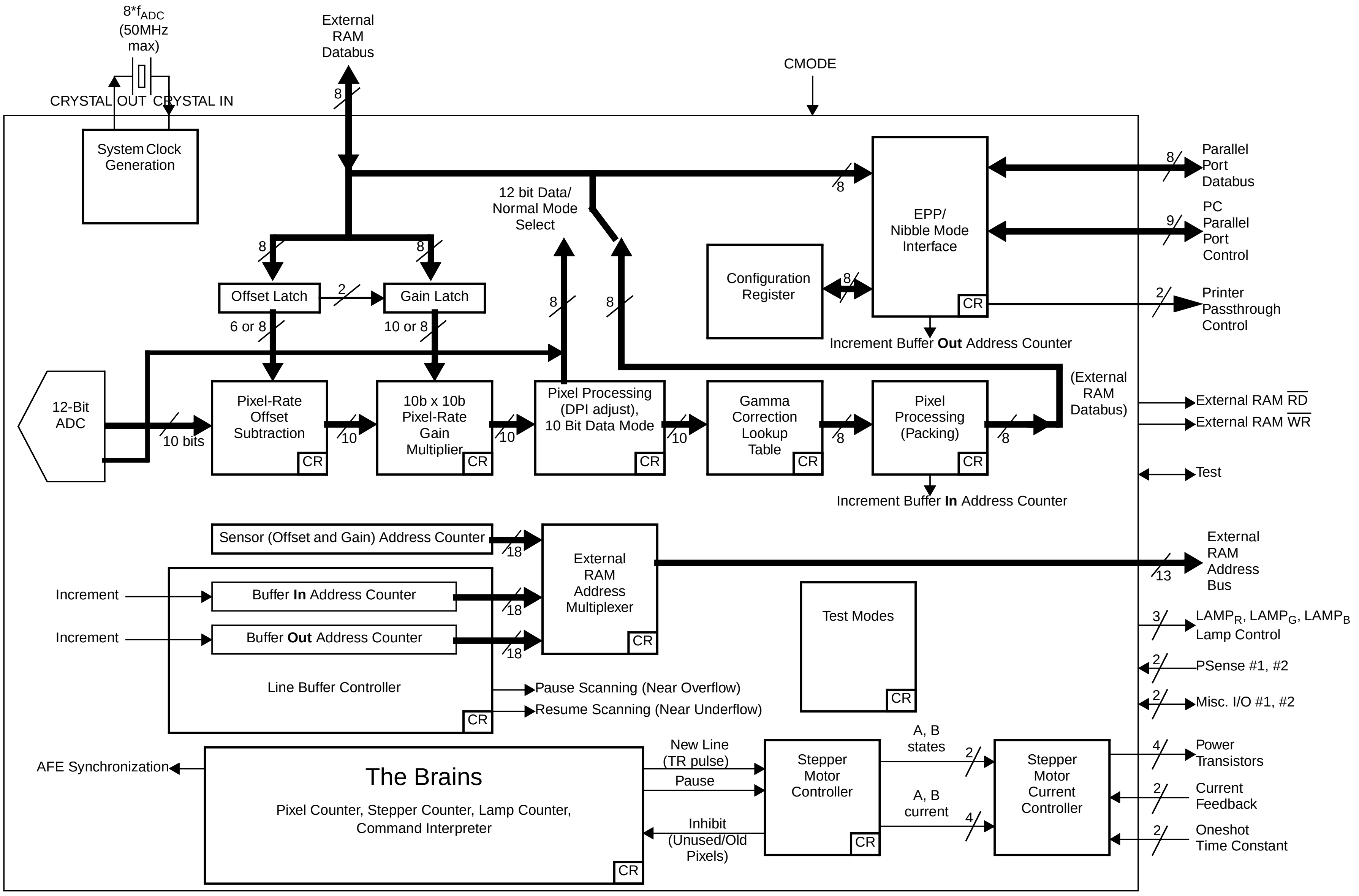
Make sure register 42 is set to the proper value (4 bit nibble or 8 bit bidirectional) for your PC’s parallel port mode before attempting to read data from the LM9830.

BUSY may go high by itself for the first few pixels after a scan is started. After starting a scan, wait several ms before talking to the LM9830.

When in 1 channel Mode A, the Dataport Target Color (reg03b1-2) value is ignored for gamma reads and writes. The 1 Channel Mode A Channel Color register (reg26b3-4) selects the gamma table to be used when in 1 Channel Mode A. This only applies to the gamma table. Register 3 is used to select the color for gain/offset coefficient data.

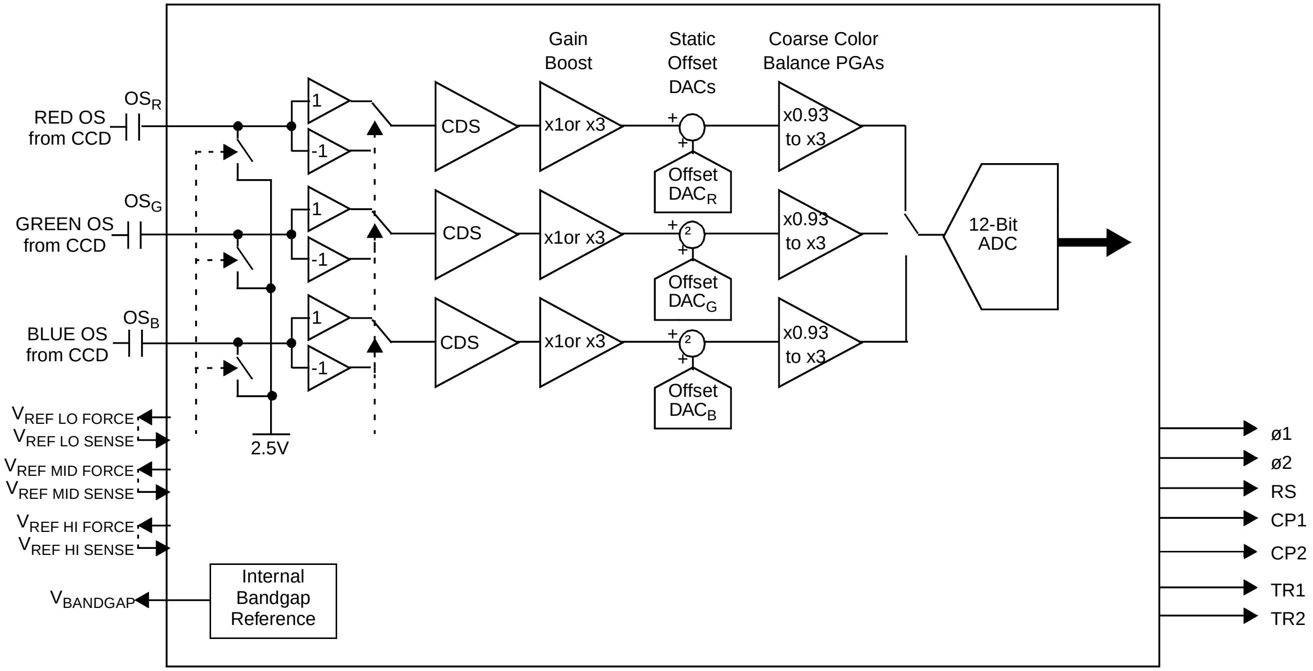
Gamma and gain/offset coefficient data should be written with register 7 = 0 (idle). Do not attempt to write gamma or gain/offset coefficient data when scanning (register 7 = 3).

Digital Processing Block Diagram

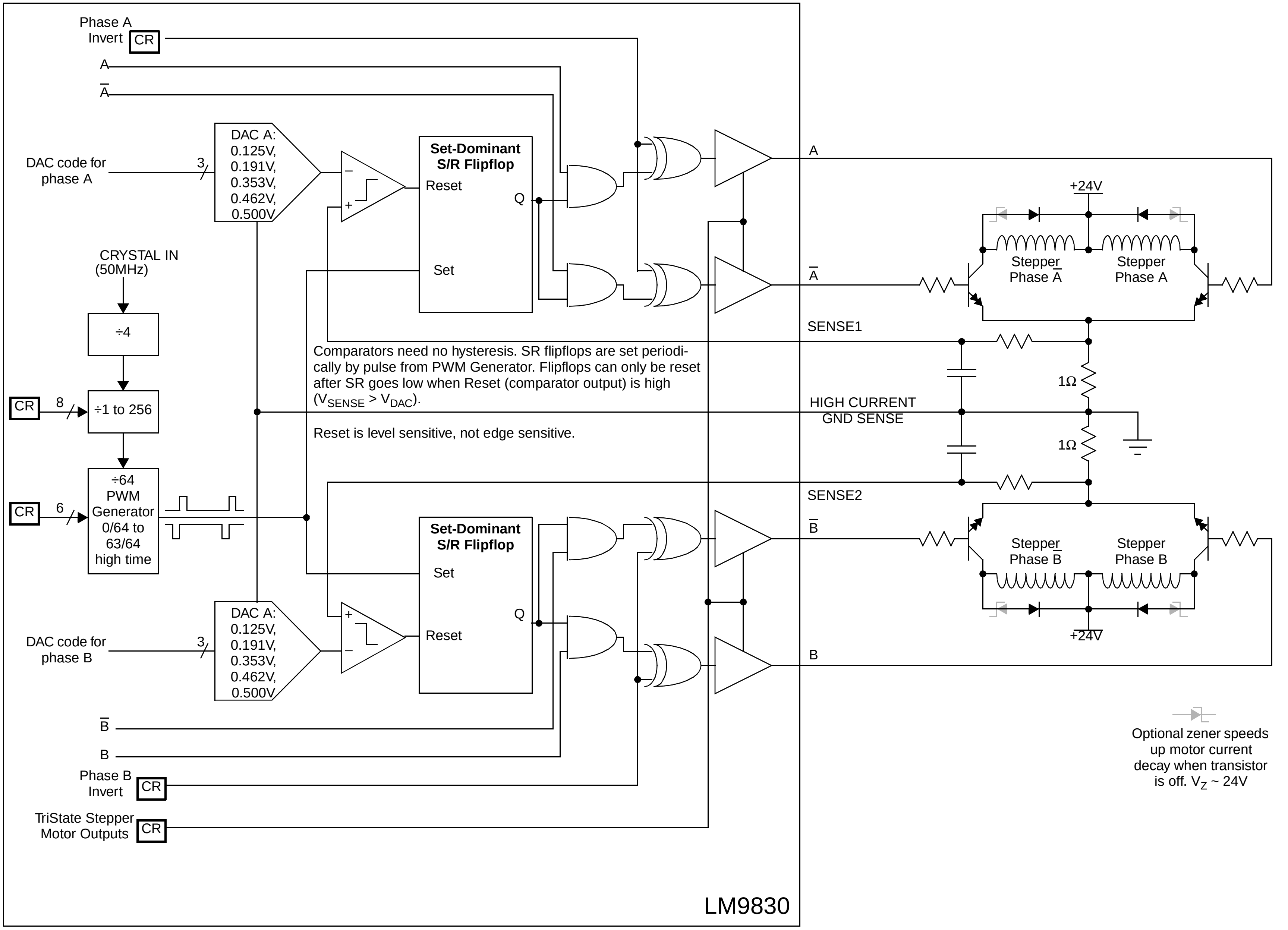

8*f_ADC (50MHz max)
CRYSTAL OUT
CRYSTAL IN
External RAM Databus
8
CMODE
System Clock Generation
12 bit Data/ Normal Mode Select
8
EPP/ Nibble Mode Interface
8
Parallel Port Databus
9
PC Parallel Port Control
Configuration Register
8
CR
2
Printer Passthrough Control
Increment Buffer **Out** Address Counter
8
8
Offset Latch
2
Gain Latch
8
8
6 or 8
10 or 8
12-Bit ADC
10 bits
Pixel-Rate Offset Subtraction
CR
10
10b x 10b Pixel-Rate Gain Multiplier
CR
10
Pixel Processing (DPI adjust), 10 Bit Data Mode
CR
10
Gamma Correction Lookup Table
CR
8
Pixel Processing (Packing)
CR
8
(External RAM Databus)
External RAM RD
External RAM WR
Test
Increment Buffer **In** Address Counter
Sensor (Offset and Gain) Address Counter
18
External RAM Address Multiplexer
CR
13
External RAM Address Bus
Increment
Buffer **In** Address Counter
18
Increment
Buffer **Out** Address Counter
18
Line Buffer Controller
CR
Pause Scanning (Near Overflow)
Resume Scanning (Near Underflow)
Test Modes
CR
3
LAMP_R, LAMP_G, LAMP_B Lamp Control
2
PSense #1, #2
2
Misc. I/O #1, #2
AFE Synchronization
The Brains
Pixel Counter, Stepper Counter, Lamp Counter, Command Interpreter
CR
New Line (TR pulse)
Pause
Inhibit (Unused/Old Pixels)
Stepper Motor Controller
CR
A, B states
2
A, B current
4
Stepper Motor Current Controller
4
Power Transistors
2
Current Feedback
2
Oneshot Time Constant

CR = Configured by bits in the Configuration Register

Analog Front End Block Diagram

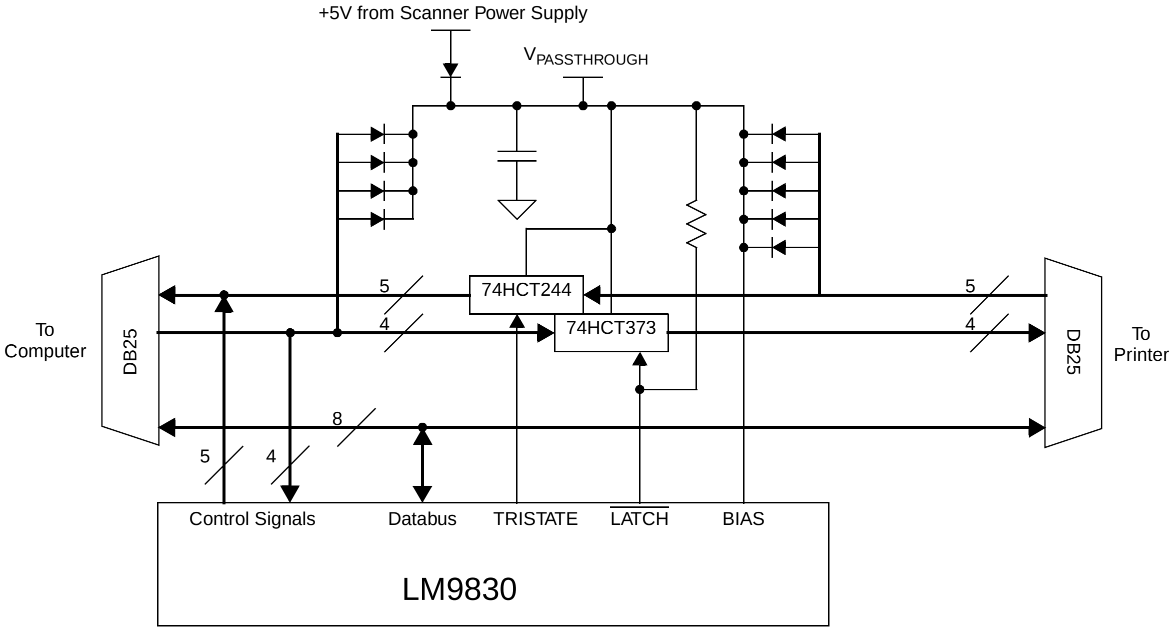

Gain Boost
Static Offset DACs
Coarse Color Balance PGAs
RED OS from CCD
OS_R
GREEN OS from CCD
OS_G
BLUE OS from CCD
OS_B
1
-1
CDS
x1or x3
+
Offset DAC_R
Offset DAC_G
Offset DAC_B
x0.93 to x3
12-Bit ADC
2.5V
$V_{REF\ LO\ FORCE}$
$V_{REF\ LO\ SENSE}$
$V_{REF\ MID\ FORCE}$
$V_{REF\ MID\ SENSE}$
$V_{REF\ HI\ FORCE}$
$V_{REF\ HI\ SENSE}$
$V_{BANDGAP}$
Internal Bandgap Reference
ø1
ø2
RS
CP1
CP2
TR1
TR2

Stepper Motor Current Controller Block Diagram


Phase A Invert
CR
A
$\overline{A}$
DAC code for phase A
3
DAC A: 0.125V, 0.191V, 0.353V, 0.462V, 0.500V
–
+
Set-Dominant S/R Flipflop
Reset
Q
Set
CRYSTAL IN (50MHz)
÷4
CR
8
÷1 to 256
CR
6
÷64 PWM Generator 0/64 to 63/64 high time
Comparators need no hysteresis. SR flipflops are set periodically by pulse from PWM Generator. Flipflops can only be reset after SR goes low when Reset (comparator output) is high ($V_{SENSE} > V_{DAC}$).
Reset is level sensitive, not edge sensitive.
Set-Dominant S/R Flipflop
Set
Q
Reset
+
–
DAC A: 0.125V, 0.191V, 0.353V, 0.462V, 0.500V
DAC code for phase B
3
$\overline{B}$
B
Phase B Invert
CR
TriState Stepper Motor Outputs
CR
LM9830
A
$\overline{A}$
SENSE1
HIGH CURRENT GND SENSE
SENSE2
$\overline{B}$
B
+24V
Stepper Phase $\overline{A}$
Stepper Phase A
1Ω
1Ω
Stepper Phase $\overline{B}$
Stepper Phase B
+24V

Optional zener speeds up motor current decay when transistor is off. V_Z ~ 24V

Printer Passthrough Block Diagram



Notes:

$V_{PASSTHROUGH}$ is generated by rectifying the control outputs from the PC and printer parallel ports. If needed, the 8 bit data lines may be rectified as well to provide additional current.

If the LM9830's TRISTATE output is not forced to ground when the LM9830 power is off, then it needs a pulldown resistor to ground.

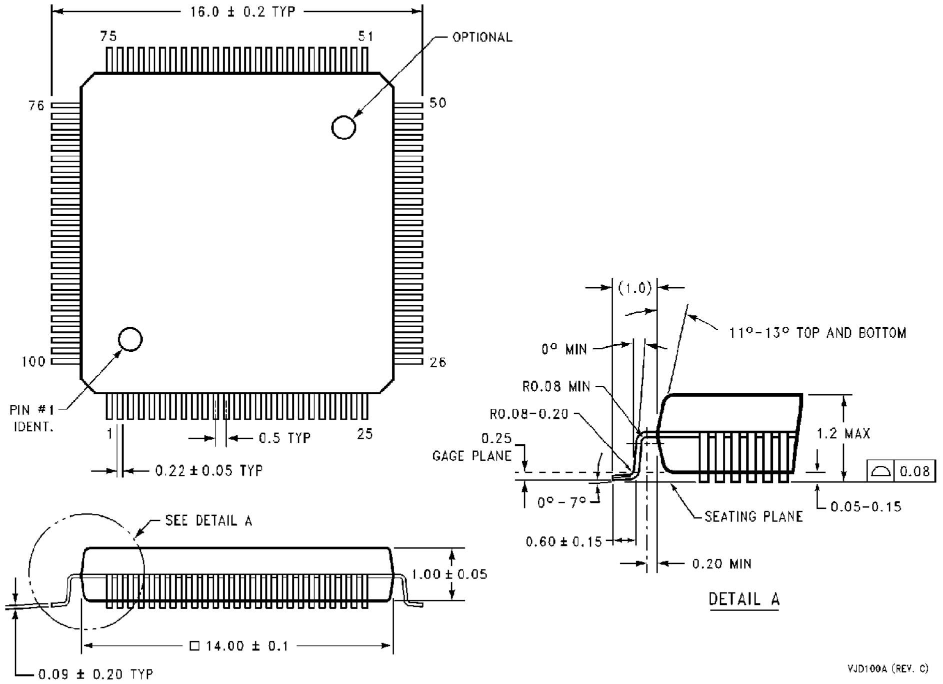
The 74HCT373 needs to pass 4 lines from the PC to the printer, the 74HCT244 controls 5 lines from the printer to the PC. The latch is needed to hold the 4 inputs to the printer in the state they were in before the LM9830 left the transparent mode. It is possible that a simple tristate buffer (74HCT244) could be used instead of the latch, with pullups/pulldowns defining the signals sent to the printer when the LM9830 is active. It is also possible that one signal (probably $\overline{\text{INIT}}$) could always be simultaneously connected to the printer port and the LM9830, allowing just one 74HCT244 to implement the printer passthrough function.

The final recommended schematic for this mode is an applications issue and will be determined after testing with final silicon.

The design requirements are:

	Scanner Active	PassThrough	LM9830 Power Off
TRISTATE	+5V	0V	0V (through pulldown, if necessary)
$\overline{\text{LATCH}}$	0V	5V	5V (through pullup) (latches previous states)
D0-D7	LM9830 sends/receives	Tristate	Tristate
$\overline{\text{STROBE}}$, $\overline{\text{AUTOFEED}}$, $\overline{\text{SELECT IN}}$, $\overline{\text{INIT}}$	Inputs to LM9830	Tristate	Tristate
$\overline{\text{ACK}}$, BUSY, PE, SELECT, $\overline{\text{ERROR}}$	LM9830 Outputs	Tristate	Tristate

Physical Dimensions (millimeters)


16.0 ± 0.2 TYP
75
51
OPTIONAL
76
50
100
26
PIN #1 IDENT.
1
0.5 TYP
25
0.22 ± 0.05 TYP
SEE DETAIL A
1.00 ± 0.05
□ 14.00 ± 0.1
0.09 ± 0.20 TYP
(1.0)
11°-13° TOP AND BOTTOM
0° MIN
R0.08 MIN
R0.08-0.20
0.25
GAGE PLANE
1.2 MAX
0.08
0° - 7°
SEATING PLANE
0.05-0.15
0.60 ± 0.15
0.20 MIN
DETAIL A
VJD100A (REV. C)

100-Pin Thin Plastic Quad FlatPac (JEDEC) (TQFP)
NS Package Number VJD100A
Order Number LM9830VJD

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National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: a49 (0) 180-530 85 86
Email: europe.support @ nsc.com
Deutsch Tel: + 49 (0) 180-530 85 85
English Tel: + 49 (0) 180-532 78 32
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Italiano Tel: + 49 (0) 180-534 16 80

National Semiconductor Hong Kong
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
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