LCD Segment Driver series

For 72/80/96 Segment type LCD
LCD Segment Driver
BU9735K, BU9796FS, BU9716BKV, BU9718KV

● Outline

This is LCD segment driver for 72-96 segment type display. There is a lineup which is suitable for multi function display and is integrated display RAM and power supply circuit for LCD driving with 4 common output type: BU9735K and BU9796FS. And 3 common output type: BU9716BKV and BU9718KV.

BU9735K 72Segment (18SEG×4COM) Driver

● Feature

1) 4wire serial interface (SCK, SD, $\overline{C/D}$, $\overline{CS}$)
2) Integrated RAM for display data (DDRAM) : 18 × 4bit (Max 72 Segment)
3) LCD driving port: 4 Common output, 18 Segment output
4) Display duty: 1/4 duty
5) Integrated Oscillator circuit (external resister type)
6) Integrated Power supply circuit for LCD driving (1/3 bias)
7) Low power/ Ultra low power consumption design: +2.5～5.5V

● Uses

DVC, Car audio, Telephone

● Absolute Maximum Ratings (Ta=25degree, VSS=0V) (BU9735K)

Parameter	Symbol	Limits	Unit	Remarks
Power Supply Voltage1	VDD	-0.3 ～ +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.3 ～ +7.0	V	LCD drive voltage
Allowable loss	Pd	400	mW	When use more than Ta=25°C, subtract 4mW per degree.
Operational temperature range	Topr	-40 ～ +85	Degree	
Storage temperature range	Tstg	-55 ～ +125	Degree	
Input voltage range	VIN	-0.3 to VDD*0.3	V	
Output voltage range	VOUT	-0.3 to VDD+0.3	V	

*This product is not designed against radioactive ray.

● Recommend operating conditions (Ta=25degree, VSS=0V) (BU9735K)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage1	VDD	2.2	-	5.5	V	
Power Supply Voltage2	VLCD	2.5	-	5.5	V	VLCD≧VC≧VSS
Oscillator frequency	fOSC	-	36	-	KHz	Rf=470kΩ

∗This document is not delivery specifications.

Jun. 2008

• Electrical Characteristics (BU9735K)

DC Characteristics (VDD=2.5～5.5V, VSS=0V, Ta=25degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition	Terminal
		Min.	Typ.	Max.			
"H" level input voltage	VIH1	0.8×VDD	-	VDD	V		SC1, SD, SCK, C/D, CS
"L" level input voltage	VIL1	0	-	0.2×VDD			
LCD Driver on resistance	RON	-	-	30	KΩ	|ΔVON|=0.1V	SEG1～18, COM1～4
"H" level input current	IIH	-2	-	-	uA	VIN=VDD	OSC1, SD, SCK, C/D, CS,
"L" level input current	IIL	-	-	2	uA	VIN=0	
Input capacitance	CI	-	5	-	pF		SD, SCK, C/D, CS
Power consumption	IDD	-	0.05	1	uA	*2 Display OFF	VDD
		-	30	70	uA	*2 Display ON	
		-	80	200	uA	*3 MPU Access	

*1: LCD Driver on resistance is not included internal power supply impedance.

*2: VLCD=VDD, Rf=470Kohm, except of OSC1 terminals are connected to VDD or VSS.

*3: VLCD=VDD, Rf=470Kohm, fSCK=200KHz

AC Characteristics (VDD=2.5～5.5V, VSS=0V, Ta=25degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
SCK rise time	tTLH	-	-	100	ns	
SCK fall time	tTHL	-	-	100	ns	
SCK cycle time	tCYC	800	-	-	ns	
Wait time for command	tWAIT	800	-	-	ns	
SCK pulse width H"	tWH1	300	-	-	ns	
SCK pulse width "L"	tWL1	300	-	-	ns	
SD setup time	tSU1	100	-	-	ns	
SD hole time	tH1	100	-	-	ns	
CS pulse width "H"	tWH2	300	-	-	ns	
CS pulse width "L"	tWL2	6400	-	-	ns	
CS setup time	tSU2	100	-	-	ns	
CS hold time	tH2	100	-	-	ns	
C/D setup time	tSU3	100	-	-	ns	
C/D hold time	tH3	100	-	-	ns	Based on SCK 8th clock rising
C/D - CS time*4	tCCH	100	-	-	ns	Based on CS rising
C/D - SCK time*4	tSCH	100	-	-	ns	Based o SCK 8th clock falling
Display start delay time	tON	140	-	-	ns	SCK 8th clock rising to display start

*4: should satisfy either one condition

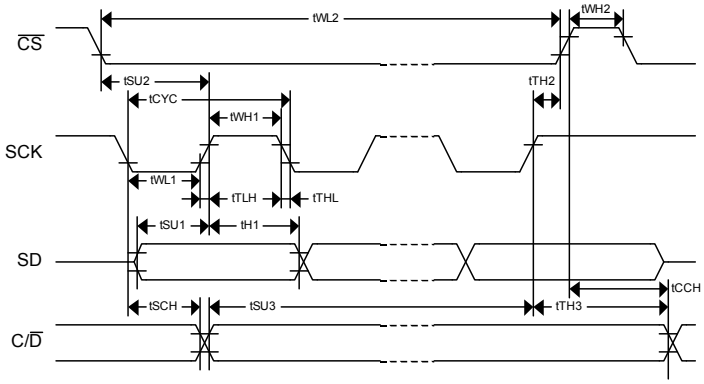


Fig. BU9735K-1 Interface timing

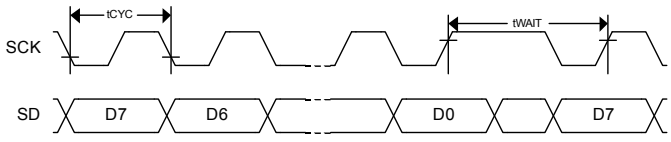


Fig. BU9735K-2 Command cycle

● Block Diagram （BU9735K）

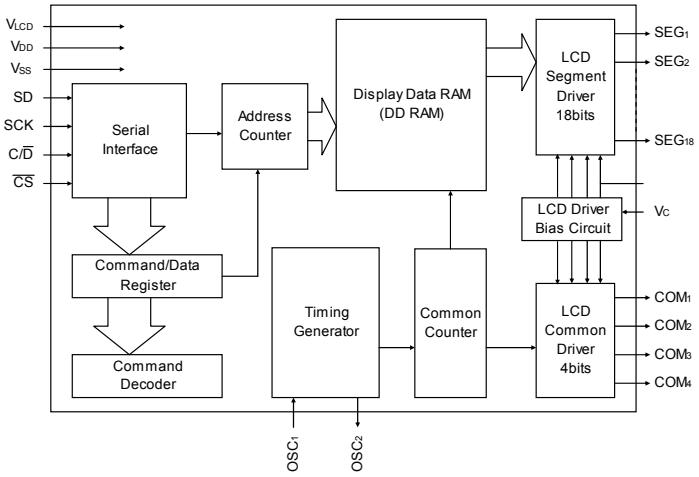


Fig. BU9735K-3 Block diagram

●Pin Arrangement （BU9735K）

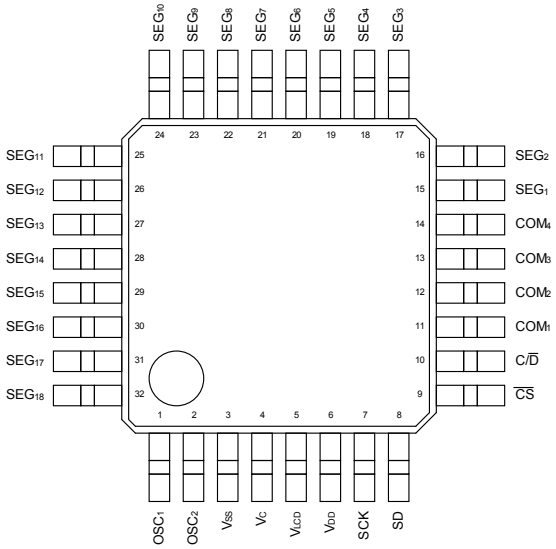


Fig. BU9735KV-4 Pin arrangement

● Terminal description （BU9735K）

Terminal	No.	Type	Function
OSC1 OSC2	1 2	I O	Int clock use mode, connect resister between OSC1 and OSC2. Ext clock use mode, input clock from OSC1, OSC2 keep OPEN.
VSS	3		VSS terminal
VC VLCD	4 5		Power supply for LCD driving Please keep VLCD≧VC≧VSS condition
VDD	6		VDD terminal
SCK	7	I	Serial clock input
SD	8	I	Serial data input
$\overline{CS}$	9	I	Chip select input "L": active,
$\overline{C/D}$	10	I	Command data judgment input “L”: display data, “H”: command
COM1～4	11～14	O	LCD COMMON output
SEG1～18	15～32	O	LCD SEGMENT output

● Block Description (BU9735K)

○ ADDRESS COUNTER

An address counter shows the address of DDRAM. Address data are transferred to the address counter automatically when an address set is written in the command/data register.

After data are written in DDRAM, +1 or +2 is done automatically with an address counter. The choice of +1 or +2 is done automatically by the next condition.

DDRAM 8bit writing (in the 8 clock of $S\overline{C}K$, C/D= "L") → +2

DDRAM 4bit rewriting (in the 8 clock of $S\overline{C}K$, C/D= "H") → +1

And, when it is counted to 11H, an address becomes 00H with an address counter by the next count up.

○ DISPLAY DATA RAM (DDRAM)

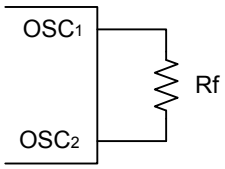
A display data RAM (DDRAM) is used to store display data. That capacity is 18 address × 4 bits. DDRAM and the relations of the display position are as the following.

DDRAM Address

				00	01	02	03	04	05	06	07	・・・・・	0F	10	11	
BIT	D0	D4	D0													COM1
	D1	D5	D1													COM2
	D2	D6	D2													COM3
	D3	D7	D3													COM4
	8bit writing		4bit re-writing	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8	・・・・・	SEG16	SEG17	SEG18	

○ TIMING GENERATER

A built-in oscillator circuit does oscillated by connecting Rf between OSC1, OSC2, and an indication timing signal is caused. And, it is possible that it is made to work by the external clock input, too.



(It is possible that Oscillating Frequency is changed with Rf.)

Fig. BU9735K-5 Rf Oscillator Circuit

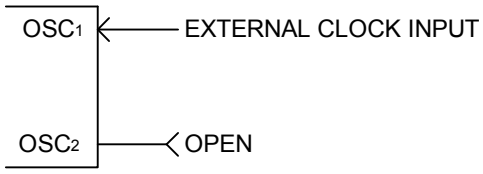


Fig. BU9735K-6 External Clock Input

○ LCD DRIVE POWER SUPPLY

LCD drive power supply occurs by BU9735K.

LCD voltage is given by VC, and it causes V1=(2/3) VC, V2=(1/3) VC.

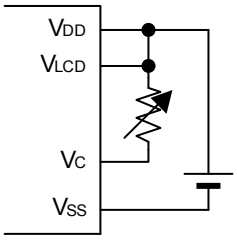


Fig. BU9735K-7 Internal Power Supply use

● DETAILS OF COMMANDS (BU9735K)

There is the following thing in the command (The 8×n clock of $\overline{SCK}$ is C/D= "H".) of BU9735K.

◯ ADDRESS SET

MSB							LSB
0	0	0	A	A	A	A	A

Address data shown as AAAAA by the binary system is set on the address counter.
Address does +2 every time indication data input (for 8bit) completes input.

◯ DISPLAY ON

MSB							LSB
0	0	1	*	*	*	*	*

* : Don't Care

There are no relations with the contents of the display data RAM (DDRAM).
And all display is turned on. In this case, the contents of DDRAM don't change.

◯ DISPLAY OFF

MSB							LSB
0	1	0	*	*	*	*	*

* : Don't Care

There are no relations with the contents of the display data RAM (DDRAM).
And all display is turned off. A built-in power supply circuit is turned off.
And an oscillation circuit stops. In this case, the contents of DDRAM don't change.

◯ DISPLAY START

MSB							LSB
0	1	1	*	*	*	*	*

* : Don't Care

Display is started in accordance with the contents of DDRAM.

◯ REWRITING OF THE DISPLAY DATA RAM (DDRAM)

MSB							LSB
1	0	0	*	D	D	D	D

* : Don't Care

The binary four bits data DDDD are written in DDRAM.
A writing address is address ordered by the address set command.
Then, after this command is carried out, an address does + 1 automatically.

◯ RESET

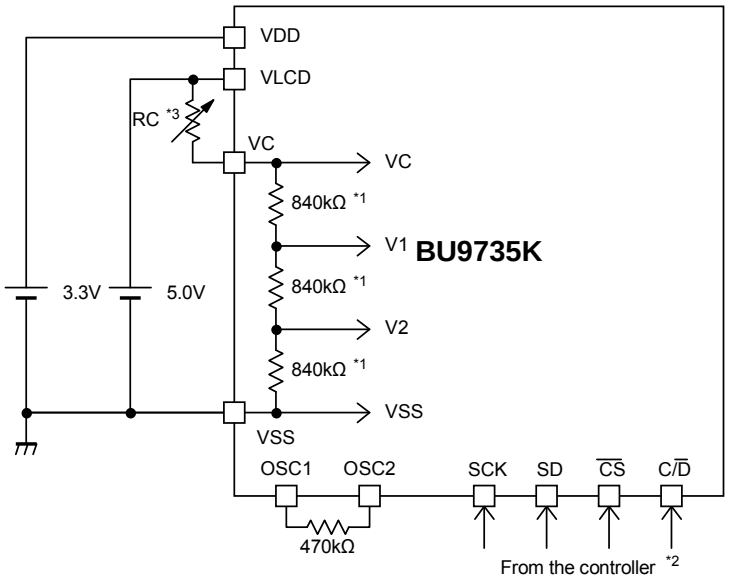
MSB							LSB
1	1	0	*	*	*	*	*

* : Don't Care

This command is to take precedence over all commands after POWER-on, and carry it out. BU9735K is initialized in the following condition by this command.

- Display off
- Address counter resetting
- Oscillation stop

● Recommendation circuit example (BU9735K)



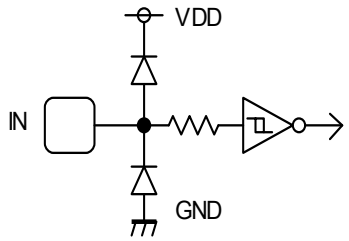
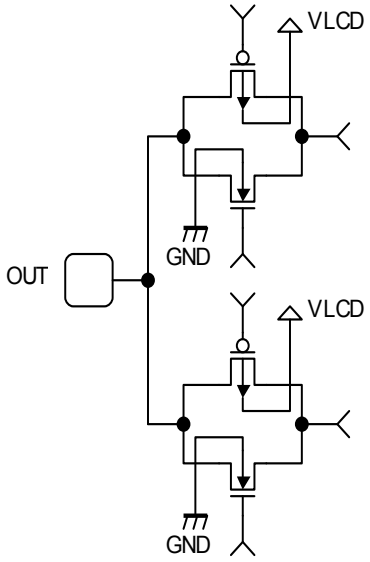
*1 The value (840kΩ) of the built-in resistance value in the figure is reference value. Value varies according to terms of manufacture and so on.

*2 The maximum value of the signal of the control isn't to use higher value than VDD. (Refer to the regulation of the input voltage in the specifications.)

*3 It can use as a resistance for the contrast adjustment when variable resistance is given to the VLCD-VC space. In this case, the resistance of the outside and resistance with built-in BU9735K become connections like a left figure. The value of RC is to decide the value, which met a system referring to the circuit of the left figure.

Fig. BU9735K-8 Power supply for control circuit and LCD driving is independent case
(Example: VLCD=5.0V and VDD=3.3V)

● INPUT OUTPUT CIRCUIT (BU9735K)

Name	I/O	Circuit	Name	I/O	Circuit
SD SCK C/D CS	I		SEG1 ～ SEG18 COM1 ～ COM4	O	

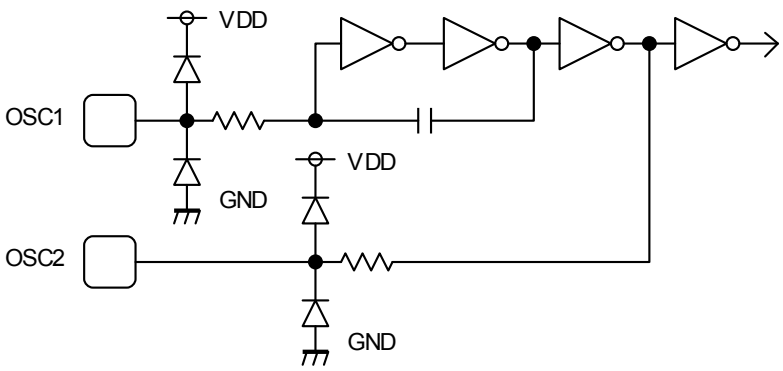
Name	I/O	Circuit
OSC1 OSC2	I O	

Fig.BU9735K-9 I/O circuit

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

● Order form name selection

B	U	9	7	3	5	K	–	E	2

ROHM form name

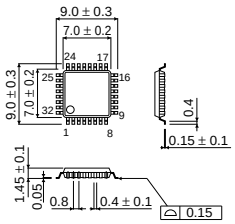
Part No.

Package type
KV=VQFP

Packaging and forming specification
E2 =Reel-shaped emboss taping

OFP32

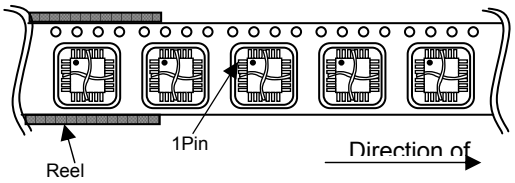
<Dimension>



(Unit:mm)

<Packing information>

Tape	Embossed carrier tape
Quantity	1500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

BU9796FS 80Segment (20SEG×4COM) Driver

● Feature (BU9796FS)

1) 2wire serial interface
2) Integrated RAM for display data (DDRAM) : 20 × 4bit (Max 80 Segment)
3) LCD driving port: 4 Common output, 20 Segment output
4) Display Duty: 1/4 duty
5) Integrated Oscillation circuit
6) Integrated Buffer AMP for LCD driving power supply circuit
7) Support 1/2bias, 1/3bias select
8) No external components
9) Low voltage / low power consumption design: 2.5～5.5V

● ● Uses (BU9796FS)

Telephone, FAX, Portable equipments（POS, ECR, PDA etc.）,
DSC, DVC, Car audio, Home electrical appliance, Meter equipment etc.

● Absolute Maximum Ratings （Ta=25degree, VSS=0V） (BU9796FS)

Parameter	Symbol	Limits	Unit	Remarks
Power Supply Voltage1	VDD	-0.5 ～ +7.0	V	Power supply
Power Supply Voltage2	VLCD	-0.5 ～ +7.0	V	LCD drive voltage
Allowable loss	Pd	0.64	W	When use more than Ta=25°C, subtract 6.4mW per degree.
Input voltage range	VIN	-0.5 ～ VDD+0.5	V	
Operational temperature range	Topr	-40 ～ +85	degree	
Storage temperature range	Tstg	-55 ～ +125	degree	

*This product is not designed against radioactive ray.

● Recommend operating conditions (Ta=25degree, VSS=0V) (BU9796FS)

Parameter	Symbol	MIN	TYP	MAX	Unit	Remarks
Power Supply Voltage1	VDD	2.5	-	5.5	V	Power supply
Power Supply Voltage2	VLCD	0	-	VDD-2.4	V	LCD drive voltage

* Please use in the range of VDD-VLCD≧ 2.4V

• Electrical Characteristics (BU9796FS)

DC Characteristics (VDD=2.5～5.5V, VLCD=0V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter		Symbol	Limit			Unit	Condition
			MIN	TYP	MAX		
“H” level input voltage		VIH	0.7VDD	-	VDD	V	
“L” level input voltage		VIL	VSS	-	0.3VDD	V	
“H” level input current		IIH	-	-	1	uA	
“L” level input current		IIL	-1	-	-	uA	
LCD Driver on resistance	SEG	RON	-	3	-	kΩ	Iload=±10uA
	COM	RON	-	3	-	kΩ	
VLCD supply voltage		VLCD	0	-	VDD-2.4	V	VDD-VLCD□2.4V
Standby current		IDD1	-	-	5	uA	Display off, Oscillation off
Power consumption		IDD2	-	12.5	30	uA	VDD=3.3V, VLCD=0V, Ta=25degree Power save mode SR = Power save mode1, Power save mode FR = Power save mode1 1/3 bias, Frame inverse
Frame frequency		fCLK	56	80	104	Hz	Power save mode FR = Normal mode

MPU interface Characteristics (VDD=2.5～5.5V, VLCD=0V, VSS=0V, Ta=-40～85degree, unless otherwise specified)

Parameter	Symbol	Limit			Unit	Condition
		MIN.	TYP.	MAX.		
Input rise time	tr	-	-	0.3	us	
Input fall time	tf	-	-	0.3	us	
SCL cycle time	tSCYC	2.5	-	-	us	
“H” SCL pulse width	tSHW	0.6	-	-	us	
“L” SCL pulse width	tSLW	1.3	-	-	us	
SDA setup time	tSDS	100	-	-	ns	
SDA hold time	tSDH	100	-	-	ns	
Buss free time	tBUF	1.3	-	-	us	
START condition hold time	tHD;STA	0.6	-	-	us	
START condition setup time	tSU;STA	0.6	-	-	us	
STOP condition setup time	tSU;STO	0.6	-	-	us	

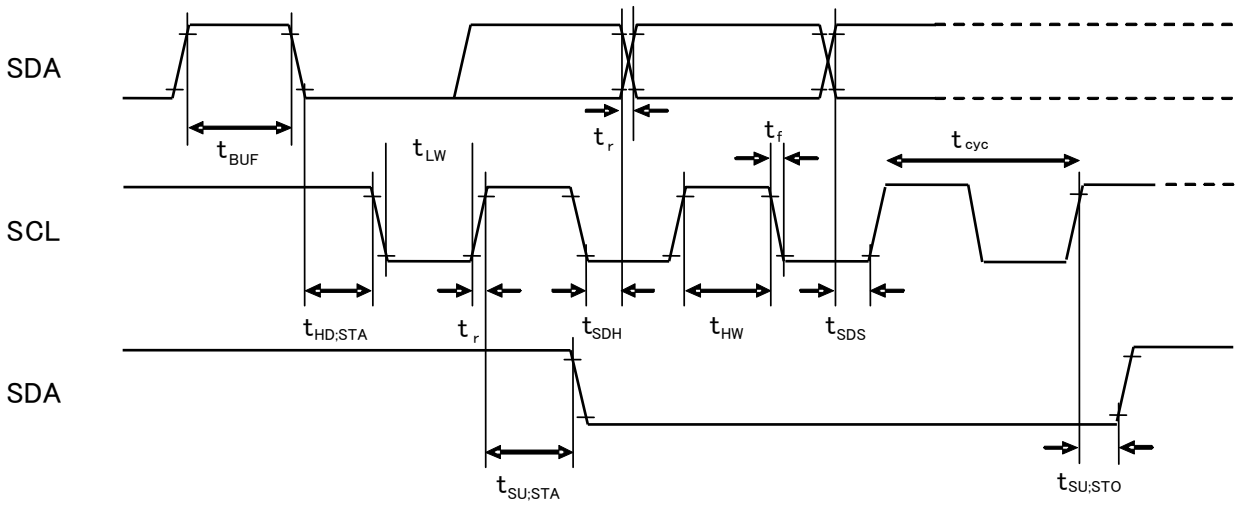


Fig. BU9796FS-1 interface timing

●Block Diagram（BU9796FS）

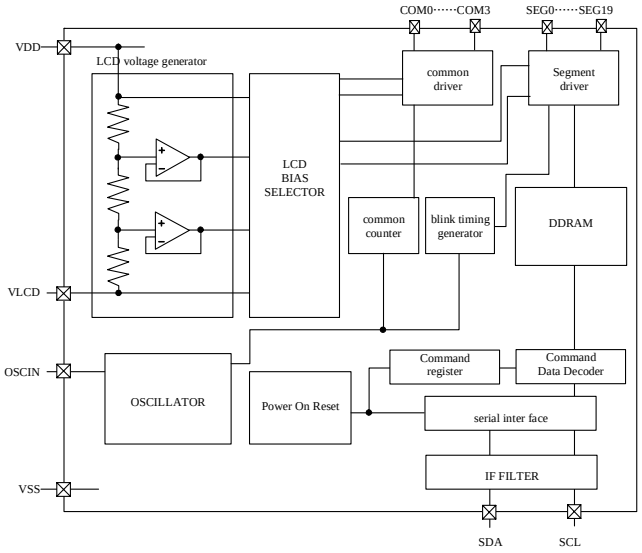


Fig. BU9796FS-2 block diagram

● Pin Arrangement （BU9796FS）

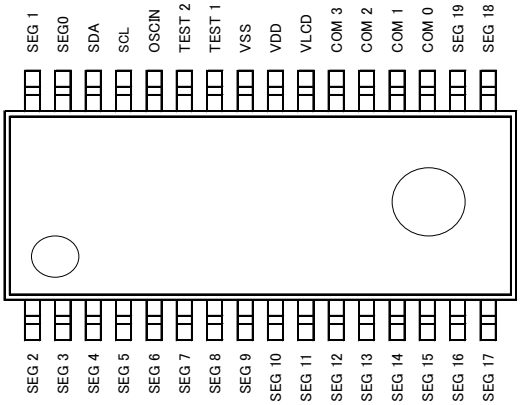


Fig. BU9796FS-3 Pin arrangement

●Terminal description （BU9796FS）

Terminal	Terminal No.	I/O	Function
TEST1	26	I	Test input (ROHM use only) Must be connect to VSS
TEST2	27	I	Test input (ROHM use only) TEST2=”L”: POR circuit enable TEST2=”H”: POR circuit disenable, refer to “Cautions in Power ON/OFF”
OSCIN	28	I	External clock input Ext clock and Int clock can be changed by command. Must be connect to VSS when use internal oscillation circuit.
SDA	30	I/O	serial data in-out terminal
SCL	29	I	serial data transfer clock
VSS	25		GND
VDD	24		Power supply
VLCD	23		Power supply for LCD driving
SEG0-19	31,32 1-18	O	SEGMENT output for LCD driving
COM0-3	19-22	O	COMMON output for LCD driving

● Command Description （BU9796FS）

D7 (MSB) is bit for command or data judgment.
Refer to Command and data transfer method.

C：0：Next byte is RAM write data.
1：Next byte is command.

○ Display control (DISCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	1	P4	P3	P2	P1	P0

Set Power save mode FR

Setup	P4	P3	Reset initialize condition
Normal mode	0	0	○
Power save mode1	0	1	
Power save mode2	1	0	
Power save mode3	1	1	

Set LCD drive waveform

Setup	P2	Reset initialize condition
Line inversion	0	○
Frame inversion	1	

Set Power save mode SR

Setup	P1	P0	Reset initialize condition
Power save mode1	0	0	
Power save mode2	0	1	
Normal mode	1	0	○
High power mode	1	1	

* Please keep condition VDD-VLCD≧3.0V in High power mode.

○ Mode Set (MODE SET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	0	*	P3	P2	*	*

(*: Don't Care)

Set display ON and OFF

Setup	P3	Reset initialize condition
Display OFF	0	○
Display ON	1	

Set bias level

Setup	P3	Reset initialize condition
1/3 Bias	0	○
1/2 Bias	1	

○ Address set (ADSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	0	0	P4	P3	P2	P1	P0

The range of address can be set as 00000 to 10011(2).

○ Set IC Operation (ICSET)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	0	1	*	P1	P0

(*: Don't Care)

Set software reset execution

Setup	P1
No operation	0
Software Reset execute	1

Set oscillator mode

setup	P0	Reset initialize condition
Internal oscillation	0	○
External clock input	1	

○ Blink control (BLKCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	0	*	P1	P0

(*: Don't Care)

Set blink mode

Blink mode (Hz)	P1	P0	Reset initialize condition
OFF	0	0	○
0.5	0	1	
1	1	0	
2	1	1	

○ All Pixel control (APCTL)

MSB LSB

D7	D6	D5	D4	D3	D2	D1	D0
C	1	1	1	1	1	P1	P0

All display set ON, OFF

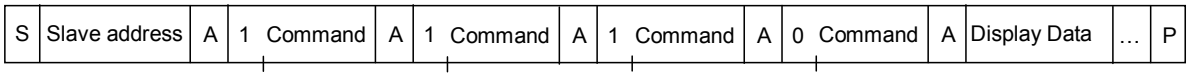
APON	P1	Reset initialize condition
Normal	0	○
All pixel ON	1	

APOFF	P0	Reset initialize condition
Normal	0	○
All pixel OFF	1	

● Function description（BU9796FS）

○ Command transfer method

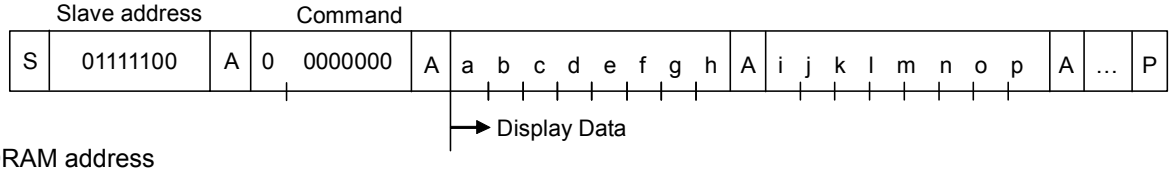
1byte after Slave Address always becomes command input.
MSB (“command or data judge bit”) of command decide to next data is command or display data.
When set “command or data judge bit”=‘1’, next byte will be command.
When set “command or data judge bit”=‘0’, next byte data is display data.



Once it becomes display data transfer condition, it cannot input command.
When want to input command again, please generate “START condition” once.

○ Write display and transfer method

This device has Display Data RAM (DDRAM) of 50×4=200bit.
The relationship between data input and display data, DDRAM data and address are as follows;



DDRAM address

BIT	00	01	02	03	04	05	06	07	・・・	2Fh	30h	31h	
0	a	e	i	m									COM0
1	b	f	j	n									COM1
2	c	g	k	o									COM2
3	d	h	l	p									COM3
	SEG0	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7		SEG47	SEG48	SEG49	

Data transfer to DDRAM happens every 4bit data. So It will be finished to transfer with no need to wait ACK.

○ Reset initialize condition

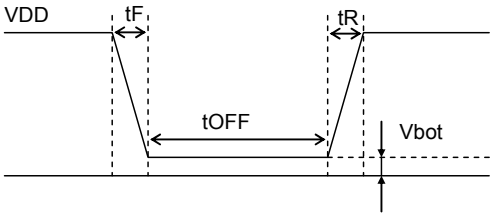
Initial condition after execute Software Reset is as follows.

- Display is OFF.
- DDRAM address is initialized (DDRAM Data is not initialized).
- Refer to Command Description about initialize value of register.

● Cautions in Power ON/OFF (BU9796FS)

This device has “P.O.R” (Power-On Reset) circuit and Software Reset function.
Please keep the following recommended Power-On conditions in order to power up properly.

Please set power up conditions to meet the recommended tR, tF, tOFF, and Vbot spec below in order to ensure P.O.R operation
* It has to set TEST2=”L” to be valid in POR circuit.



Recommendation condition of tR, tF, tOFF, Vbot (Ta=25℃)

tR	tF	tOFF	Vbot
Less than 1ms	Less than 1ms	More than 100ms	Less than 0.1V

Fig. BU9796FS-4 Power ON/OFF waveform

If it is difficult to meet above conditions, execute the following sequence after Power-On.

* It has to keep the following sequence in the case of TEST2=”H”. As POR circuit is invalid status. But it is not able to accept Command input in Power off status, it has to take care that software reset is not perfectly alternative method of POR function.

(1) Generate STOP condition

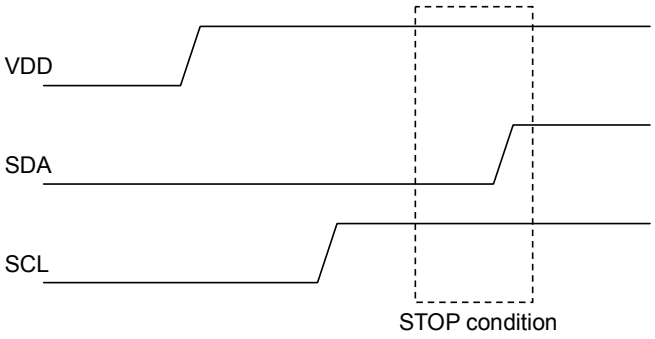


Fig. BU9796FS-5 Stop condition

(2) Generate START condition.
(3) Issue slave address
(4) Execute Software Reset (ICSET) command

● IO Equivalent Circuit (BU9796FS)

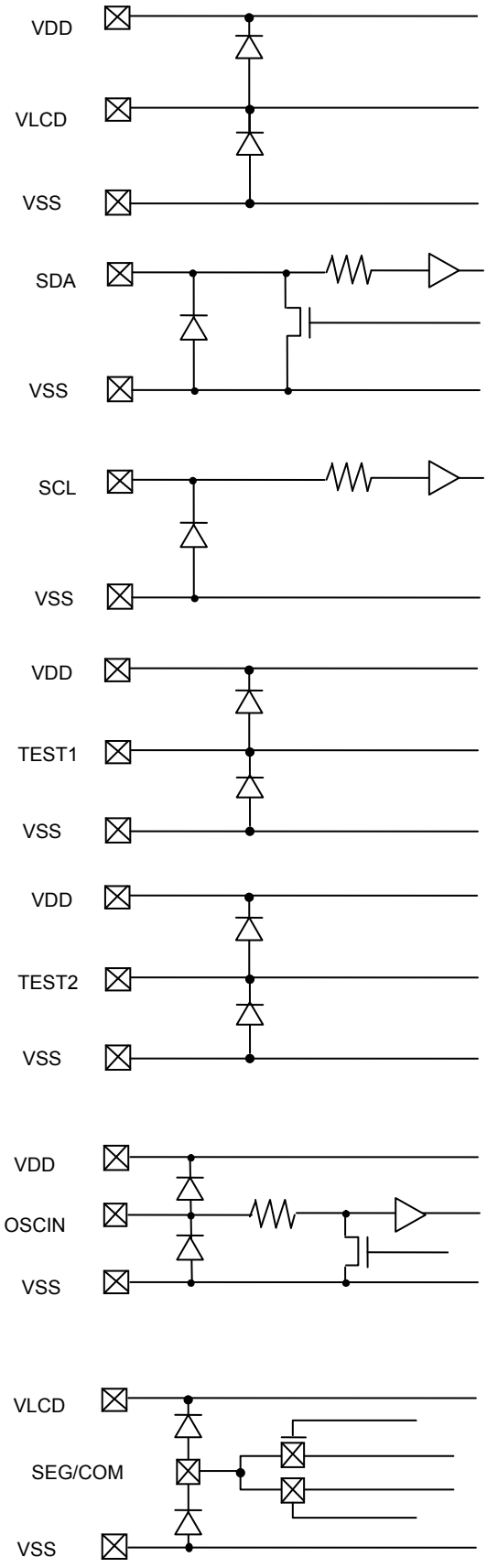


Fig. BU9796FS-6 I/O equivalent circuit

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

● Order form name selection

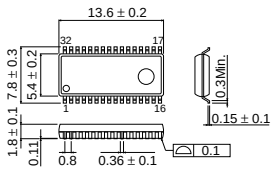
B	U	9	7	9	6	F	S	–	E	2

ROHM form name　Part No.　Package type　Packaging and forming specification

FS: SSOP-A32　E2 =Reel-shaped emboss taping

SSOP-A32

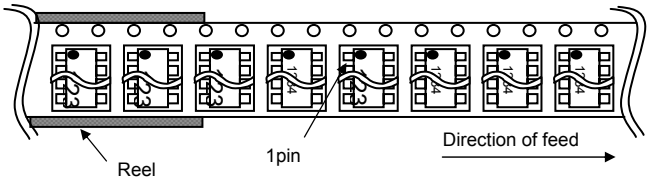
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



※When you order , please order in times the amount of package quantity.

BU9716BKV／BU9718KV 96SEGMENT (32SEG×3COM) Driver

● Features (BU9716BKV/BU9718KV)

1) LCD driving port : 3 Common output, 32 Segment output
2) Display duty: 1/3duty
3) Each 1/2 or 1/3 can be selected for power supply for LCD display.

● Uses (BU9716BKV/BU9718KV)

Portable equipments（POS, ECR, PDA etc.）
DSC, DSC, Telephone etc.

● Line up (BU9716BKV/BU9718KV)

Parameter	BU9716BKV	BU9718KV
Recommended operating voltage	4.5～5.5V	2.7～3.5V
Package	VQFP-48C	VQFP-48C

● ABSOLUTE MAXIMUM RATINGS (Ta=25degree, Vss=0V) (BU9716BKV/BU9718KV)

Parameter	Symbol	Pin	Ratings	Unit
Maximum Supply Voltage	VDD	VDD	-0.3～+7.0	V
Input Voltage	VIN	OSC,CS,CK,DI,$\overline{RES}$	-0.3～VDD+0.3	V
Output Voltage	VOUT	OSC	-0.3～VDD+0.3	V
Output Current	ISO	S1～S32	300	mA
	ICO	COM1～COM3	3	mA
Power Dissipation	Pd	―	400	mW
Storage Temperature Range	Tstg	―	-55～+125	degree

Note: Derating decreases at -4mW/degree for operation above Ta=25degree.

● RECOMMENDED OPERATING CONDITIONS

◎ BU9716BKV

Parameter	Symbol	Pin	MIN	TYP	MAX	Unit
Supply Voltage	VDD	VDD	+4.5		+5.5	V
Input Voltage	VDD1	VDD1	0	2/3VDD	VDD	V
	VDD2	VDD2	0	1/3VDD	VDD	V
Operating Temperature	Topr	―	-40		+85	degree

◎ BU9718KV

Parameter	Symbol	Pin	MIN	TYP	MAX	Unit
Supply Voltage	VDD	VDD	+2.7	-	+3.5	V
Input Voltage	VDD1	VDD1	0	2/3VDD	VDD	V
	VDD2	VDD2	0	1/3VDD	VDD	V
External Input wave frequency	fOSC	OSC	-	38	100	kHz
Recommended external resistor	R	OSC	-	47	-	kΩ
Recommended external capacitor	C	OSC	-	1000	-	pF
Operating Temperature	Topr	―	-40	-	+85	degree

* This product is not designed to be protected against radiation.

● ERECTRICAL CHARACTERISTICS

◎ BU9716BKV (VDD=4.5V-5.5V, Ta=25degree)

Parameter	Symbol	Pin	Condition	MIN	TYP	MAX	Unit
"H" Level Input Voltage	VIH	CS,CK,DI,$\overline{RES}$		0.8VDD	-	VDD	V
"L" Level Input Voltage	VIL	CS,CK,DI,$\overline{RES}$		0	-	0.2VDD	V
"H" Level Input Current	IIH	CS,CK,DI,$\overline{RES}$	VI=VDD	0	-	6.0	uA
"L" Level Input Current	IIL	CS,CK,DI,$\overline{RES}$	VI=VSS	0	-	6.0	uA
"H" Level Output Voltage	VSOH	S1～S32	IO=-20mA	-	VDD-1.0	-	V
	VCOH	COM1～COM3	IO=-100mA	-	VDD-1.0	-	V
"L" Level Output Voltage	VSOL	S1～S32	IO=20mA	-	1.0	-	V
	VCOL	COM1～COM3	IO=100mA	-	1.0	-	V
Center-Level Output Voltage	VCM1	COM1～COM3	1/2bias	-	1/2 VDD	-	V
	VSM1	S1～S32	1/3bias	-	2/3 VDD	-	V
	VCM2	COM1～COM3	1/3bias	-	2/3 VDD	-	V
	VSM2	S1～S32	1/3bias	-	1/3 VDD	-	V
	VCM3	COM1～COM3	1/3bias	-	1/3 VDD	-	V
Supply Current	IQ		Low Power Mode	-	30	70	uA
	IDD		fOSC=38kHz	-	200	500	uA

◎ BU9718KV (VDD=2.7-3.5V, Ta=25degree)

Parameter	Symbol	Pin	Condition	MIN	TYP	MAX	Unit
"H" level Input Voltage	VIH	CS,CK,DI,$\overline{RES}$		0.8VDD	-	VDD	V
"L" Level Input Voltage	VIL	CS,CK,DI,$\overline{RES}$		0	-	0.2VDD	V
"H" Level Input Current	IIH	CS,CK,DI,$\overline{RES}$	VI=VDD	0	-	6.0	uA
"L" Level Input Current	IIL	CS,CK,DI,$\overline{RES}$	VI=VSS	0	-	6.0	uA
"H" Level Output Voltage	VSOH	S1～S32	IO=-20mA	-	VDD-1.0	-	V
	VCOH	COM1～COM3	IO=-100mA	-	VDD-1.0	-	V
"L" Level Output Voltage	VSOL	S1～S32	IO=20mA	-	1.0	-	V
	VCOL	COM1～COM3	IO=100mA	-	1.0	-	V
Center-Level Output Voltage	VCM1	COM1～COM3	1/2bias	-	1/2 VDD	-	V
	VSM1	S1～S32	1/3bias	-	2/3 VDD	-	V
	VCM2	COM1～COM3	1/3bias	-	2/3 VDD	-	V
	VSM2	S1～S32	1/3bias	-	1/3 VDD	-	V
	VCM3	COM1～COM3	1/3bias	-	1/3 VDD	-	V
Supply Current	IQ		Low Power Mode	-	0.1	30	uA
	IDD		fOSC=38kHz	-	100	300	uA

● AC ERECTRICAL CHARACTERISTICS

◎ BU9716BKV (VDD=4.5-5.5V, Ta=25degree)

Parameter	Symbol	Pin	MIN	TYP	MAX	Unit
Recommended External Resistance	R	OSC	-	47	-	kΩ
Recommended External Capacitance	C	OSC	-	1000	-	pF
Oscillator frequency guaranteed range	fOSC	OSC	19	38	76	kHz
Data Setup Time	tDS	CK,DI	100	-	-	ns
Data Hold Time	tDH	CK,DI	100	-	-	ns
CS Setup Time	tCS	CS,CK	100	-	-	ns
CS Hold Time	tCH	CS,CK	100	-	-	ns
CK High-Level Pulse width	tCKH	CK	100	-	-	ns
CK Low-Level Pulse width	tCKL	CK	100	-	-	ns
Rise Time	tr	CS,CK,DI	-	-	300	ns
Fall Time	tf	CS,CK,DI	-	-	300	ns

◎ BU9718KV (VDD=2.7V-3.5V, Ta=25degree)

Parameter	Symbol	Pin	MIN	TYP	MAX	Unit	Condition
Oscillator frequency guaranteed range	fOSC	OSC	10	38	80	kHz	R=47kΩ,C=1000pF
Operating frequency	fOSC	OSC	-	-	100	kHz	External Input case
Data Setup Time	tDS	CK,DI	200	-	-	ns	
Data Hold Time	tDH	CK,DI	200	-	-	ns	
CS Setup Time	tCS	CS,CK	200	-	-	ns	
CS Hold Time	tCH	CS,CK	200	-	-	ns	
CK High-Level Pulse width	tCKH	CK	200	-	-	ns	
CK Low-Level Pulse width	tCKL	CK	200	-	-	ns	
Rise Time	tr	CS,CK,DI	-	-	100	ns	
Fall Time	tf	CS,CK,DI	-	-	100	ns	

Fig. BU9716BKV/BU9718KV-2 CK: Normal Low Level case

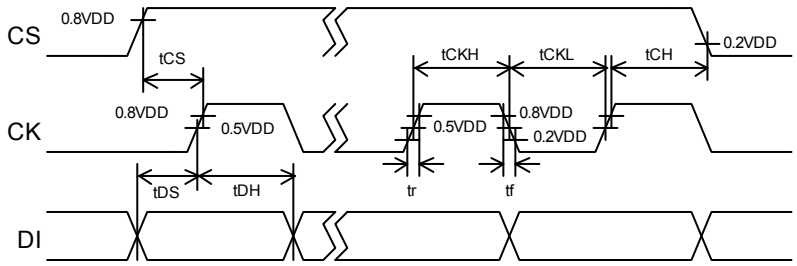
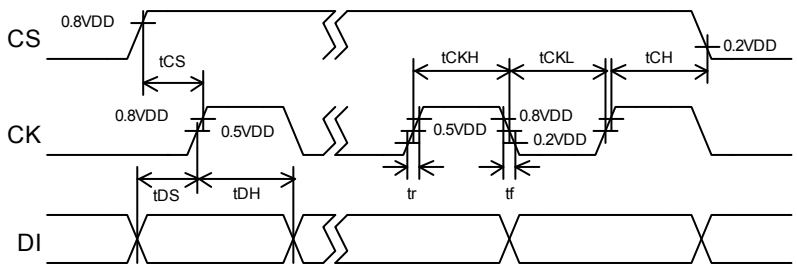


Fig. BU9716BKV/BU9718KV-3 CK: Normal High Level case



◎ BU9716BKV

● Block Diagram

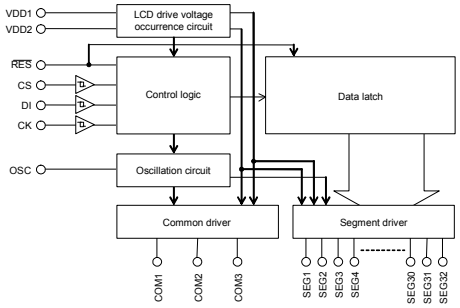


Fig. BU9716BKV /BU9718KV-3
BU9716BKV Block Diagram

● Pin assignment

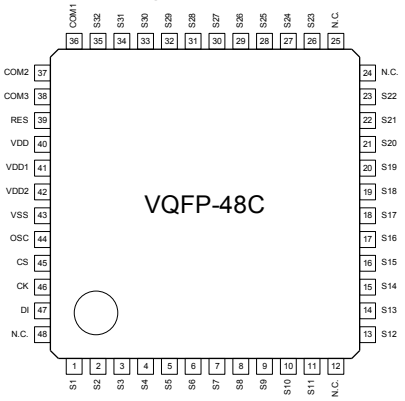


Fig. BU9716BKV /BU9718KV-4
BU9716BKVPin assignment

● Terminal description

Pin No,	Terminal	I/O	Description	Unused
1-11 13-23 26-35	S1-S32	O	Segment output pins. It output the proper LCD voltage levels corresponding to the input data multiplexed with COM1 to CPM3.	OPEN
36 37 38	COM1 COM2 COM3	O	Common driver output pins. Frame frequency: fO＝（fOSC／384）Hz	OPEN
39	$\overline{RES}$	I	Active low reset input. Used for resetting all latches. (Include Control Code.)	VDD
44	OSC	-	Internal Oscillator connection for an external resister and capacitor which determines fOSC.	VSS
45	CS	I	Chip select. Used for serial data transfer. Active high.	VSS
46	CK	I	Input data clock. Used for serial data transfer.	VSS
47	DI	I	Data input. Used for serial data transfer.	VSS
41	VDD1	-	Internal voltage reference connection. Connect to VDD2 at 1/2 bias mode.	OPEN
42	VDD2	-	Internal voltage reference connection. Connect to VDD1 at 1/2 bias mode.	OPEN

◎ BU9718KV

● Block Diagram

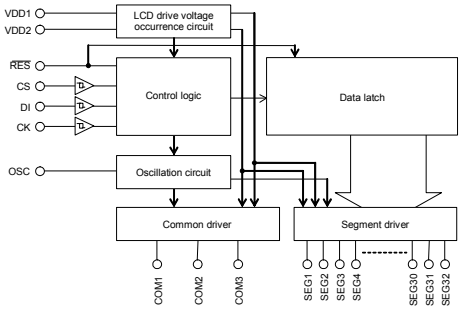


Fig. BU9716BKV /BU9718KV-5
BU9718KV Block Diagram

● Pin assignment

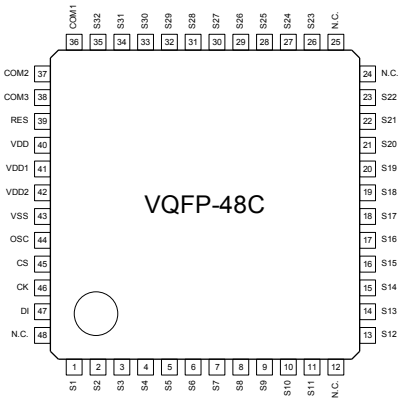


Fig. BU9716BKV /BU9718KV-6
BU9718KV Pin assignment

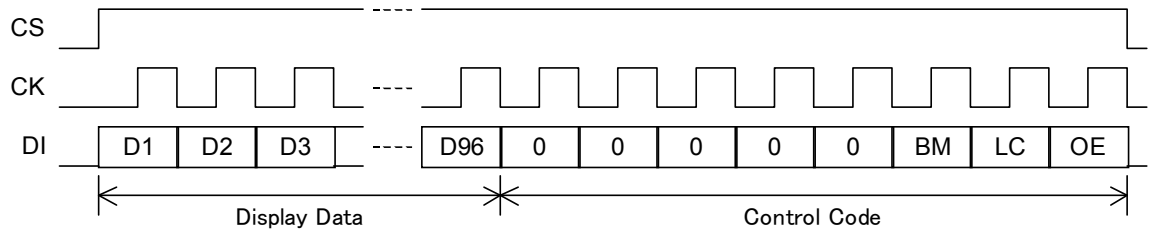
● Terminal description

Pin No,	Terminal	I/O	Description	Unused
1-11 13-23 26-35	S1-S32	O	Segment output pins. It output the proper LCD voltage levels corresponding to the input data multiplexed with COM1 to CPM3.	OPEN
36 37 38	COM1 COM2 COM3	O	Common driver output pins. Frame frequency: fO＝（fOSC／384）Hz	OPEN
39	$\overline{RES}$	I	Active low reset input. Used for resetting all latches. (Include Control Code.)	VDD
44	OSC	-	Internal Oscillator connection for an external resister and capacitor which determines fOSC.	VSS
45	CS	I	Chip select. Used for serial data transfer. Active high.	VSS
46	CK	I	Input data clock. Used for serial data transfer.	VSS
47	DI	I	Data input. Used for serial data transfer.	VSS
41	VDD1	-	Internal voltage reference connection. Connect to VDD2 at 1/2 bias mode.	OPEN
42	VDD2	-	Internal voltage reference connection. Connect to VDD1 at 1/2 bias mode.	OPEN

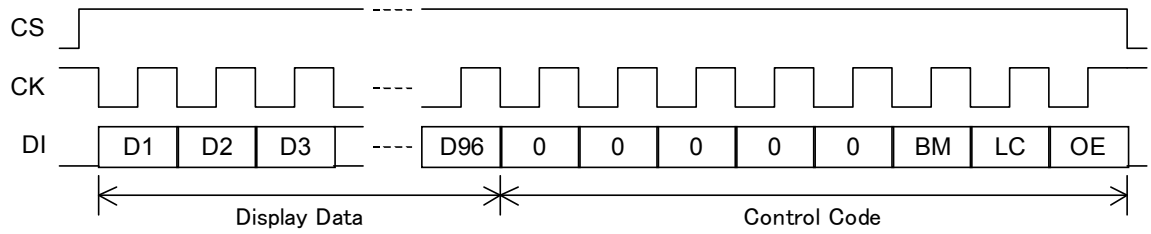
● Timing chart

◎ Command / data Input

1. CK: Normal Low level case



2. CK: Normal High level case



Data transfer is enabled when CS is asserted high. The value of DI is shifted into the shift register on the rising edge of CK. After all of the data in DI is sifted in, CS must be asserted low. The new display data and control code takes effect after the falling edge of CS.

◎ Control Code

OE	Output-Enable Control
0	Normal Operation
1	Blank Display-as if all display data =0(Oscillator is active.)

LC	Low-power Mode Control
0	Normal Operation
1	Low-power Mode: Oscillator is stopped, segment /common outputs=”L”

BM	Bias Mode Control
0	1／3 Bias
1	1／2 Bias

◎ DISPLAY DATA

SEGMENT	COM3	COM2	COM1	SEGMENT	COM3	COM2	COM1
S1	D1	D2	D3	S17	D49	D50	D51
S2	D4	D5	D6	S18	D52	D53	D54
S3	D7	D8	D9	S19	D55	D56	D57
S4	D10	D11	D12	S20	D58	D59	D60
S5	D13	D14	D15	S21	D61	D62	D63
S6	D16	D17	D18	S22	D64	D65	D66
S7	D19	D20	D21	S23	D67	D68	D69
S8	D22	D23	D24	S24	D70	D71	D72
S9	D25	D26	D27	S25	D73	D74	D75
S10	D28	D29	D30	S26	D76	D77	D78
S11	D31	D32	D33	S27	D79	D80	D81
S12	D34	D35	D36	S28	D82	D83	D84
S13	D37	D38	D39	S29	D85	D86	D87
S14	D40	D41	D42	S30	D88	D89	D90
S15	D43	D44	D45	S31	D91	D92	D93
S16	D46	D47	D48	S32	D94	D95	D96

● Cautions on use

(1) Absolute Maximum Ratings
An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down devices, thus making impossible to identify breaking mode such as a short circuit or an open circuit. If any special mode exceeding the absolute maximum ratings is assumed, consideration should be given to take physical safety measures including the use of fuses, etc.

(2) Operating conditions
These conditions represent a range within which characteristics can be provided approximately as expected. The electrical characteristics are guaranteed under the conditions of each parameter.

(3) Reverse connection of power supply connector
The reverse connection of power supply connector can break down ICs. Take protective measures against the breakdown due to the reverse connection, such as mounting an external diode between the power supply and the IC's power supply terminal.

(4) Power supply line
Design PCB pattern to provide low impedance for the wiring between the power supply and the GND lines. In this regard, or the digital block power supply and the analog block power supply, even though these power supplies has the same level of potential, separate the power supply pattern for the digital block from that for the analog block, thus suppressing the diffraction of digital noises to the analog block power supply resulting from impedance common to the wiring patterns. For the GND line, give consideration to design the patterns in a similar manner.
Furthermore, for all power supply terminals to ICs, mount a capacitor between the power supply and the GND terminal. At the same time, in order to use an electrolytic capacitor, thoroughly check to be sure the characteristics of the capacitor to be used present no problem including the occurrence of capacity dropout at a low temperature, thus determining the constant.

(5) GND voltage
Make setting of the potential of the GND terminal so that it will be maintained at the minimum in any operating state. Furthermore, check to be sure no terminals are at a potential lower than the GND voltage including an actual electric transient.

(6) Short circuit between terminals and erroneous mounting
In order to mount ICs on a set PCB, pay thorough attention to the direction and offset of the ICs. Erroneous mounting can break down the ICs. Furthermore, if a short circuit occurs due to foreign matters entering between terminals or between the terminal and the power supply or the GND terminal, the ICs can break down.

(7) Operation in strong electromagnetic field
Be noted that using ICs in the strong electromagnetic field can malfunction them.

(8) Inspection with set PCB
On the inspection with the set PCB, if a capacitor is connected to a low-impedance IC terminal, the IC can suffer stress. Therefore, be sure to discharge from the set PCB by each process. Furthermore, in order to mount or dismount the set PCB to/from the jig for the inspection process, be sure to turn OFF the power supply and then mount the set PCB to the jig. After the completion of the inspection, be sure to turn OFF the power supply and then dismount it from the jig. In addition, for protection against static electricity, establish a ground for the assembly process and pay thorough attention to the transportation and the storage of the set PCB.

(9) Input terminals
In terms of the construction of IC, parasitic elements are inevitably formed in relation to potential. The operation of the parasitic element can cause interference with circuit operation, thus resulting in a malfunction and then breakdown of the input terminal. Therefore, pay thorough attention not to handle the input terminals, such as to apply to the input terminals a voltage lower than the GND respectively, so that any parasitic element will operate. Furthermore, do not apply a voltage to the input terminals when no power supply voltage is applied to the IC. In addition, even if the power supply voltage is applied, apply to the input terminals a voltage lower than the power supply voltage or within the guaranteed value of electrical characteristics.

(10) Ground wiring pattern
If small-signal GND and large-current GND are provided, It will be recommended to separate the large-current GND pattern from the small-signal GND pattern and establish a single ground at the reference point of the set PCB so that resistance to the wiring pattern and voltage fluctuations due to a large current will cause no fluctuations in voltages of the small-signal GND. Pay attention not to cause fluctuations in the GND wiring pattern of external parts as well.

(11) External capacitor
In order to use a ceramic capacitor as the external capacitor, determine the constant with consideration given to a degradation in the nominal capacitance due to DC bias and changes in the capacitance due to temperature, etc.

(12) No Connecting input terminals
In terms of extremely high impedance of CMOS gate, to open the input terminals causes unstable state. And unstable state brings the inside gate voltage of p-channel or n-channel transistor into active. As a result, battery current may increase. And unstable state can also causes unexpected operation of IC. So unless otherwise specified, input terminals not being used should be connected to the power supply or GND line.

(13) Rush current
When power is first supplied to the CMOS IC, it is possible that the internal logic may be unstable and rush current may flow instantaneously. Therefore, give special condition to power coupling capacitance, power wiring, width of GND wiring, and routing of connections.

● Order form name selection

B	U	9	7	1	8	K	V

ROHM form name

Part No.

BU9716B: 4.5V-5.5V

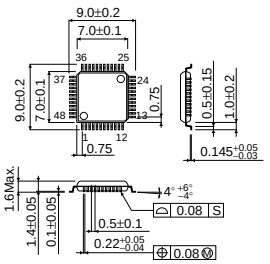
BU9718: 2.7V-3.5V

Package type

KV: VQFP

VQFP48C

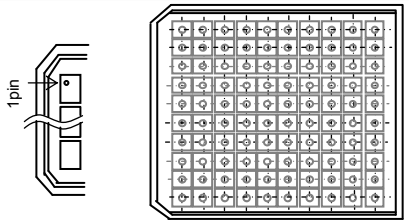
<Dimension>



(Unit:mm)

<Packing information>

Container	Tray
Quantity	1000pcs
Direction of feed	Direction of product is fixed in a tray.



□When you order , please order in times the amount of package quantity.

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