Benchmarq Products
r[illegible]ents

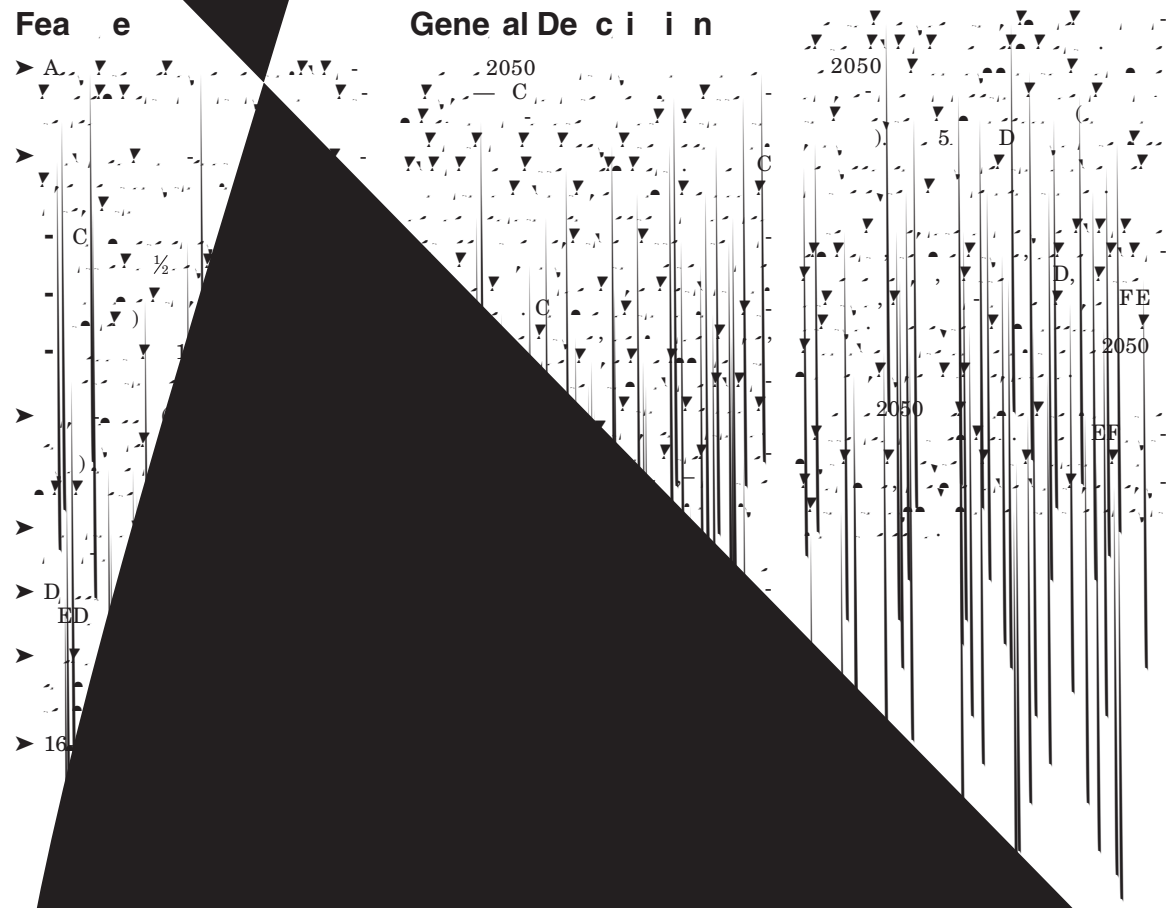
b2050H

Fea[illegible]e

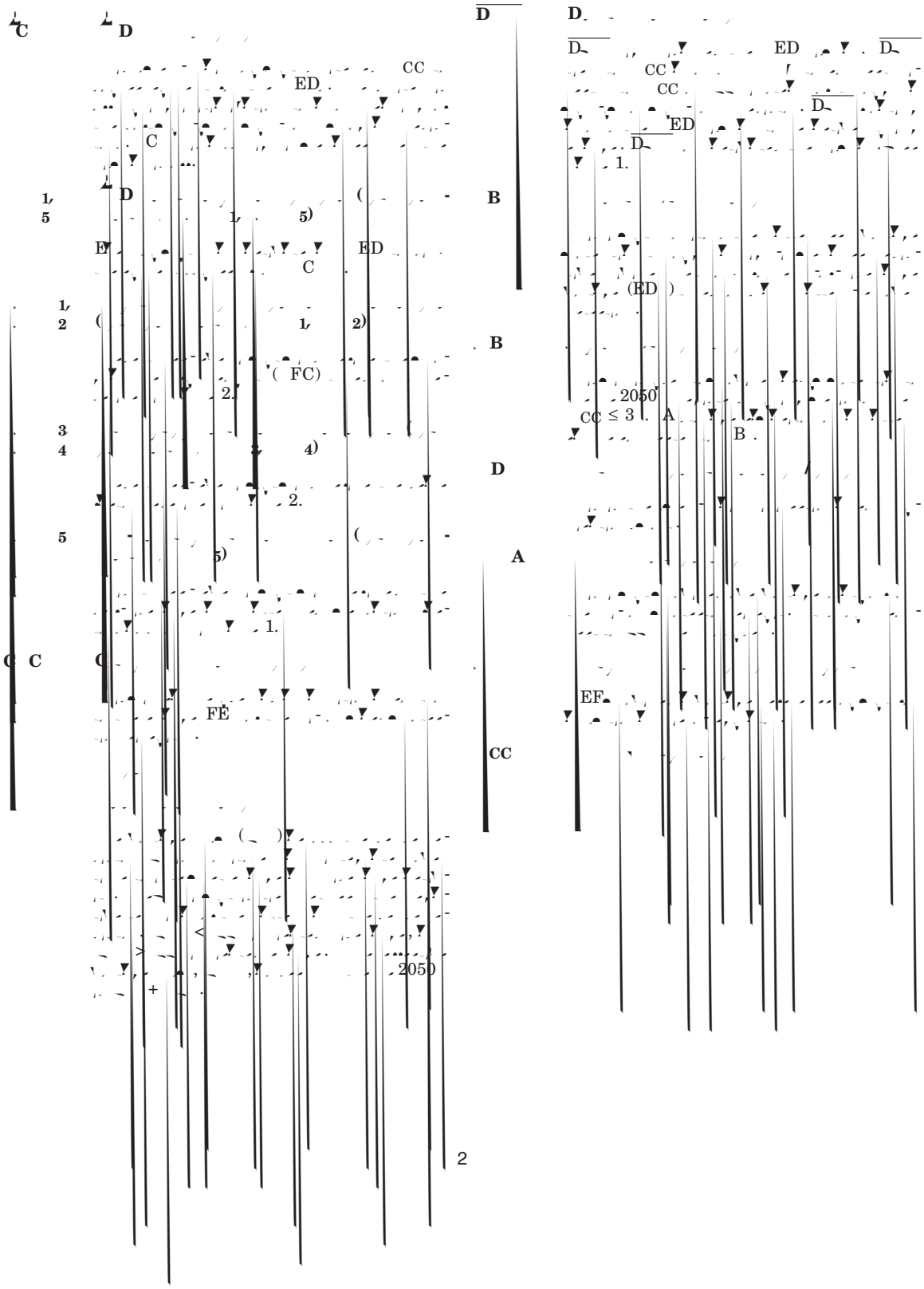
- A[illegible]
- [illegible]
  - C[illegible]
  - [illegible] ½ [illegible]
  - [illegible])
  - [illegible]
- [illegible]
  - [illegible])
- [illegible]
- D[illegible]
  ED[illegible]
- [illegible]
- 16[illegible]

Gene al De c i i n

2050
— C
C
C
2050
). 5 D (
D,
FE
2050
2050
EF



Pin De c i i n


C
D
CC
ED
C
D
1
5
1
5)
E
ED
C
1
2
1
2)
(FC)
2.
3
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3
4)
2.
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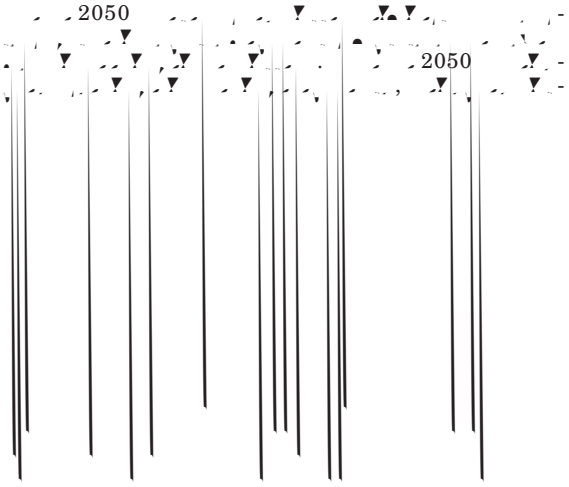
5)
1.
C
C
FE
( )
2050
+
D
D
D
ED
D
CC
CC
D
ED
D
1.
B
(ED)
B
2050
CC ≤ 3
A
B
D
A
EF
CC

F nc i nal De c i i n

Gene al O e a i n



V l age Th e h ld

TMP (he)	Tem e a e Range
0	< -30 C
1	-30 C -20 C
2	-20 C -10 C
34	

2050

B

$$\frac{B1}{B2} = 4 - 1$$

B1
B2

(ED)

ED

ED 2050

ED 1 ( ) = 0.76

ED F ( ) = ED 1-0.025 = 0.735

ED

D 2050

ED

2C (D F = 1)

2C

½

RBI In

B

2050

3.0 CC B CC 3.0

( )

Re e

2050 CC

B 15

00 FC (= 1E)

00 D (= 05).

Tem e a e

2050

10 C -35 C +85 C.

10 C

:

La C n ide a i n

2050

( )

C C F

C

A

(C1 C2)

CC B

A

0.1uF CC.

( )

2050

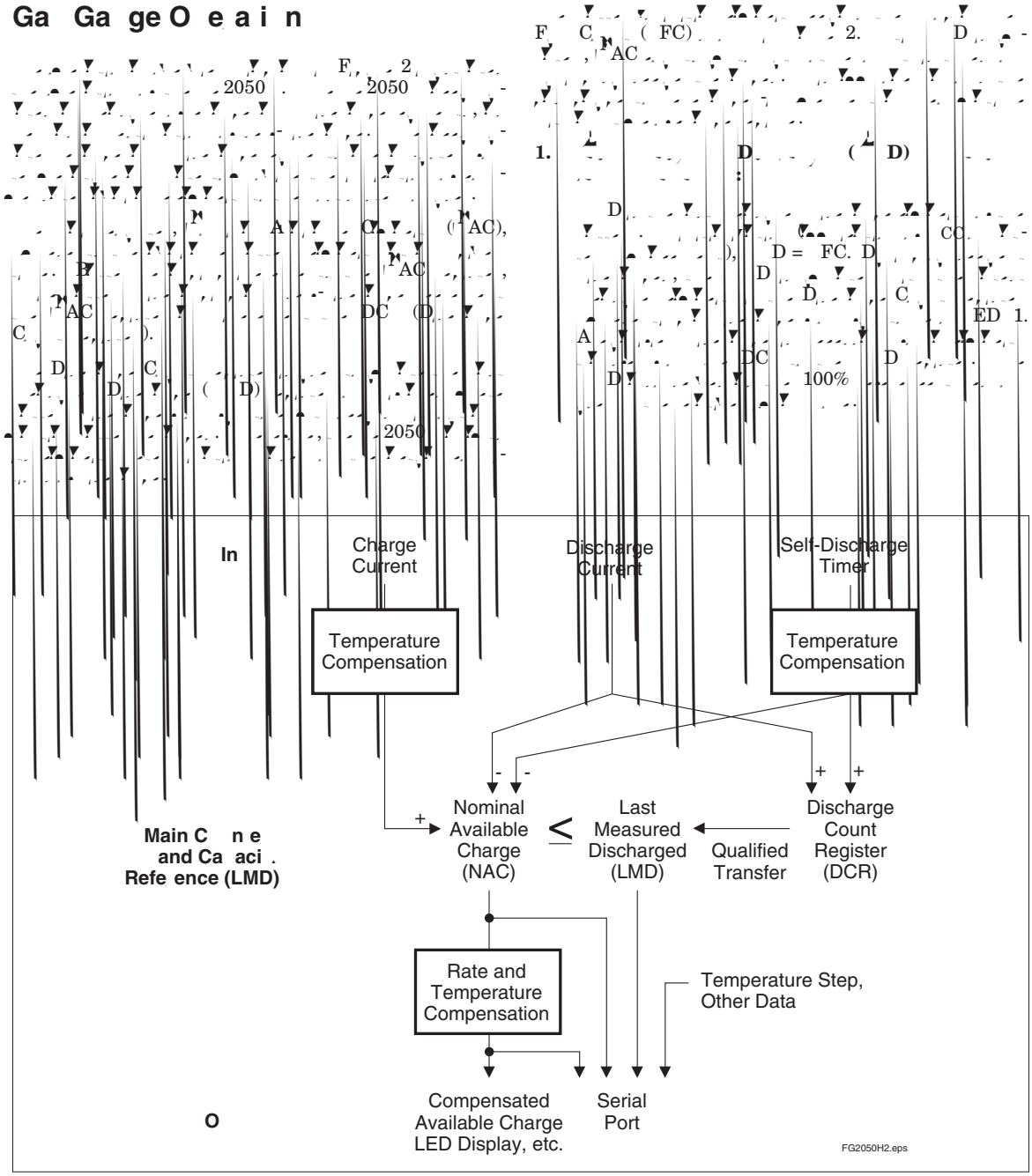


Figure 2. Operational Overview

2. **C (C)** -

:

D

1 4. 2050

FC 2. FC

A :

B (A) * (Ω) =

FC ( )

FC

2050 .

Example: Selecting a PFC Value

:

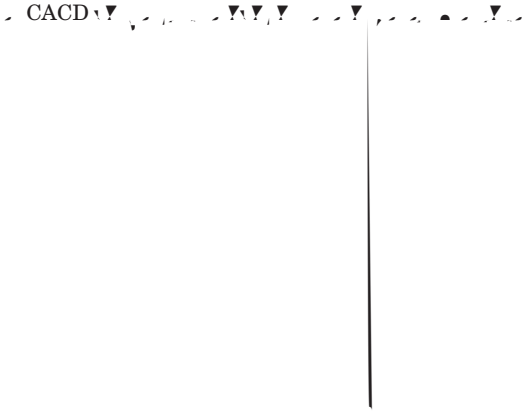
= 0.05Ω

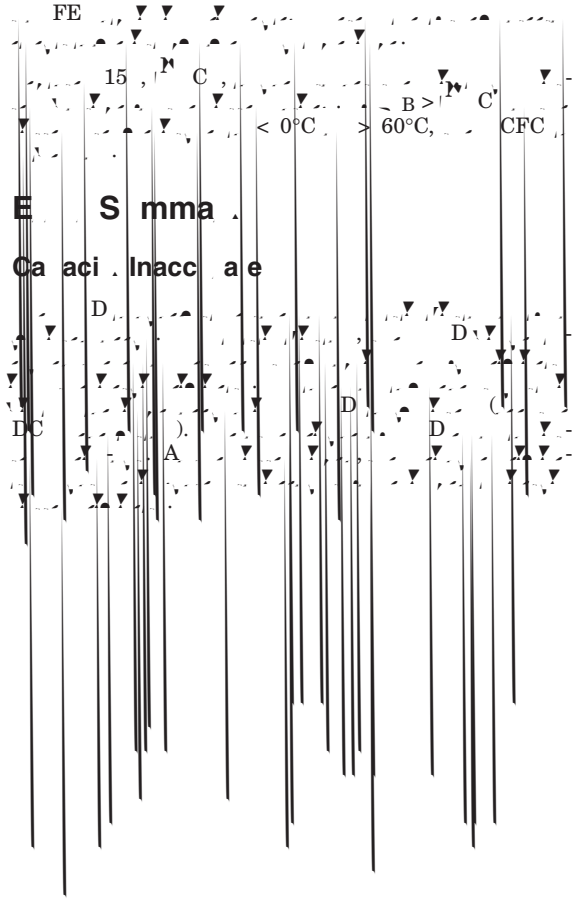
= 2

= 1000 A ,

= 50 A 1A

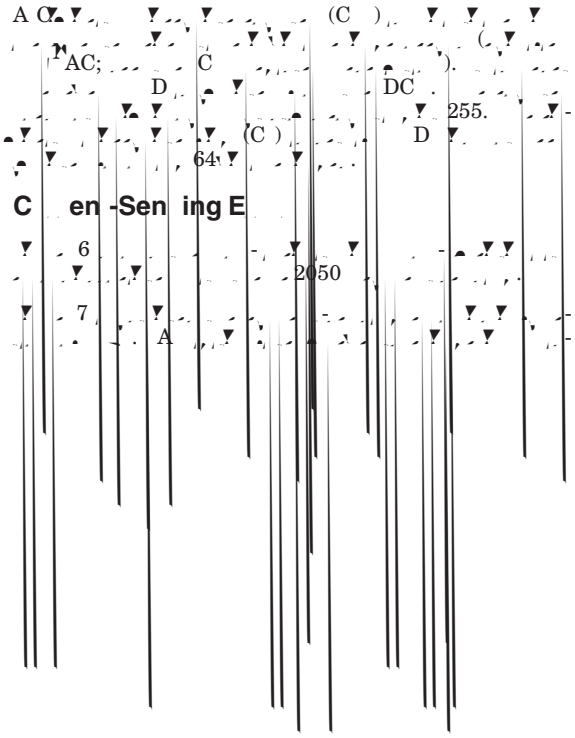
=


CACD



E S mma

Ca aci Inacc a e

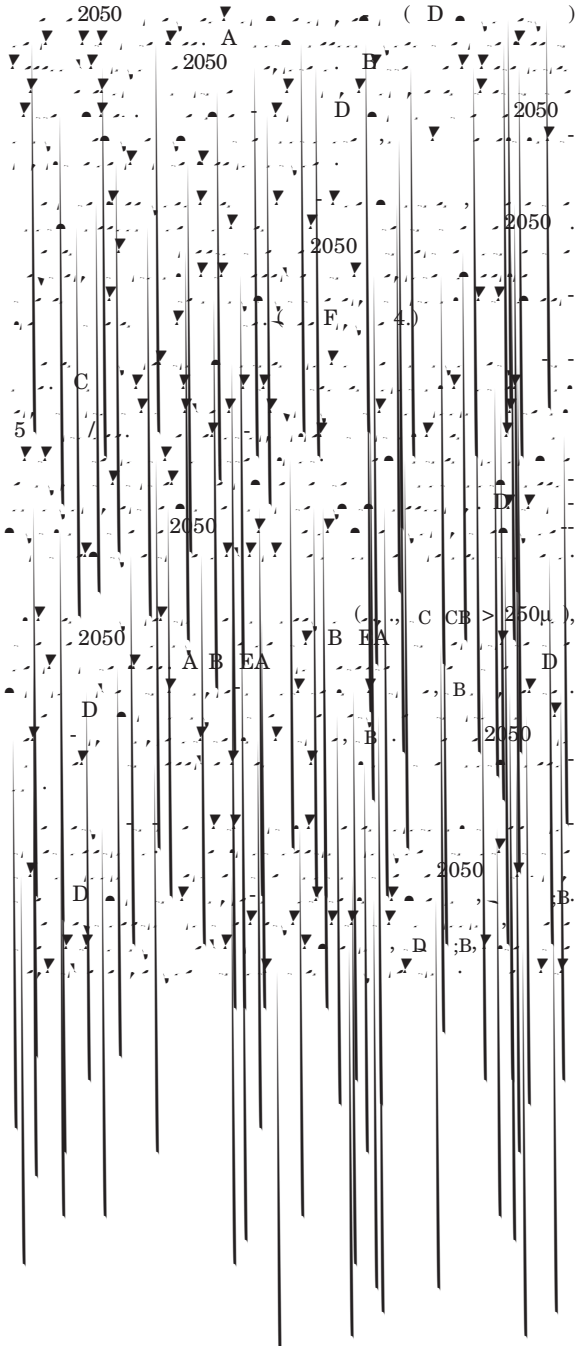


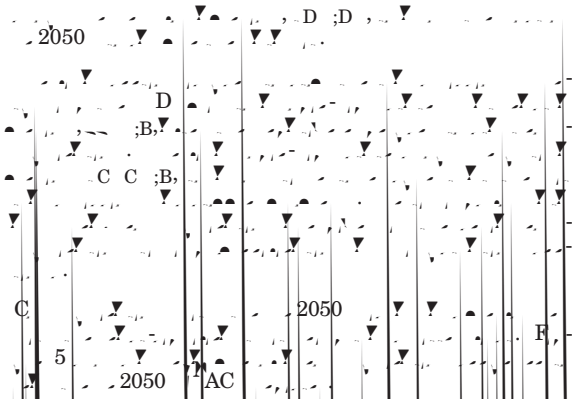
C en -Sen ing E

Table 7. VOS-Rela ed C en Sen e E (C en = 1A)

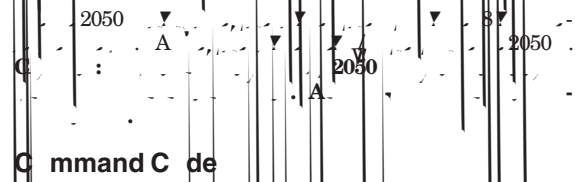
VOS (µV)	Sen e Re i			
	20	50	100	Ω
50	0.25	0.10	0.05	%
100	0.50	0.20	0.10	%
150	0.75	0.30	0.15	%
180	0.90	0.36	0.18	%

C mm nica ing Wi h he b◂2050H

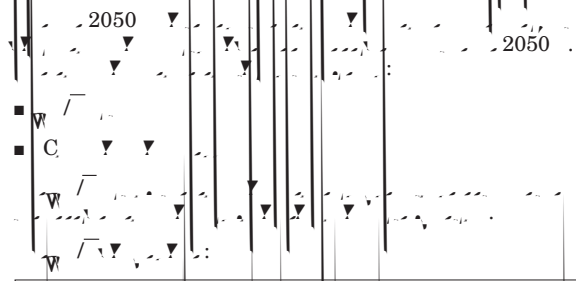




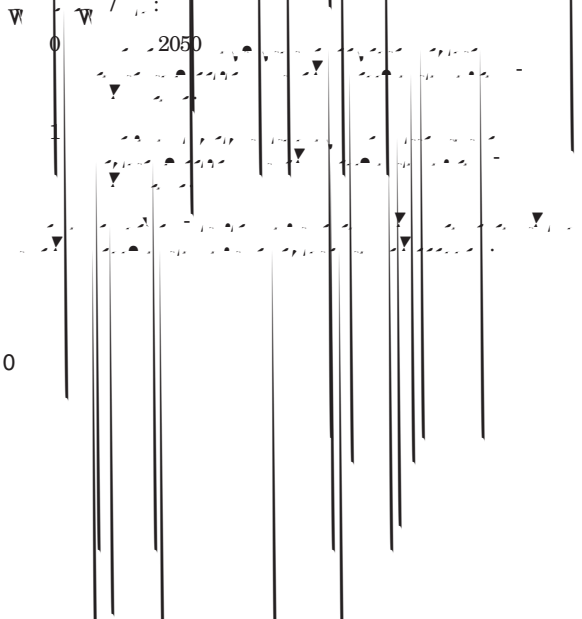
b◂2050H C mmand C de and Regi e



C mmand C de



C mmand C de Bi							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	-



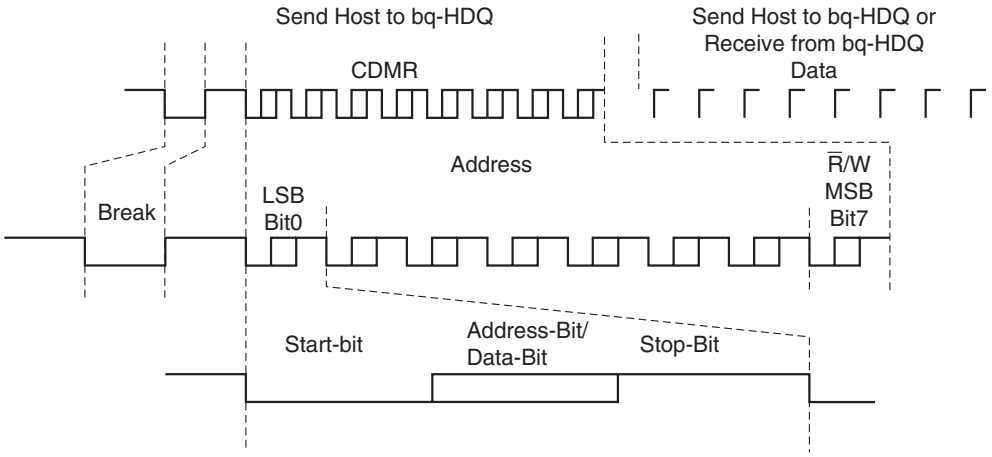

Send Host to bq-HDQ
Send Host to bq-HDQ or
Receive from bq-HDQ
CDMR
Data
Address
R/W
MSB
Bit7
Break
LSB
Bit0
Start-bit
Address-Bit/
Data-Bit
Stop-Bit
TD201807.eps

Table 8. b◂2050H C mmand and S a Regi e

S.mb l	Regi e Name	L c. (he)	Read/ W i e	C n l Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
F ⌝ 1		01		C ⌝	B	⌝ A	C	D	1	ED 1	ED F
		02		3	2	1	0	3	2	1	0
⌜AC		03	⁄W	⌜AC 7	⌜AC 6	⌜AC 5	⌜AC 4	⌜AC 3	⌜AC 2	⌜AC 1	⌜AC 0
⌜AC		17	⁄W	⌜AC 7	⌜AC 6	⌜AC 5	⌜AC 4	⌜AC 3	⌜AC 2	⌜AC 1	⌜AC 0
BA D		04	⁄W	BA D7	BA D6	BA D5	BA D4	BA D3	BA D2	BA D1	BA D0
D		05	⁄W	D7	D6	D5	D4	D3	D2	D1	D0
F ⌝ 2		06		⌝ D	D 2	D 1	D 0	E⌜ ⌜		⌝ D	D
D		07		⌝ D	⌝ D	⌝ D	D5	D4	D3	D2	D1
		08		⌝ D	⌝ D	⌝ D	5	4	3	2	1
C		09	⁄W	C 7	C 6	C 5	C 4	C 3	C 2	C 1	C 0
⌝ B		0		⌝ B7	⌝ B6	⌝ B5	⌝ B4	⌝ B3	⌝ B2	⌝ B1	⌝ B0
⌝		0.	⁄W	⌝ 7	⌝ 6	⌝ 5	⌝ 4	⌝ 3	⌝ 2	⌝ 1	⌝ 0
CAC		0	⁄W	CAC 7	CAC 6	CAC 5	CAC 4	CAC 3	CAC 2	CAC 1	CAC 0
CACD		0.	⁄W	CACD7	CACD6	CACD5	CACD4	CACD3	CACD2	CACD1	CACD0
⌝ AE		0.		⌝ AE 7	⌝ AE 6	⌝ AE 5	⌝ AE 4	⌝ AE 3	⌝ AE 2	⌝ AE 1	⌝ AE 0
⌝ AE		10		⌝ AE 7	⌝ AE 6	⌝ AE 5	⌝ AE 4	⌝ AE 3	⌝ AE 2	⌝ AE 1	⌝ AE 0
CAC	CAC	11		-	CAC6	CAC5	CAC4	CAC3	CAC2	CAC1	CAC0
⌝		12		⌝ 7	⌝ 6	⌝ 5	⌝ 4	⌝ 3	⌝ 2	⌝ 1	⌝ 0
⌝		13		⌝ 7	⌝ 6	⌝ 5	⌝ 4	⌝ 3	⌝ 2	⌝ 1	⌝ 0
⌜ C		15	⁄W	⌜ C 7	⌜ C 6	⌜ C 5	⌜ C 4	⌜ C 3	⌜ C 2	⌜ C 1	⌜ C 0
DC		18	⁄W	DC 7	DC 6	DC 5	DC 4	DC 3	DC 2	DC 1	DC 0
FC		1.	⁄W	⌝ D	⌝ D	⌝ D	⌝ D	⌝ D	⌝ D	⌝ D	⌝ D
⌜		38		⌝ D	⌝ D	⌝ D	⌝ D	DC	⌝ D	⌝ D	C
⌝		39	⁄W	⌝	0	0	0	0	0	0	0
E⁄ FF	C	3.	⁄W	1	1	1	1	1	1	1	1

. :

⌝ D =

A

C mmand C de Bi							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (B)

P ima . S a Flag Regi e (FLGS1)

F 1 (= 01) 2050 .

charge status (C) C > A C .

C :

FLGS1 Bi							
7	6	5	4	3	2	1	0
C	-	-	-	-	-	-	-

C :

0 E ≤

1 >

battery replaced (B) 2050 CC B AC D, ED 1 B = 1 .

B :

FLGS1 Bi							
7	6	5	4	3	2	1	0
-	B	-	-	-	-	-	-

B :

0 B AC = D ED 1

1 2050

protector status (A) A .

A :

FLGS1 Bi							
7	6	5	4	3	2	1	0
-	-	A	-	-	-	-	-

A :

0 A (A < 0.5)

1 A (A > 2.5)

capacity inaccurate (C) D C 64 D 2050 D .

C :

FLGS1 Bi							
7	6	5	4	3	2	1	0
-	-	-	C	-	-	-	-

C :

0 D -

1 A 64 D 2050

valid discharge (D) 2050 AC= D. D D :

- AC 6% D
- A > 2 AC .
- ED 1 0 C

D :

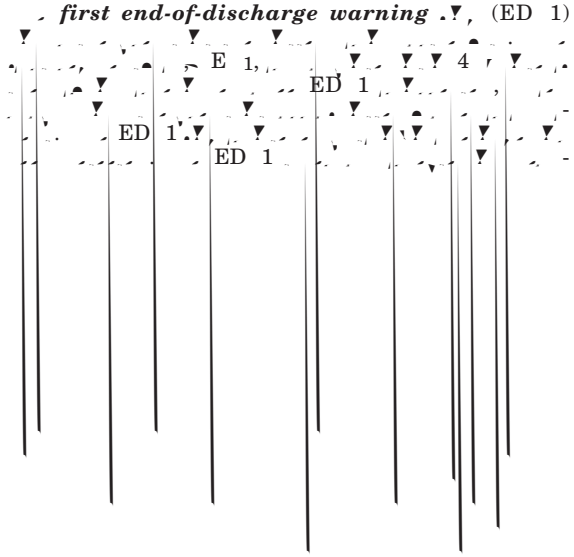
FLGS1 Bi							
7	6	5	4	3	2	1	0
-	-	-	-	D	-	-	-

D :

0 - 6% AC, ED 1 0 C,

1 AC = D

first end-of-discharge warning, (ED 1)



La Mea ed Di cha ge Regi e (LMD)

D =05) 2050
2050
D 2050
D FC
2050

D DC ED
D

DC < 0.94 D, D 0.94 * D.

Sec nda S a Flag Regi e (FLGS2)

F 2 =06)
2050 .

B 7 1 F 2 D

discharge rate D 2 0, 6 4.

:

enable interrupt (E) 2050 .

valid charge ( ), 2 F 2,
2050

AC = D.

:

W :

0

AC = D ED 1

1

overload (D)
2C D
0.5
2C.

C

AC > 0.94 * D,

C

C

AC < 0.94 * D.

C

AC. C 255

C

64, W C ,

F 1 C

D

C

Ba e V l age Regi e (VSB)

B B (

= 0B)

B = 1.2 * (B 256).

VSB Regi e B							
7	6	5	4	3	2	1	0
B7	B6	B5	B4	B3	B2	B1	B0

V l age Th e h ld Regi e (VTS)

(ED 1

ED F) =

0C) ED 1 . ED F

25 ED 1.

A2 , ED 1 = 0.76 ED F =

0.735 . ED 1 = 1.2 * (/256).

VTS Regi e Bi							
7	6	5	4	3	2	1	0
7	6	5	4	3	2	1	0

C m en a ed A ailable Cha ge Regi e (CACT/CACD)

CACD = 0E AC

> 0.5C AC.

CACD

AC CACD

D03 D(-11(D 127)-31E -1.12 -25.9474 51.12544 D ( )-493.55 AC 3(-222.4( )15(.-493. ( )

Ma im m Cell V l age Regi e (NMCV)

C (15)

CFC

C

CFC B

C

:

$$C = 2 \left(\frac{256 * C * B2}{1.2 * (B1 + B2)} \right)$$

W :

C =

C = 00

Di cha ge C n Regi e (DCR)

DC (= 18)

DC

FF DC ED 1 = 1

FF

P g am Pin F ll C n (PPFC)

FC

2050

DC V l age Th e h ld ($T_A = T_{OPR}$; V = 3.0 6.5V)

S.mb l	Pa ame e	Minim m	T. ical	Ma im m	Uni	N
ED 1	F	0.73	0.76	0.79		B,
ED F	F	ED 1 - 0.035	ED 1 - 0.025	ED 1 - 0.015		B,
		-300	-	+500		+

DC Elec ical Cha ac e i ic ($T_A = T_{OPR}$)

S.mb l	Pa ame e	Minim m	T. ical	Ma im m	Uni	N e
CC		3.0	4.25	6.5		CC < 2.0 ≥ 3.0
		-	±50	±150	µ	D = CC
EF	25 C	5.7	6.0	6.3		EF = 5µA
	-40 C +85 C	4.5	-	7.5		EF = 5µA
EF		2.0	5.0	-	Ω	EF = 3
CC		-	90	135	µA	CC = 3.0 , D = 0
		-	120	180	µA	CC = 4.25 , D = 0
		-	170	250	µA	CC = 6.5 , D = 0
B	B	0	-	CC		
B	B	10	-	-	Ω	0 < B < CC
D	D	-	-	5	µA	D =
C	C	-0.2	-	0.2	µA	D = CC
B	B	-	-	100	A	B > CC < 3
D		500	-	-	Ω	
		10	-	-	Ω	-200 < < CC
FC		CC - 0.2	-	-		1 5
FC		-	-	+ 0.2		1 5
FC			-			1 5
	E CC	-	0.1	-		CC = 3 , ≤ 1.75 A E 1 E 5, CFC
	E CC	-	0.4	-		CC = 6.5 , ≤ 11.0 A E 1 E 5, CFC
	C CC	CC - 0.3	-	-		CC = 3 , C = -5.25 A
	C CC	CC - 0.6	-	-		CC > 3.5 , C = -33.0 A
	E	11.0	-	-	A	A = 0.4 , CC = 6.5
		5.0	-	-	A	A = + 0.3 , D
		-	-	0.3		≤ 5 A, D
D	D	2.5	-	-		D
D	D	-	-	0.8		D
		2.5	-	-		A
		-	-	0.5		A
		-	-	200	Ω	1 5
F A	F	-	5	-	Ω	1 5

:

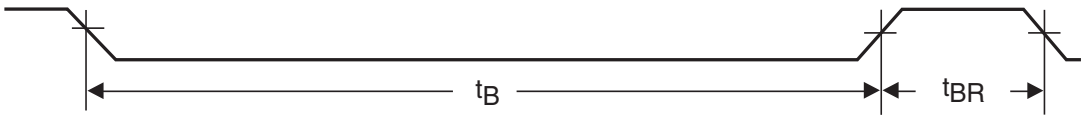
High-S eed Se ial C mm nica i n Timing S ecifica i n ($T_A = T_{OPR}$)

S.mb l	Pa ame e	Minim m	T. ical	Ma im m	Uni	N e
C C	C , , 2050 ( )	190	-	-	µ	
C CB	C , , 2050 ( )	190	205	250	µ	
	, 2050 ( )	5	-	-		
B	, 2050 ( )	32	-	-	µ	
D	D	-	-	50	µ	
D B	D	-	-	50	µ	
D	D	90	-	-	µ	
D	D	-	-	80	µ	
		-	-	145	µ	
B		-	-	145	µ	
	, 2050	190	-	320	µ	
B	B	190	-	-	µ	
B	B	40	-	-	µ	

: - D CC D

D

B eak Timing



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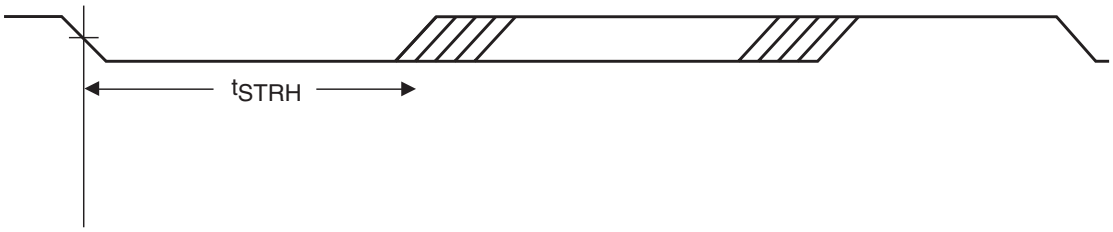
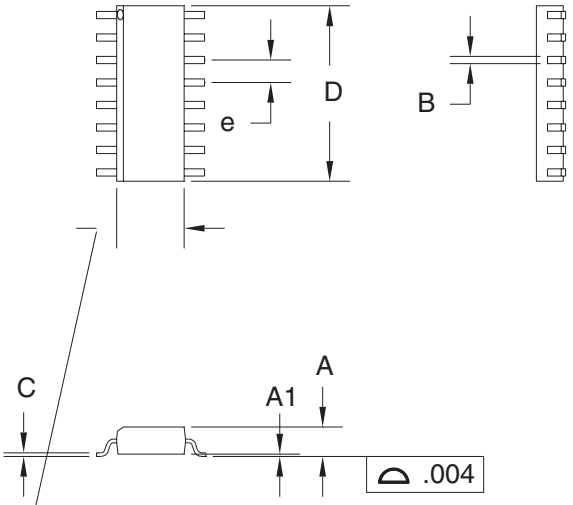


16-Pin SOIC Na (SN)



Da a Shee Re i i n Hi

ChangeN .	Page N .	De c i i n f Change
1	A	F
2	8	D 200µ 250µ .
2	18	200µ ( ) 250µ ( ).
2	18	D -200µ ( ) -250µ ( ).
3	3	
3	12	C
3	16	C
3	18	C +2000 +500
3	19	C 0.5 0.3
3	20	C B 95µ 145µ

: C 1 = A 1997 B 1996
C 2 = 1998 C A 1997 B.
C 3 = 1999 D 1998 C.

O de ing Inf ma i n

b-2050H

: = C (0 +70 C)

= 16 C

D :
2050 C

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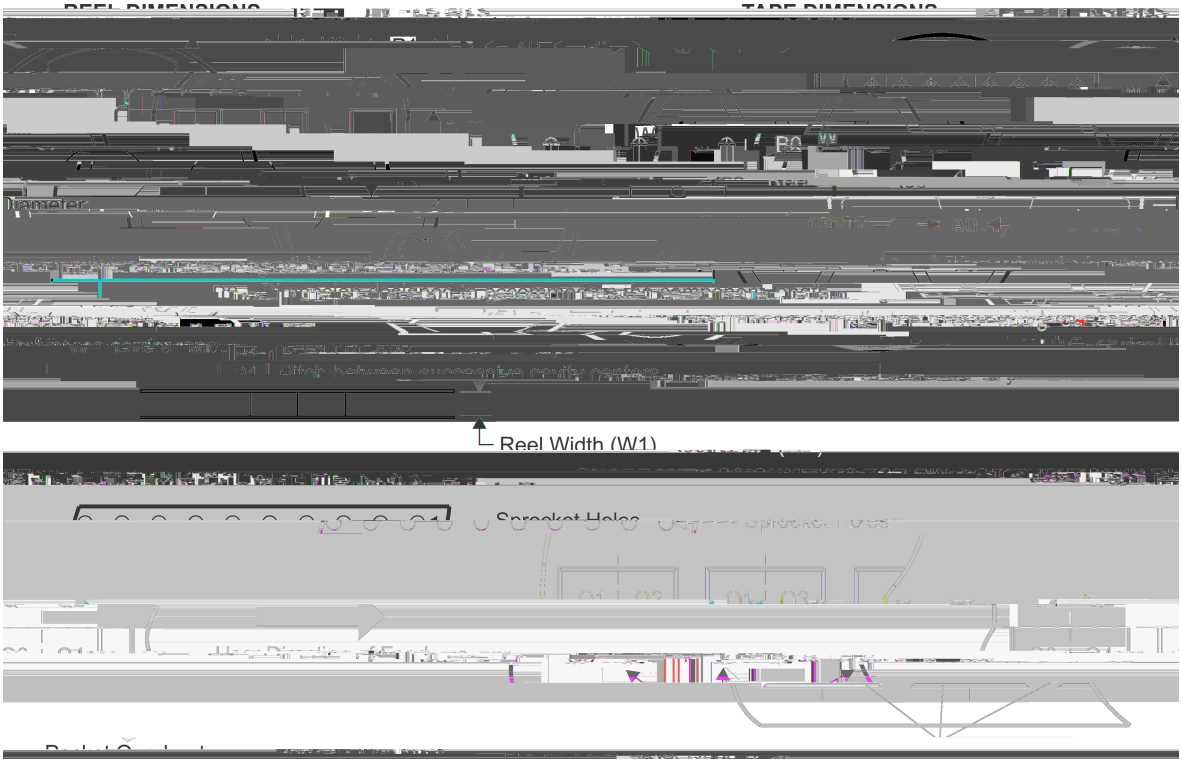
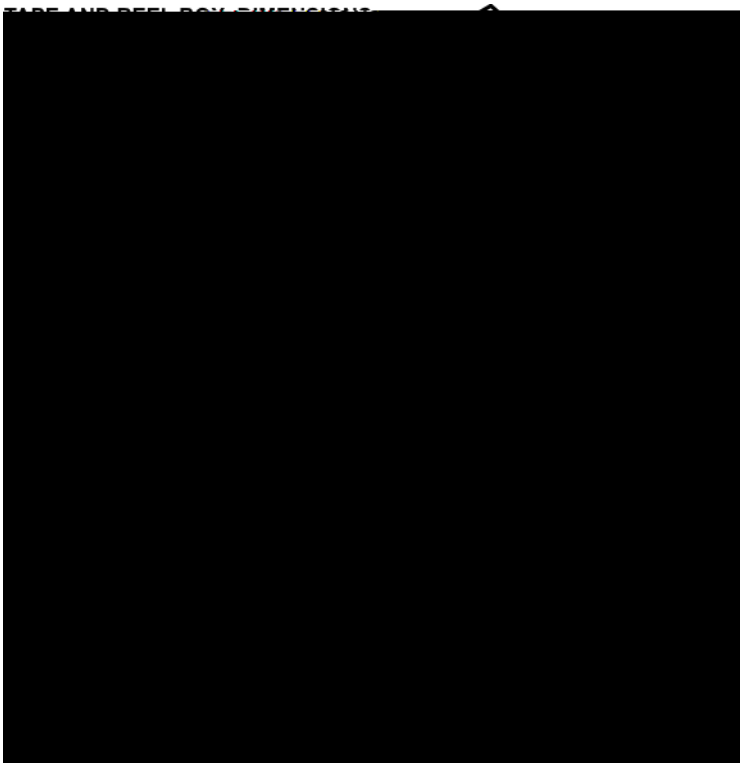


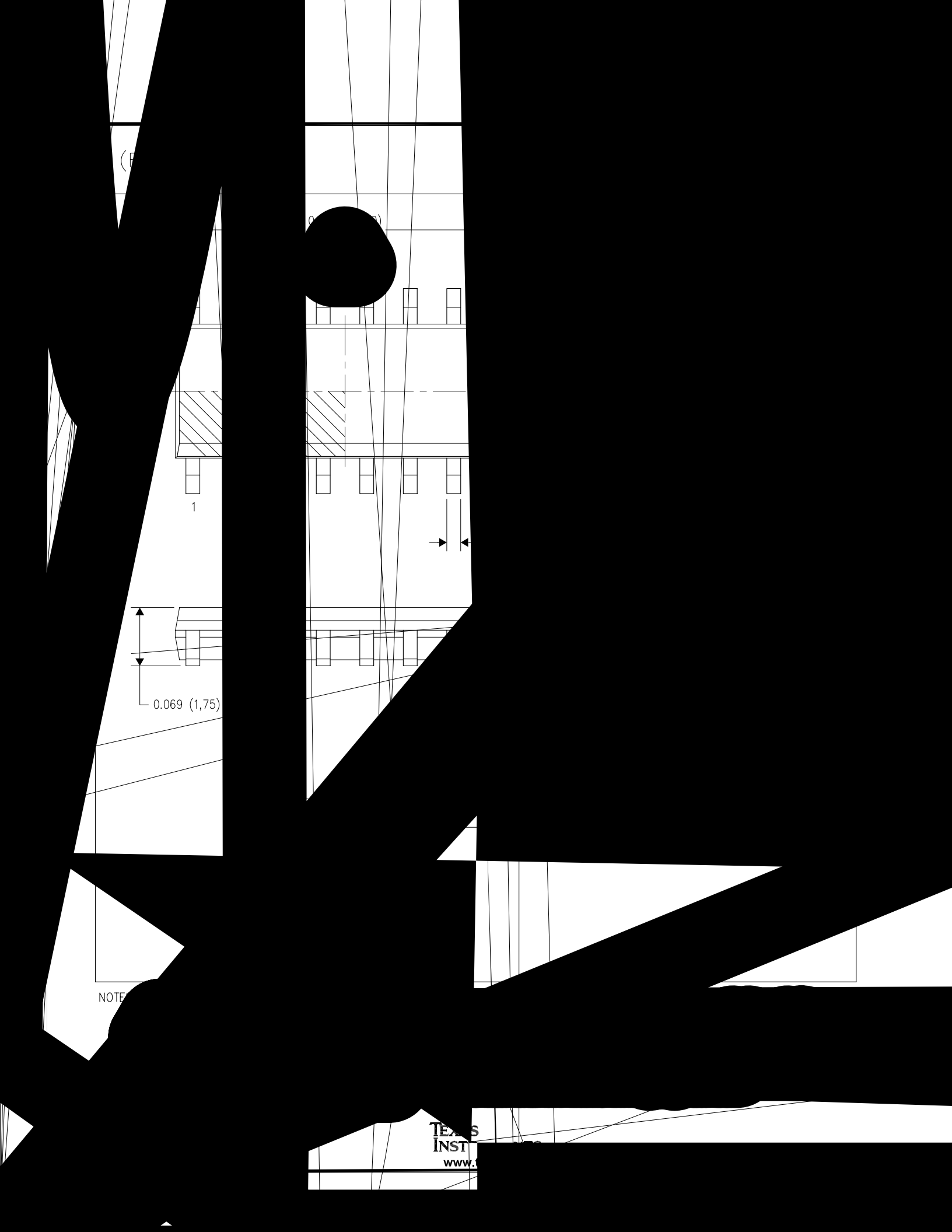
*All dimensions are nominal

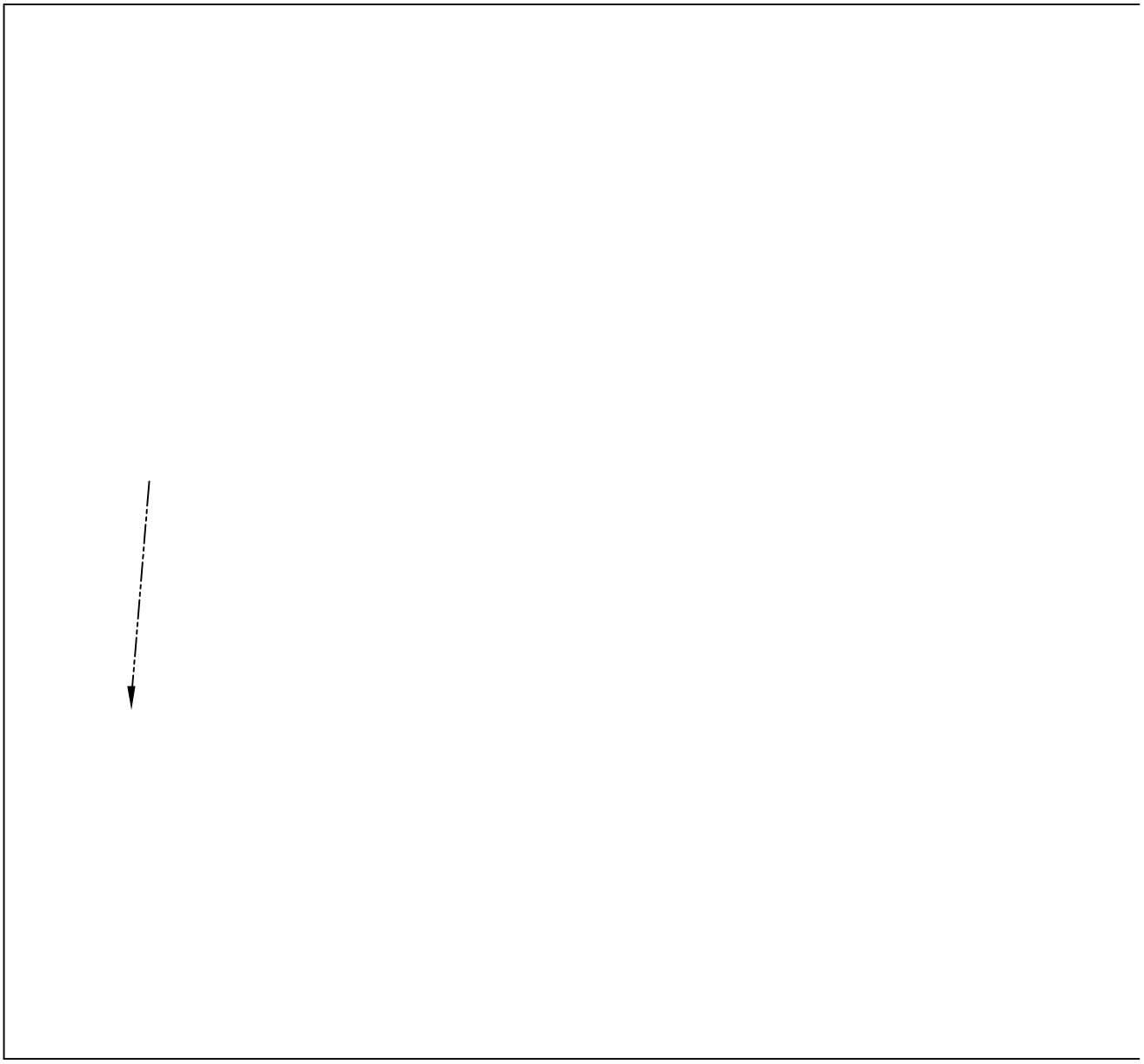
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2050HSN-A508TR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2050HSN-A508TR	SOIC	D	16	2500	367.0	367.0	38.0


1
0.069 (1,75)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.