

## Integrated 5-Port 10/100 QoS Switch

The KS8995XA is a highly integrated Layer-2 QoS switch with optimized BOM (Bill of Materials) cost for low port count, cost-sensitive 10/100Mbps switch systems. It also provides an extensive feature set including three different QoS priority schemes, dual MII interface for BOM cost reduction, programmable rate limiting to offload CPU tasks, software & hardware power-down, MDC/MDIO control interface and port monitoring to effectively address both current and emerging Fast Ethernet applications.

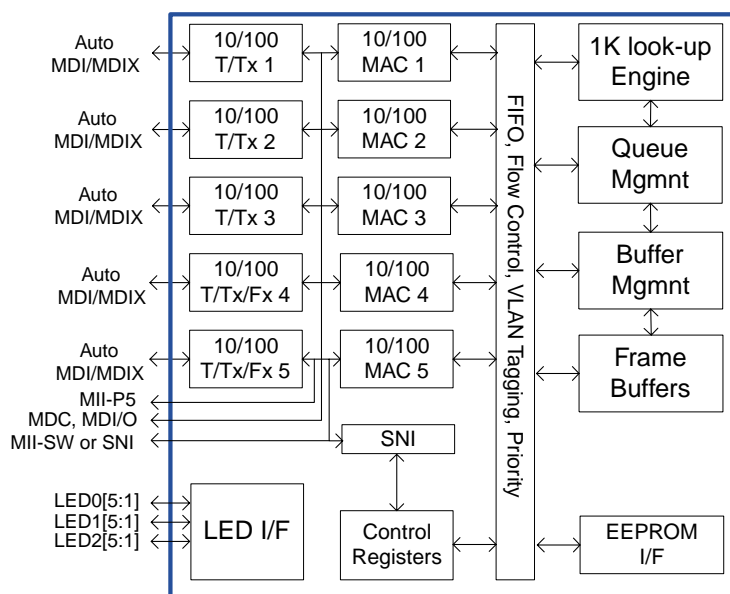
The KS8995XA contains five 10/100 transceivers with patented mixed-signal low-power technology, five MAC (Media Access Control) units, a high-speed non-blocking switch fabric, a dedicated address lookup engine, and an on-chip frame buffer memory.

All PHY units support 10Base-T and 100BaseTX. In addition, two of the PHY units support 100BaseFX (Ports 4 and 5).

### Features

- Integrated switch with five MACs and five Fast Ethernet transceivers fully compliant to IEEE 802.3u standard
- Shared memory based switch fabric with fully non-blocking configuration
- 10BaseT, 100BaseTX and 100BaseFX modes (FX in Ports 4 and 5)
- Dual MII configuration: MII-Switch (MAC or PHY mode MII) and MII-P5 (PHY mode MII)
- VLAN ID tag/untag options, per-port basis
- Programmable rate limiting, ingress and egress port, rate options for high and low priority, per port basis
- Flow control or drop packet rate limiting (ingress port)
- Broadcast storm protection with percent control – global and per-port basis
- Optimization for fiber-to-copper media conversion
- Full-chip hardware power-down support (register configuration not saved)
- Per-port based software power-save on PHY (idle link detection, register configuration preserved)

### Block Diagram



KS8995XA

## Features

- QoS/CoS packets prioritization supports: per port, 802.1p and DiffServ based
- 802.1p/q tag insertion or removal on a per port basis (egress)
- Port-based VLAN support
- MDC and MDI/O interface support to access the MII PHY control registers (not all control registers)
- MII local loopback support
- On-chip 64kB memory for frame buffering (not shared with 1K unicast address table)
- 1.4Gbps high performance memory bandwidth
- Wire-speed reception and transmission
- Integrated look-up engine with dedicated 1K unicast MAC addresses
- Automatic address learning, address aging and address migration
- Full duplex IEEE 802.3x and half-duplex back pressure flow control
- Comprehensive LED support
- 7-wire SNI support for legacy MAC interface
- Automatic MDI/MDI-X crossover for plug-and-play
- Low power, 1.8V, 2.5V or 3.3V, 0.18 $\mu$ m CMOS technology
- Available in 128-pin PQFP package

## Applications

- Broadband gateway/firewall/VPN
- Integrated DSL or cable modem multi-port router
- Wireless LAN access point plus gateway
- Home networking expansion
- Standalone 10/100 switch
- Hotel/campus/MxU gateway
- Enterprise VoIP gateway/phone
- FTTx customer premise equipment
- Media converter

# System Level Applications

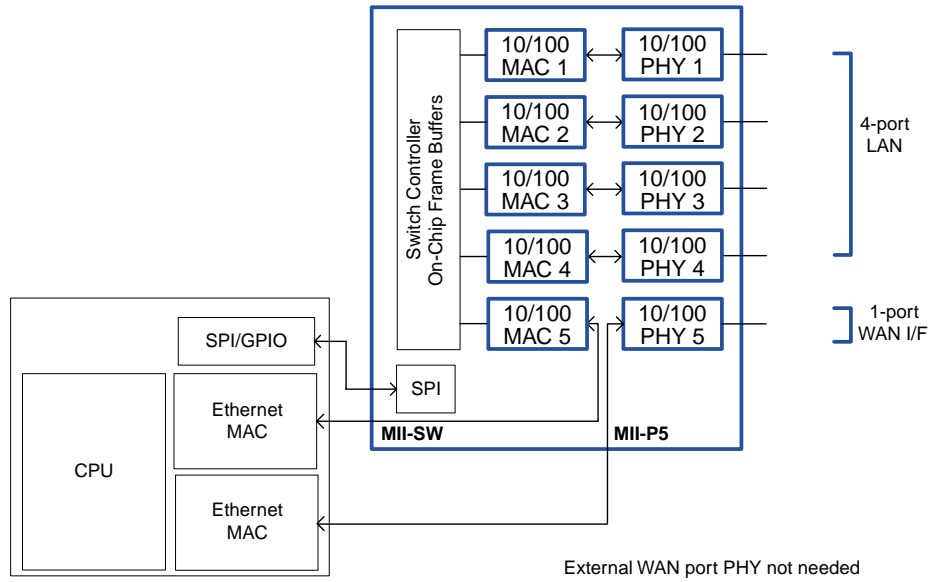


Figure 1. Broadband Gateway

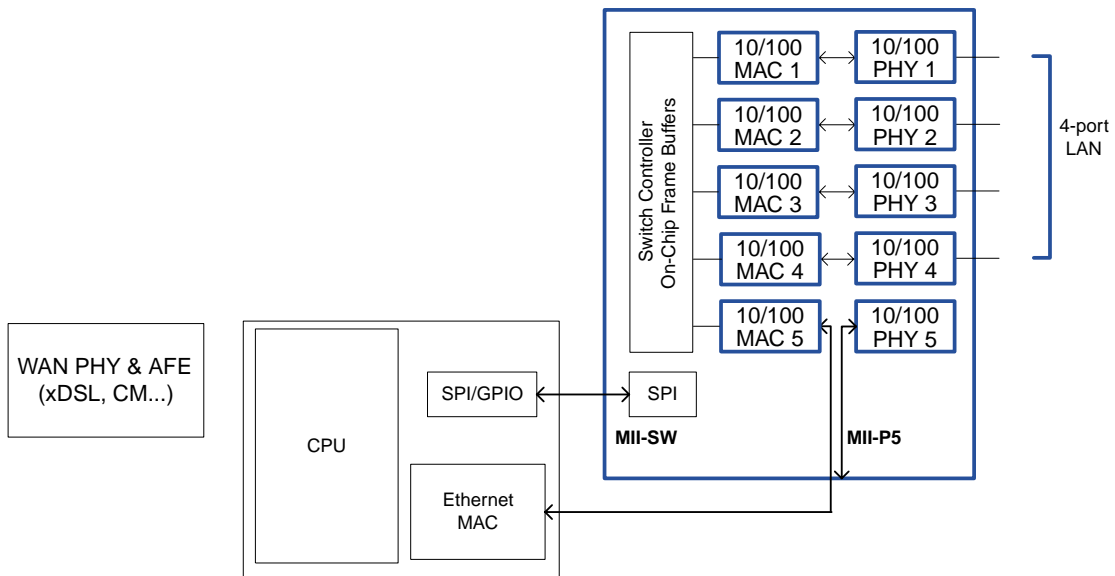


Figure 2. Integrated Broadband Router

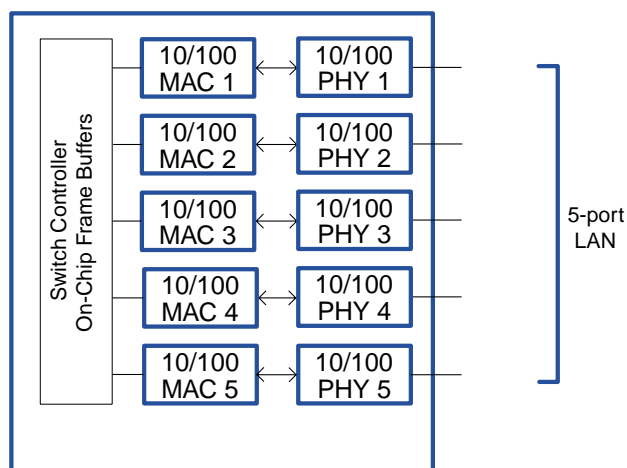


Figure 3. Standalone Switch

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