

SBS 1.1-COMPLIANT GAS GAUGE ENABLED WITH IMPEDANCE TRACK™ TECHNOLOGY FOR USE WITH THE bq29330

Check for Samples: [bq20z60-R1](#)

FEATURES

- **Next Generation Patented Impedance Track™ Technology Accurately Measures Available Charge in Li-Ion and Li-Polymer Batteries**
 - Better Than 1% Error Over the Lifetime of the Battery
- **Supports the Smart Battery Specification SBS V1.1**
- **Flexible Configuration for 2-, 3-, and 4-Series Li-Ion and Li-Polymer Cells**
- **Powerful 8-Bit RISC CPU With Ultralow Power Modes**
- **Full Array of Programmable Protection Features**
 - Voltage, Current, and Temperature
- **Satisfies JEITA Guidelines**
- **Added Flexibility to Handle More Complex Charging Profiles**
- **Lifetime Data Logging**
- **Drives 3-, 4-, or 5-Segment LED Display for Battery-Pack Conditions**
- **Supports SHA-1 Authentication**
- **Available in 30-Pin TSSOP (DBT) and 32-Pin QFN (RSM) Packages**

APPLICATIONS

- **Notebook PCs**
- **Medical and Test Equipment**
- **Portable Instrumentation**

DESCRIPTION

The bq20z60-R1 SBS-compliant gas gauge and protection IC, incorporating patented Impedance Track™ technology, is designed for battery-pack or in-system installation. The bq20z60-R1 measures and maintains an accurate record of available charge in Li-Ion or Li-Polymer batteries, using its integrated high-performance analog peripherals. The bq20z60-R1 monitors capacity change, battery impedance, open-circuit voltage, and other critical parameters of the battery pack, which reports the information to the system host controller over a serial-communication bus. It is designed to work with the bq29330 analog front-end (AFE) protection IC to maximize functionality and safety, while minimizing external component count and cost in smart battery circuits.

The Impedance Track™ technology continuously analyzes the battery impedance, resulting in superior gas-gauging accuracy. This enables the remaining capacity to be calculated with discharge rate, temperature, and cell aging, which are all accounted for during each stage of every cycle with high accuracy.

Table 1. AVAILABLE OPTIONS

T _A	PACKAGE			
	30-PIN TSSOP (DBT) Tube	30-PIN TSSOP (DBT) Tape & Reel	32-PIN QFN (RSM) Tube	32-PIN QFN (RSM) Tape & Reel
–40°C to 85°C	bq20z60-R1DBT ⁽¹⁾	bq20z60-R1DBTR ⁽²⁾	bq20z60-R1RSM ⁽¹⁾	bq20z60-R1RSMR ⁽²⁾

(1) A single tube quantity is 60 units.

(2) A single reel quantity is 2000 units.



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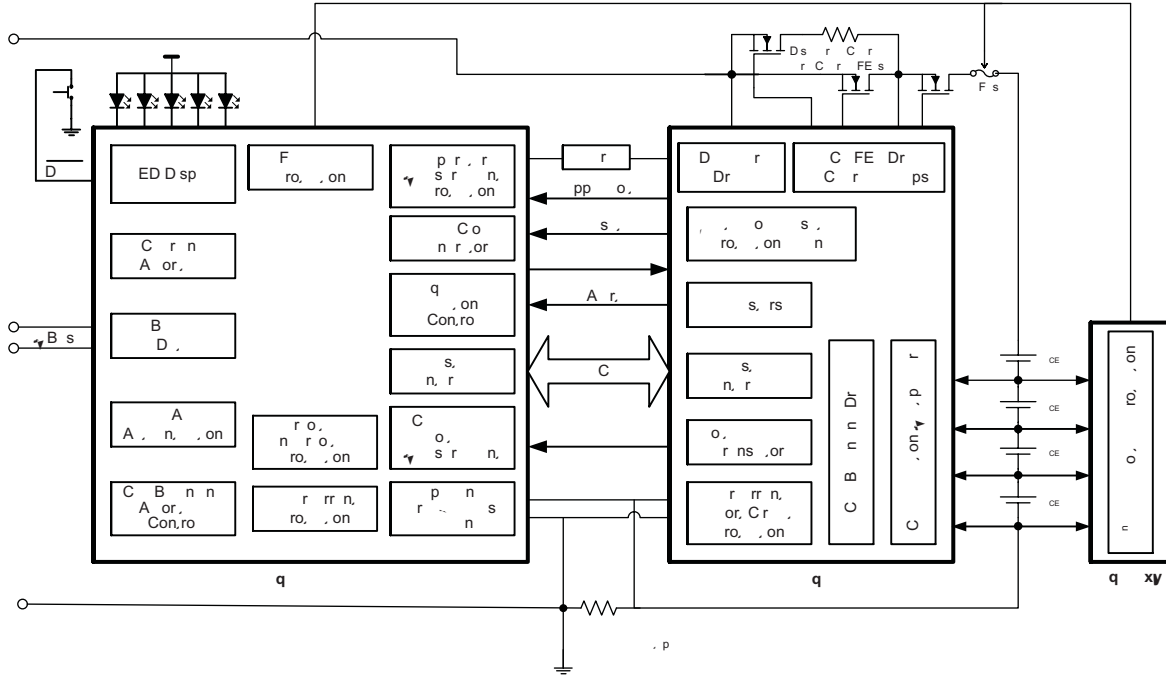
Impedance Track is a trademark of Texas Instruments.

THERMAL INFORMATION

THERMAL METRIC ⁽¹⁾		bq20z60-R1		UNITS
		TSSOP (DBT)	QFN (RSM)	
		30 PINS	32 PINS	
$\theta_{JA, \text{ High K}}$	Junction-to-ambient thermal resistance ⁽²⁾	81.4	37.4	°C/W
$\theta_{JC(\text{top})}$	Junction-to-case(top) thermal resistance ⁽³⁾	16.2	30.6	
θ_{JB}	Junction-to-board thermal resistance ⁽⁴⁾	34.1	7.7	
ψ_{JT}	Junction-to-top characterization parameter ⁽⁵⁾	0.4	0.4	
ψ_{JB}	Junction-to-board characterization parameter ⁽⁶⁾	33.6	7.5	
$\theta_{JC(\text{bottom})}$	Junction-to-case(bottom) thermal resistance ⁽⁷⁾	N/A	2.6	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).
- (2) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, high-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (3) The junction-to-case (top) thermal resistance is obtained by simulating a cold plate test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (4) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold plate fixture to control the PCB temperature, as described in JESD51-8.
- (5) The junction-to-top characterization parameter, ψ_{JT} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (6) The junction-to-board characterization parameter, ψ_{JB} , estimates the junction temperature of a device in a real system and is extracted from the simulation data for obtaining θ_{JA} , using a procedure described in JESD51-2a (sections 6 and 7).
- (7) The junction-to-case (bottom) thermal resistance is obtained by simulating a cold plate test on the exposed (power) pad. No specific JEDEC standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.

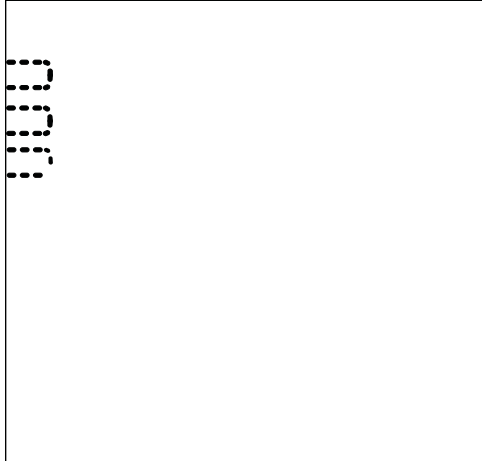
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled at temperatures below 30°C. Electrostatic discharge (ESD) damage to the device can occur if proper ESD precautions are not taken before and after the device is handled and mounted on a printed circuit board.



- | | | | | |
|------|--------------------------|---|-------------------------------------|--------------------------|
| NC | <input type="checkbox"/> | 1 | <input checked="" type="checkbox"/> | <input type="checkbox"/> |
| | <input type="checkbox"/> | 2 | <input type="checkbox"/> | <input type="checkbox"/> |
| | <input type="checkbox"/> | 3 | <input type="checkbox"/> | <input type="checkbox"/> |
| SCLK | <input type="checkbox"/> | 4 | <input type="checkbox"/> | <input type="checkbox"/> |
| | <input type="checkbox"/> | 5 | <input type="checkbox"/> | <input type="checkbox"/> |
| | <input type="checkbox"/> | | <input type="checkbox"/> | <input type="checkbox"/> |
| TS2 | | | | MRST |
| PRES | | | | |

QFN (RSM) PIN FUNCTIONS

QFN (RSM)
(TOP VIEW)

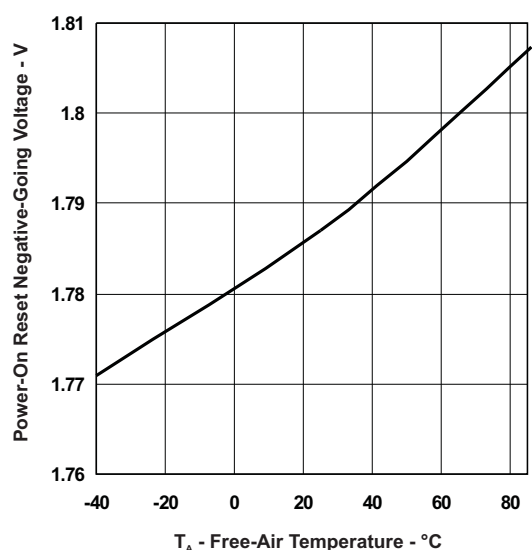


QFN (RSM) PIN CONFIGURATIONS

PIN		I/O ⁽¹⁾	DESCRIPTION
NO.	NAME		
1	NC	—	Not used—leave

TS2

POWER ON RESET BEHAVIOR
VS
FREE-AIR TEMPERATURE



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SCLR,

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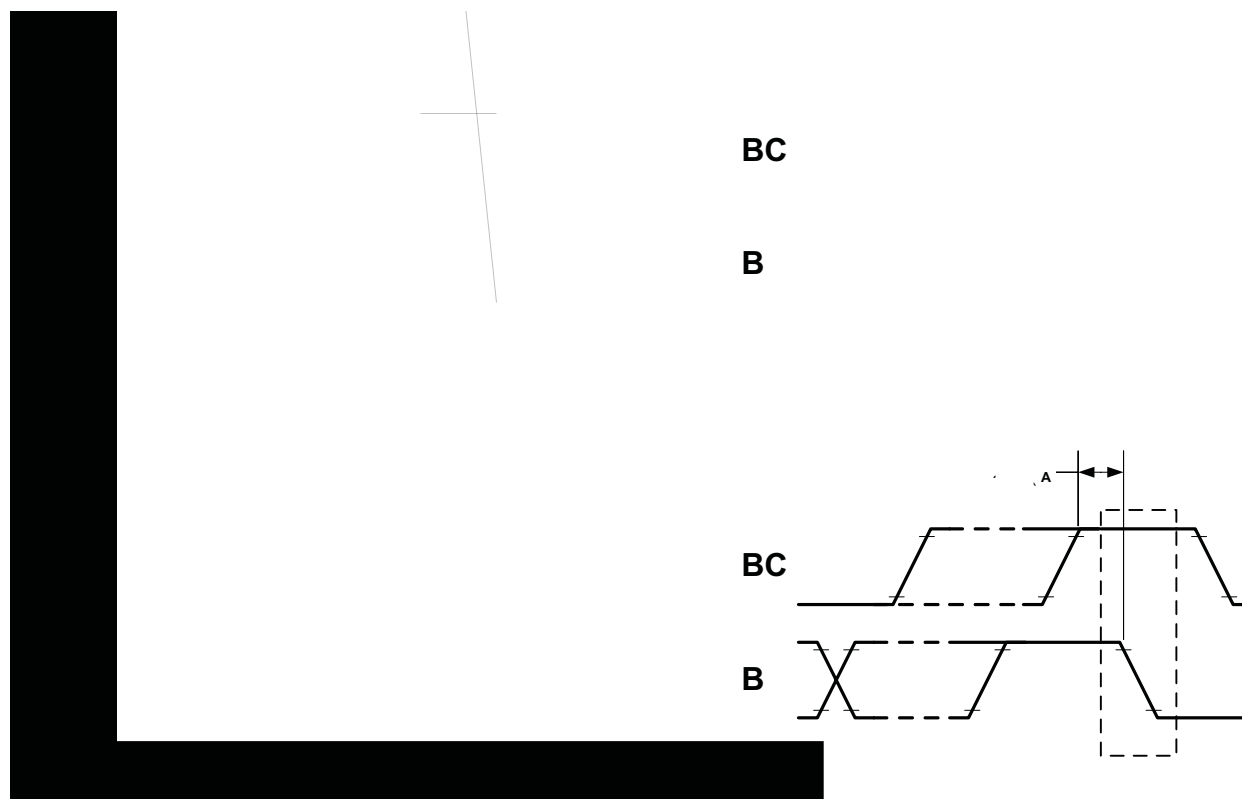
SMBus TIMING SPECIFICATIONS (continued)

V_{CC} = 2.4 V to 2.6 V, T_A = -40°C to 85°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t _{LOW}	Clock low period		4.7			μs
t _{HIGH}	Clock high period	See ⁽²⁾	4		50	
t _{LOW:SEXT}	Cumulative clock low slave extend time	See ⁽³⁾			25	ms
t _{LOW:MEXT}	Cumulative clock low master extend time	See ⁽⁴⁾			10	
t _F	Clock/data fall time	(V _{ILMAX} - 0.15 V) to (V _{IHMIN} + 0.15 V)			300	ns
t _R	Clock/data rise time	0.9 V _{CC} to (V _{ILMAX} - 0.15 V)			1000	

- (2) t_{HIGH:MAX} is minimum bus idle time. SMBC = 1 for t > 50 μs causes reset of any transaction involving the bq20z60-R1 that is in progress.
- (3) t_{LOW:SEXT} is the cumulative time a slave device is allowed to extend the clock cycles in one message from initial start to the stop.
- (4) t_{LOW:MEXT} is the cumulative time a master device is allowed to extend the clock cycles in one message from initial start to the stop.

SMBus TIMING DIAGRAM



A. SCLKACK is the acknowledge related clock pulse generated by the master.

FEATURE SET

Primary (1st Level) Safety Features

The bq20z60-R1 supports a wide range of battery and system protection features that can easily be configured. The primary safety features include:

- Cell over/undervoltage protection
- Charge and discharge overcurrent
- Short circuit protection
- Charge and discharge overtemperature with independent alarms and thresholds for each thermistor
- AFE Watchdog

Secondary (2nd Level) Safety Features

The secondary safety features of the bq20z60-R1 can be used to indicate more serious faults via the SAFE pin. This pin can be used to blow an in-line fuse to permanently disable the battery pack from charging or discharging. The secondary safety protection features include:

- Safety overvoltage
- Safety undervoltage
- 2nd level protection IC input
- Safety over current in charge and discharge
- Safety overtemperature in charge and discharge with independent alarms and thresholds for each thermistor
- Charge FET and zero-volt Charge FET fault
- Discharge FET fault
- Cell imbalance detection (active and at rest)
- Open thermistor detection
- AFE communication fault

Charge Control Features

The bq20z60-R1 charge control features include:

- Supports JEITA temperature ranges. Reports charging voltage and charging current according to the active temperature range
- Handles more complex charging profiles. Allows for splitting the standard temperature range into two sub-ranges and allows for varying the charging current according to the cell voltage.
- Reports the appropriate charging current needed for constant current charging and the appropriate charging voltage needed for constant voltage charging to a smart charger using SMBus broadcasts
- Determines the chemical state of charge of each battery cell using Impedance Track, and reduces the charge difference of the battery cells in fully charged state of the battery pack, gradually using the cell balancing algorithm during charging. This prevents fully charged cells from overcharging and causing excessive degradation, and also increases the usable pack energy by preventing premature charge termination.
- Supports pre-charging/zero-volt charging
- Supports charge inhibit and charge suspend if battery pack temperature is out of temperature range
- Reports charging fault and also indicate charge status via charge and discharge alarms

Gas Gauging

The bq20z60-R1 uses the Impedance Track technology to measure and calculate the available charge in battery cells. The achievable accuracy is better than 1% error over the lifetime of the battery and there is no full charge discharge learning cycle required.

See *Theory and Implementation of Impedance Track Battery Fuel-Gauging Algorithm* application note ([SLUA364](#)) for further details.

Lifetime Data Logging Features

The bq20z60-R1 offers lifetime data logging, where important measurements are stored for warranty and analysis purposes. The data monitored includes:

- Lifetime maximum temperature
- Lifetime maximum temperature count
- Lifetime maximum temperature duration
- Lifetime minimum temperature
- Lifetime maximum battery cell voltage
- Lifetime maximum battery cell voltage count
- Lifetime maximum battery cell voltage duration
- Lifetime minimum battery cell voltage
- Lifetime maximum battery pack voltage
- Lifetime minimum battery pack voltage
- Lifetime maximum charge current
- Lifetime maximum discharge current
- Lifetime maximum charge power
- Lifetime maximum discharge power
- Lifetime maximum average discharge current
- Lifetime maximum average discharge power
- Lifetime average temperature

Authentication

The bq20z60-R1 supports authentication by the host using SHA-1.

Power Modes

The bq20z60-R1 supports three separate power modes to reduce power consumption:

- In Normal Mode, the bq20z60-R1 performs measurements, calculations, protection decisions, and data updates in 1-s intervals. Between these intervals, the bq20z60-R1 is in a reduced power stage.
- In Sleep Mode, the bq20z60-R1 performs measurements, calculations, protection decisions, and data updates in adjustable time intervals. Between these intervals, the bq20z60-R1 is in a reduced power stage. The bq20z60-R1 has a wake function that enables exit from Sleep mode when current flow or failure is detected.
- In Shutdown Mode, the bq20z60-R1 is completely disabled.

CONFIGURATION

Oscillator Function

The bq20z60-R1 fully integrates the system oscillators; therefore, no external components are required for this feature.

System Present Operation

The bq20z60-R1 periodically verifies the $\overline{\text{PRES}}$ pin and detects that the battery is present in the system via a low state on a $\overline{\text{PRES}}$ input. When this occurs, the bq20z60-R1 enters normal operating mode. When the pack is removed from the system and the $\overline{\text{PRES}}$ input is high, the bq20z60-R1 enters the battery-removed state, disabling the charge, discharge, and ZVCHG FETs. The $\overline{\text{PRES}}$ input is ignored and can be left floating when non-removal mode is set in the data flash.

bq20z60-R1

SLUS991A – DECEMBER 2009 – REVISED MARCH 2011

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BATTERY PARAMETER MEASUREMENTS

The bq20z60-R1 uses an integrating delta-sigma analog-to-digital converter (ADC) for current measurement, and a second delta-sigma ADC for individual cell and battery voltage and temperature measurement.

Charge and Discharge Counting

The integrating delta-sigma ADC measures the charge/discharge flow of the battery by measuring the voltage drop across a small-value sense resistor between the SRP and SRN pins. The integrating ADC measures bipolar signals from -0.25 V to 0.25 V . The bq20z60-R1 detects charge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is positive and discharge activity when $V_{SR} = V_{(SRP)} - V_{(SRN)}$ is negative. The bq20z60-R1 continuously integrates the signal over time, using an internal counter. The fundamental rate of the counter is 0.65 nVh .

Voltage

The bq20z60-R1 updates the individual series cell voltages through the bq29330 at 1-s intervals. The bq20z60-R1 configures the bq29330 to connect the selected cell, cell offset, or bq29330 VREF to the CELL pin of the bq29330, which is required to be connected to VIN of the bq20z60-R1. The internal ADC of the bq20z60-R1 measures the voltage, scales it, and calibrates itself appropriately. This data is also used to calculate the impedance of the cell for the Impedance Track gas-gauging.

Current

The bq20z60-R1 uses the SRP and SRN inputs to measure and calculate the battery charge and discharge current using a $5\text{-m}\Omega$ to $20\text{-m}\Omega$ typ. sense resistor.

Wake Function

The bq20z60-R1 can exit sleep mode, if enabled, by the presence of a programmable level of current signal across SRP and SRN.

Auto Calibration

The bq20z60-R1 provides an auto-calibration feature to cancel the voltage offset error across SRP and SRN for maximum charge measurement accuracy. The bq20z60-R1 performs auto-calibration when the SMBus lines a

cancel

APPLICATION SCHEMATIC



REVISION HISTORY

Changes from Original (December 2009) to Revision A	Page
• Added the 32-pin QFN (RSM) package	1

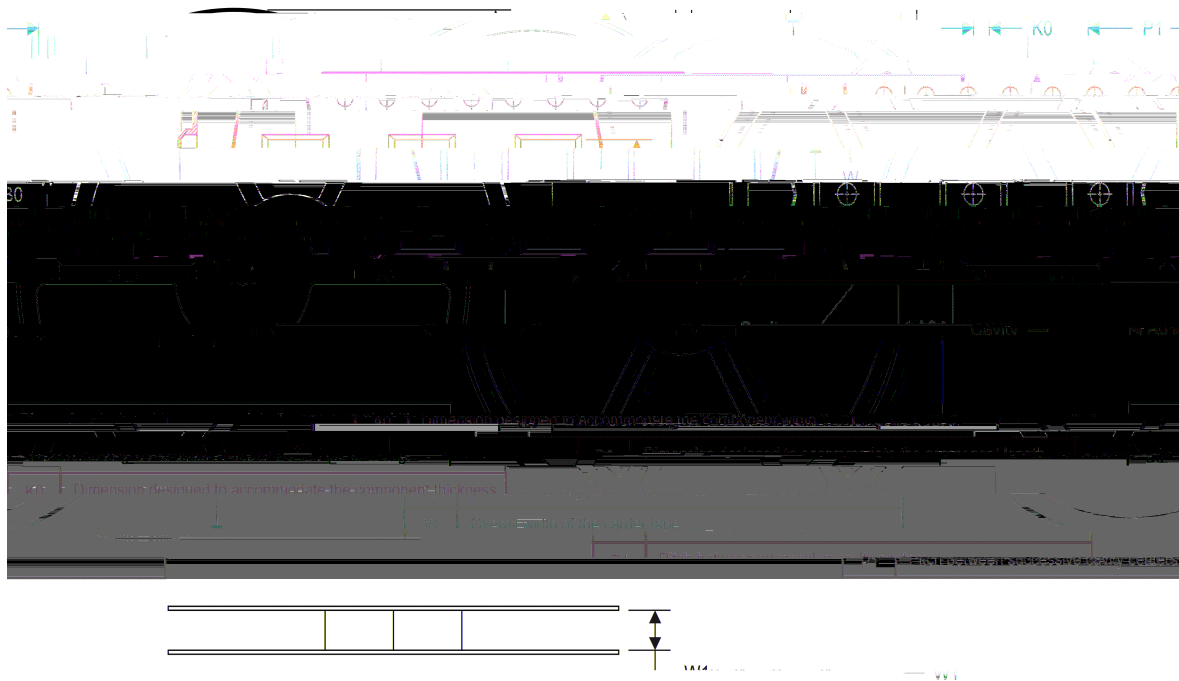
PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing
			Type.i8.9.09.1 0 0 1 267.48vice

TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS



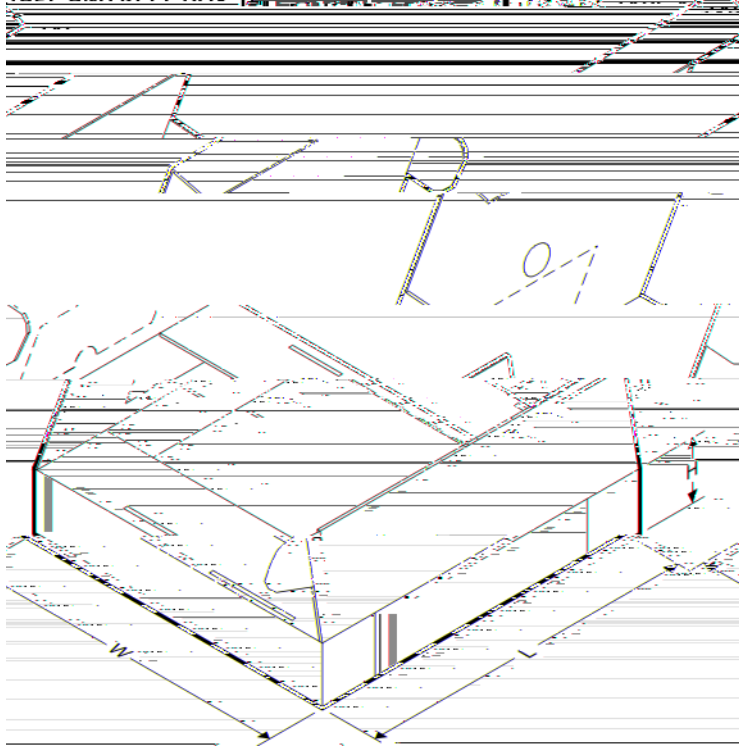
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device

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TAPE AND REEL ROY DIMENSIONS

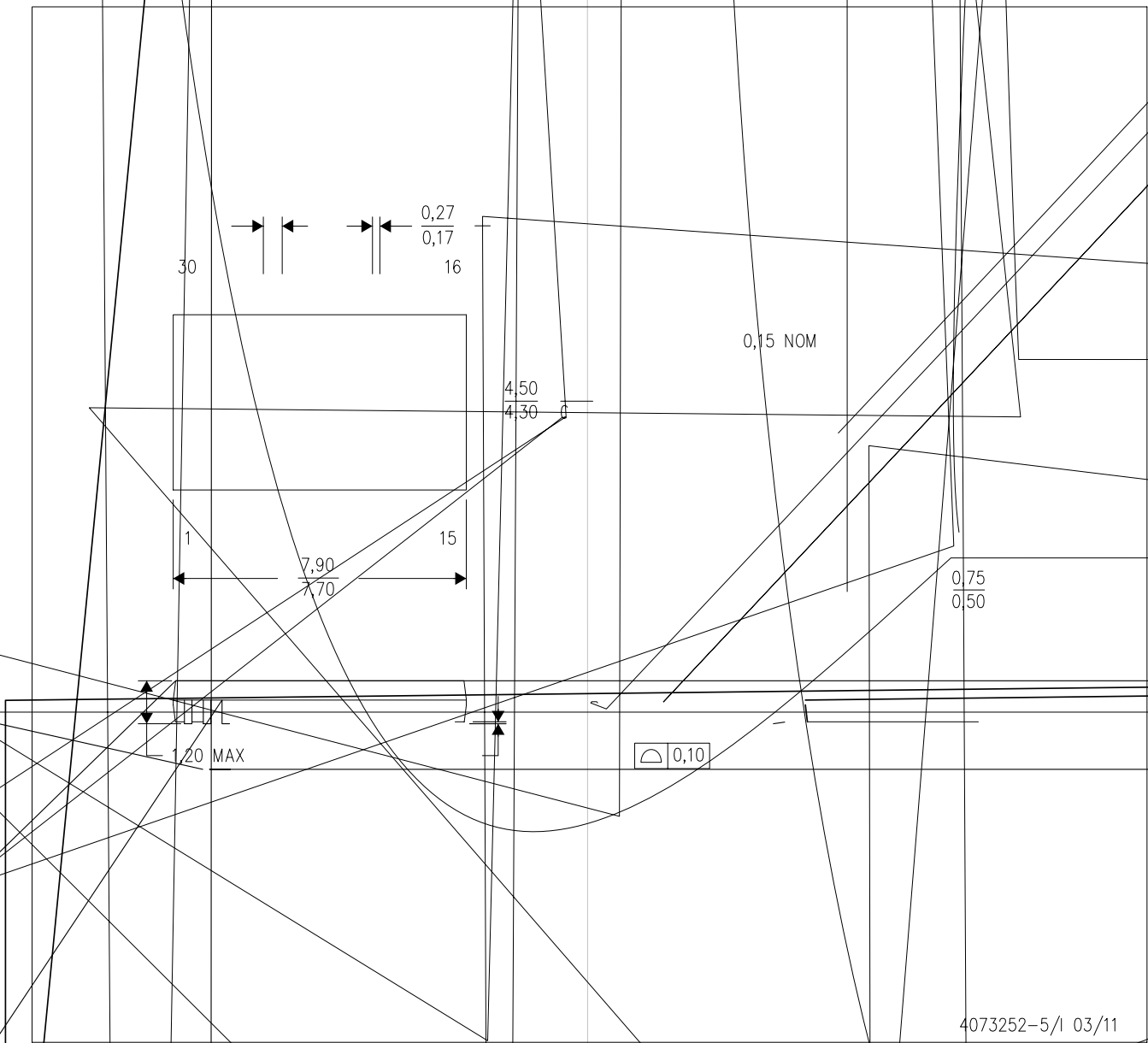


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ20Z60DBTR-R1	TSSOP	DBT	30	2000	367.0	367.0	38.0

DBT (R-PDSO-G30)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.
C. All dimensions do not include mold flash or protrusion.

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