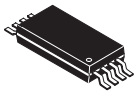


SLUS509A − DECEMBER 2001 − REVISED NOVEMBER 2004

HIGH-PERFORMANCE BATTERY MONITOR WITH COLOUMB COUNTER AND FLASH MEMORY

FEATURES

- **Multifunction Monitoring Device Designed to Work With an Intelligent Host Controller**
  - **Provides State of Charge Information for Rechargeable Batteries**
  - **Enhances Charge Termination**
- **High Accuracy Coulometric Charge and Discharge Current Integration With Automatic Offset Compensation**
- **Differential Current Sense**
- **32 Bytes of General-Purpose RAM**
- **96 Bytes of Flash (Including 32 Bytes of Shadow Flash)**
- **8 Bytes of ID ROM**
- **Internal Temperature Sensor Eliminates Need for External Thermistor**
- **Multifunction Digital Output Port**
- **High-Accuracy Internal Timebase Eliminates External Crystal Oscillator**
- **Low Power Consumption**
  - **Operating : <95 μA**
  - **Sleep: <2 μA**
- **Single-Wire HDQ Serial Interface**
- **8-Lead TSSOP Package**

DESCRIPTION

The bq26200 is an advanced battery monitoring IC designed to accurately measure the charge and discharge currents in rechargeable battery packs. Intended for pack integration, the bq26200 contains all the necessary functions to form the basis of a comprehensive battery capacity management system in portable applications such as cellular phones, PDA's, or other portable products.

The bq26200 works with the host controller in the portable system to implement the battery management system. The host controller is responsible for interpreting the bq26200 data and communicating meaningful battery data to the end-user or power management system.

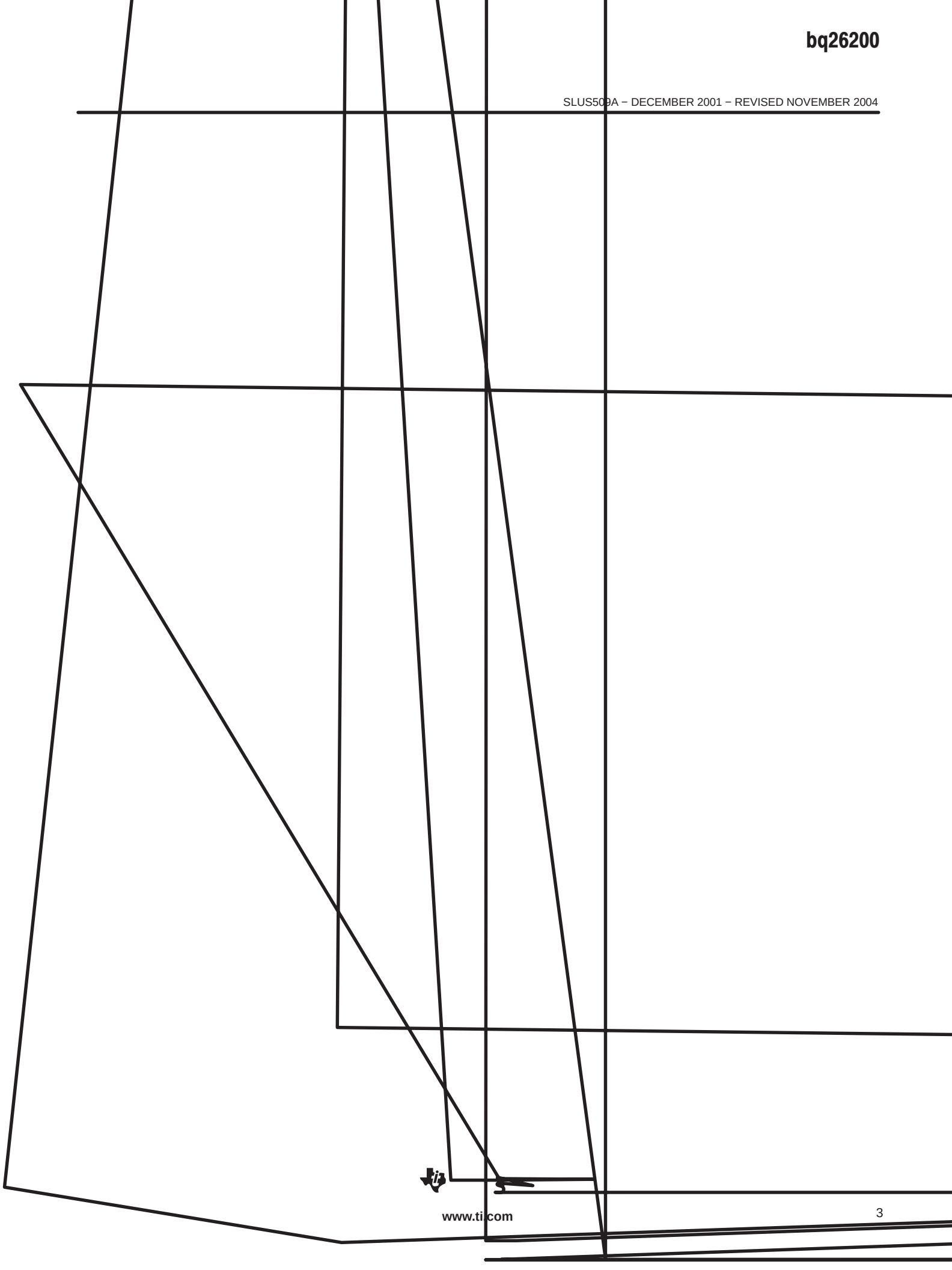
The bq26200 provides 64 bytes of general-purpose flash memory, 8 bytes of ID ROM and 32 bytes of flash backed RAM for data storage. The non-volatile memory can maintain formatted battery monitor information, identification codes, warranty information, or other critical battery parameters during periods when the battery is temporarily shorted or deeply discharged.

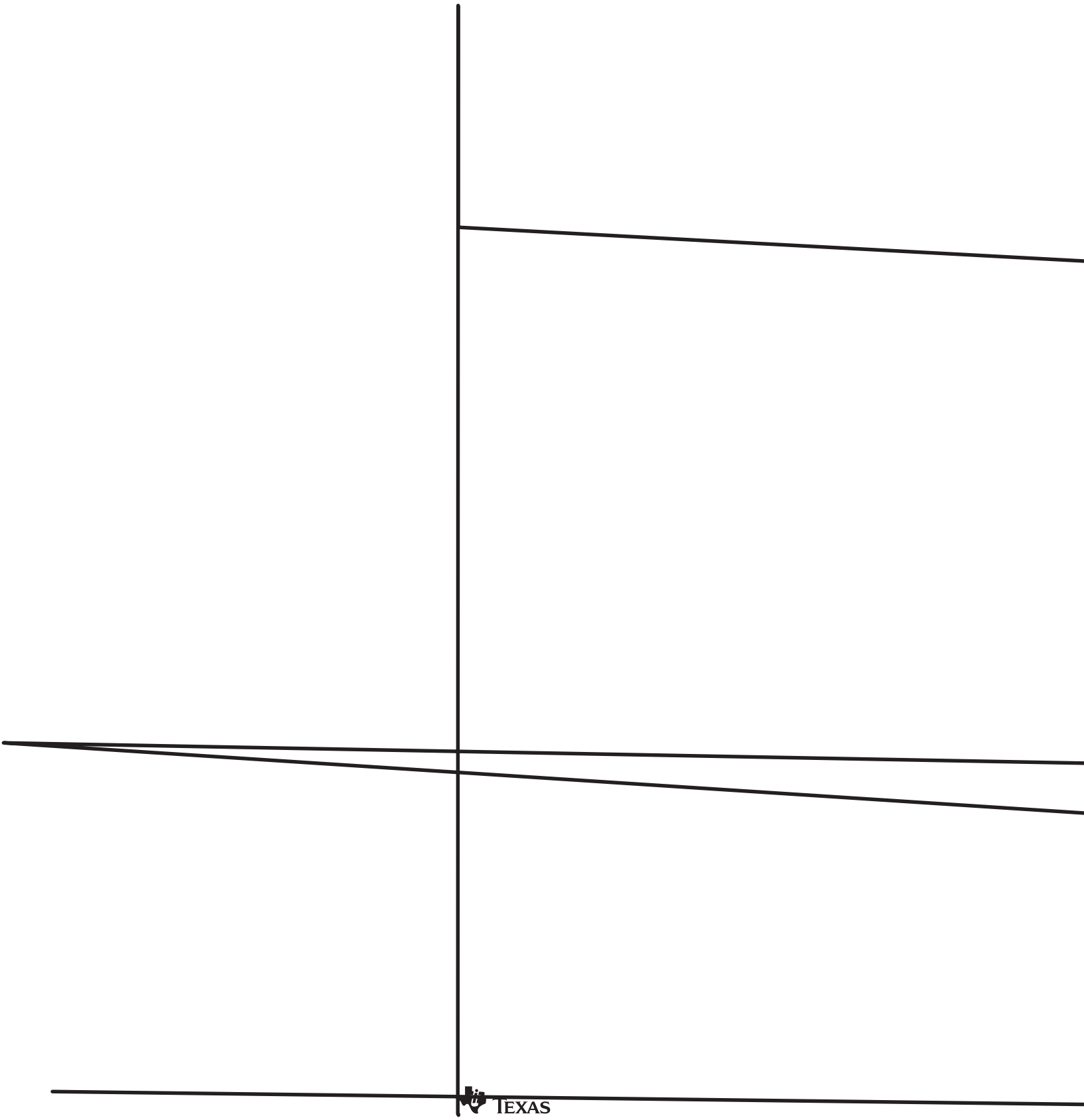
PW PACKAGE
(TOP VIEW)

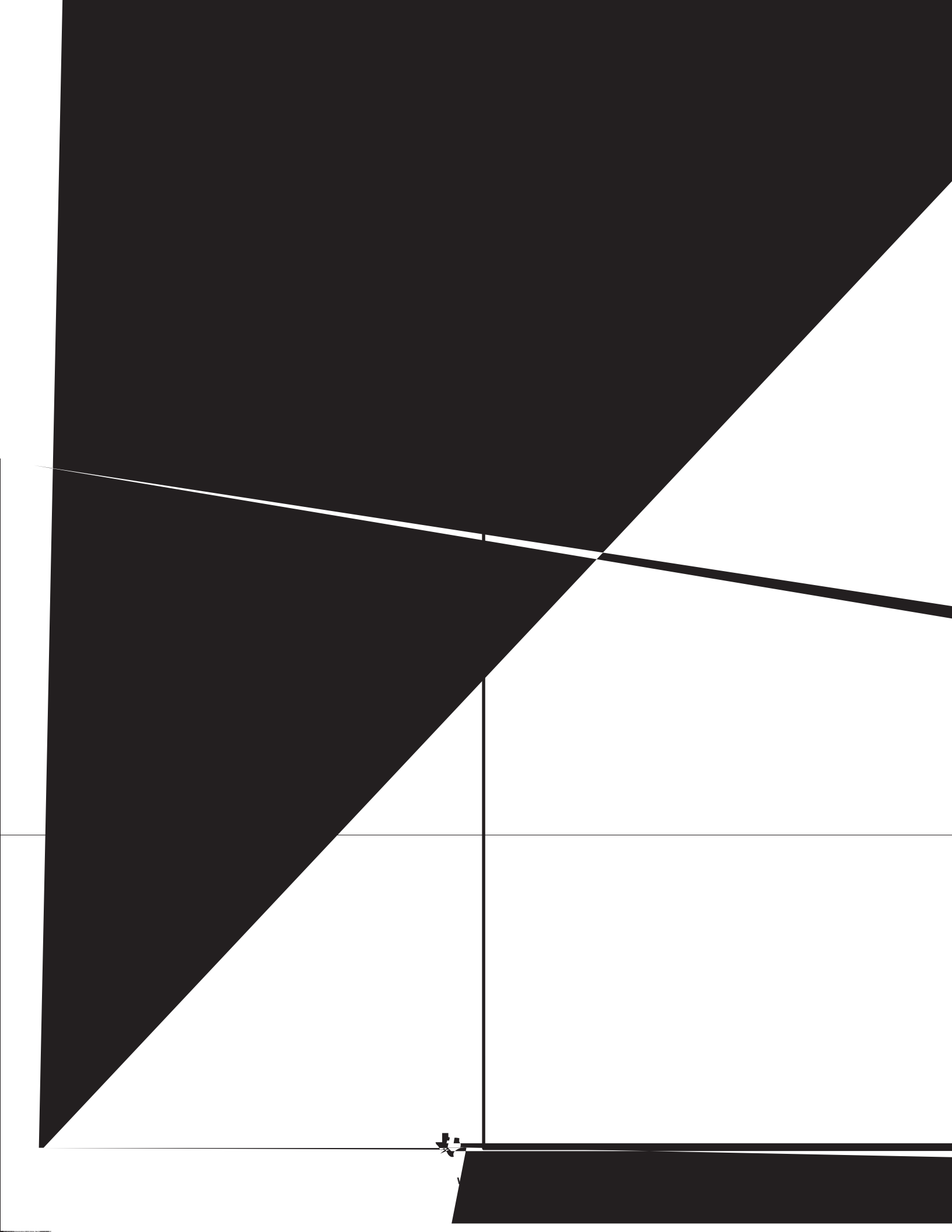
AVAILABLE OPTIONS

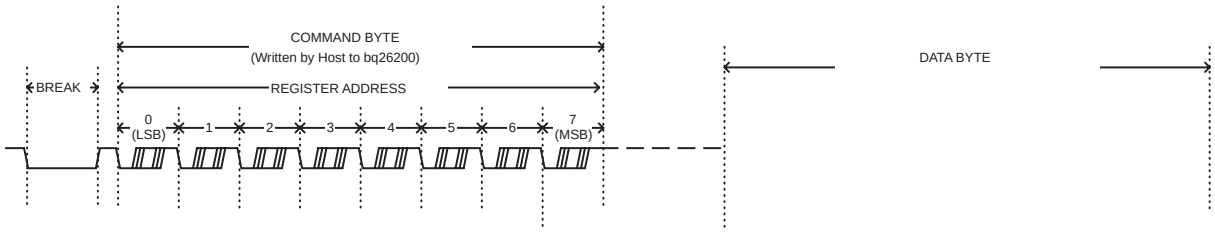
T_A	MARKING	PACKAGE
		TSSOP (PW)
−20°C to 70°C	bq262	bq26200PW

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

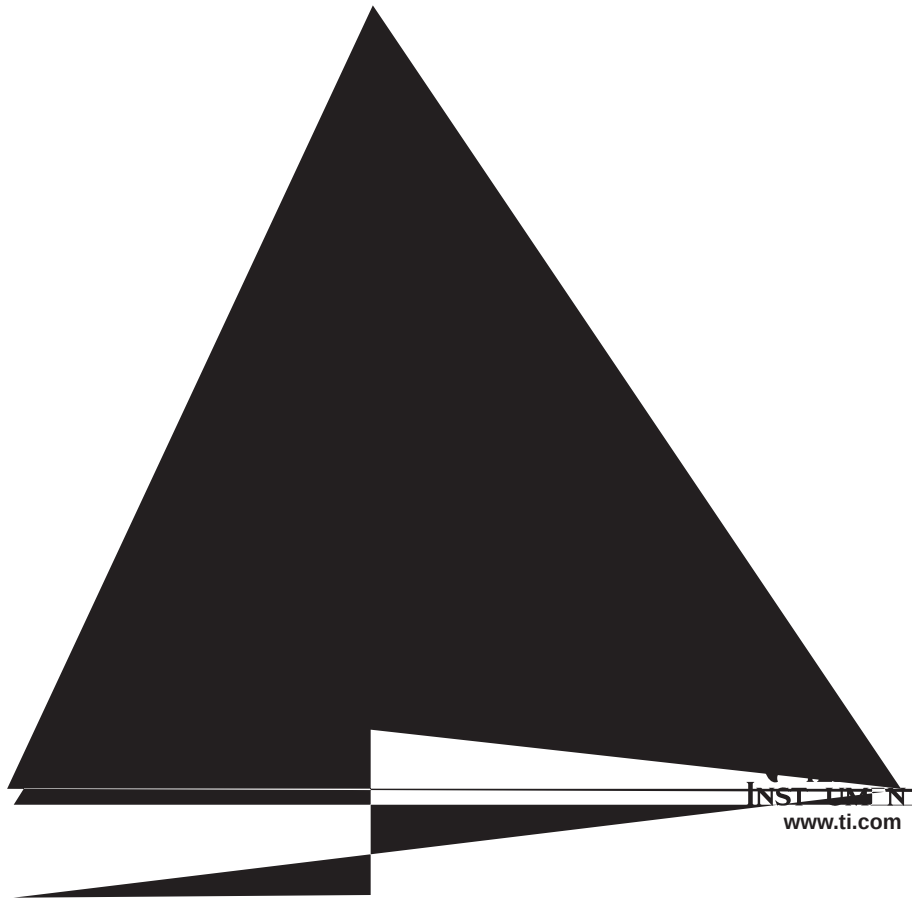







COMMAND BYTE
(Written by Host to bq26200)
DATA BYTE
BREAK
REGISTER ADDRESS
0
(LSB)
1
2
3
4
5
6
7
(MSB)

UDG−01150



APPLICATION INFORMATION

sleep mode operation

The bq26200 begins low-power operation in response to the host issuing the sleep command. Before entering the low-power state, the host processor writes the command to transfer the registers to flash. After the sleep command is sent and the charge/discharge activity is less than the value indicated by the WOE bits shown in Table 3, the chip clock is powered down and data acquisition functions cease except for self-discharge detection. During device sleep the bq26200 periodically wakes briefly to maintain the self-discharge registers. The bq26200 wakes on either a low-to-high or high-to-low transition on the HDQ pin.

Table 2. Operational States

MODE	ACTIVE REGISTERS
Normal	CCR, DCR, CTC, DTC, SDR
Sleep	SDR

Table 3. WOE Thresholds

$WOE_{3–1}$ (HEX)	V_{WOE} (mV)
0h	n/a
1h	3.516
2h	1.758
3h	1.172
4h	0.879
5h	0.703
6h	0.586
7h*	0.502

current sense offset calibration and compensation

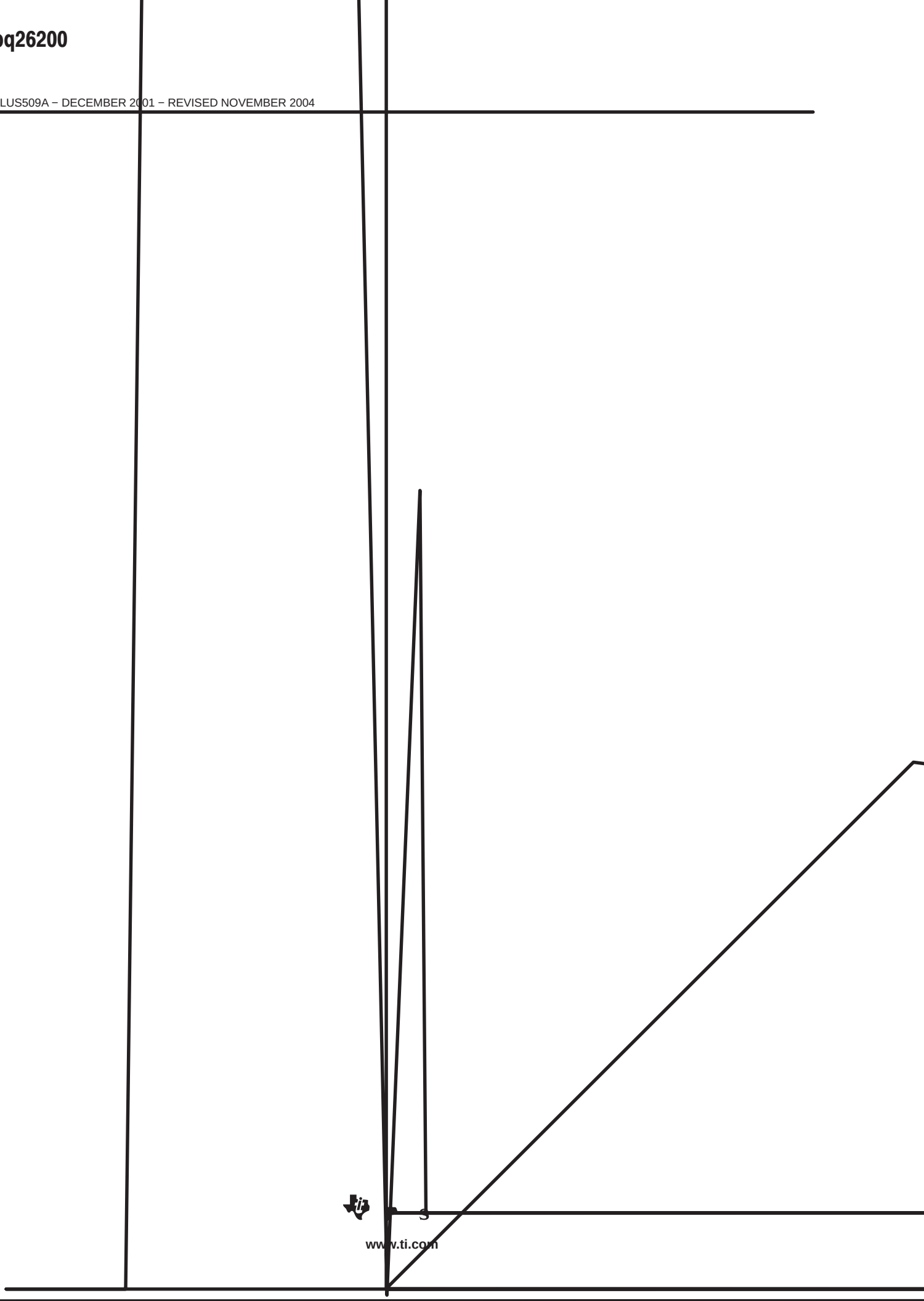
The bq26200 automatically and continuously compensates for $V_{(SRP)} - V_{(SRN))}$ offset. No host calibration or compensation is required.

gas gauge control registers

The host maintains the charge and discharge and the self-discharge count registers (CCR, CTC, DCR, DTC, and SCR). To facilitate this maintenance, the bq26200 CLR register resets the specific counter or register pair to zero. The host system clears a register by writing the corresponding register bit to 1. When the bq26200 completes the reset, the corresponding bit in the CLR register is automatically reset to 0. Clearing the DTC or CTC registers clears the MODE register bits STC/STD and sets the CTC/DTC count rates to the default value of 1.138 counts per second.

device temperature measurement

The bq26200 reports die temperature in units of ºK through register pair TMPH-TMPL. Refer to the TMP register description for more details.



APPLICATION INFORMATION

memory

ID ROM

The bq26200 has 8 bytes of ID ROM. This data field is factory programmed with a unique serial number. Please contact your Texas Instruments representative for details.

flash-shadowed RAM

The host system has direct access to read and modify 32 bytes of RAM. These 32 bytes are shadowed by 32 bytes of flash to provide non-volatile storage of battery conditions. The information stored in RAM is transferred to flash, and the information stored in flash is transferred to RAM by writing a single command into the flash command register (FCMD). When a power-on-reset occurs, PAGE0 of flash is transferred to RAM. For more details, refer to the *flash command register* section.

user-flash memory

In addition to the flash-shadowed RAM, the bq26200 has 64 bytes of user-flash. The user-flash can store specific battery pack parameters, such as charge per VFC pulse, battery chemistry, and self-discharge rates.

flash programming

The two banks of direct user-flash are programmed one byte at a time, but the single bank of flash-shadowed RAM can be programmed one page at a time or by writing the RAM-to-flash transfer code into the flash command register (FCMD). This programming is performed by writing the desired code into the flash command register, FCMD (address 0x62), the host may transfer data between flash and RAM, page erase the flash, place the device into the low power mode, or perform VFC offset measurement. For more details, refer to the *flash command register* section. Summaries of the flash command codes are shown in Table 5.

Table 5. Flash Command Code Summary

COMMAND CODE (HEX)	DESCRIPTION
0x0F	Program byte
0x40	Erase page 0 flash
0x41	Erase page 1 flash
0x42	Erase page 2 flash
0x45	Transfer page 0 RAM to page 0 flash
0x48	Transfer page 0 flash to page 0 RAM
0xF6	Power down

single-byte programming

To program an individual byte in flash, the byte of data is first written into the FPD register while the address to be programmed is written into the FPA register. The program byte command, 0x0F, is then written to the FCMD. The result of this sequence is that the contents of the FPD register are logically AND'd with the contents of the flash address pointed to by the FPA register.

RAM-to-flash transfer

The content of the flash that shadows the user RAM is logically AND'd to the RAM contents when the RAM-to-flash transfer command is sent. If new data is to be written over old data, then it is necessary to first erase the flash page that is being updated and restore all necessary data.

APPLICATION INFORMATION

charge-time count registers (CTCH/CTCL)

The CTCH high-byte register (address = 0x66) and the CTCL low-byte register (address = 0x65) determine the length of time the $V_{SRP} > V_{SRN}$, indicating a charge activity. The counts in these registers are incremented at a rate of 4096 counts per hour. If the CTCH/CTCL registers continue to count beyond FFFF hex, the STC bit is set in the MODE/WOE register indicating a rollover. Once set, DTCH and DTCL increment at a rate of 16 counts per hour.

NOTE: If a second rollover occurs, STC is cleared. Access to the bq26200 should be timed to clear CTCH/CTCL more often than every 170 days. The TMP/CLR register forces the reset of both the CTCH and CTCL to zero.

mode, wake-up enable register (MODE/WOE)

As described below, the MODE/WOE register (address = 0x64) contains regulator disable and the STC and STD bits, and wake-up enable information.

Table 7. MODE/MOE Bits

MODE/WOE BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	DISREG	STC	STD	WOE2	WOE1	WOE0	0

RSVD

APPLICATION INFORMATION

clear register (CLR)

The bits in the CLR register (address 0x63) clear the DCR, CCR, SCR, DTC, and CTC registers indicate if the bq26200 has experienced a power-on-reset and setting the state of the STAT pin as described below:

Table 8. CLR Bits

CLR BITS							
7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
RSVD	POR	STAT	CTC	DTC	SCR	CCR	DCR

RSVD RSVD bit is reserved for future use and should not be modified by the host

POR POR bit indicates a power-on-reset has occurred. This bit is set when V_{CC} has gone below the POR level. This bit can also be set and cleared by the host.

STAT STAT bit, (bit 5), sets the state of the open-drain output of the STAT pin. A 1 turns off the open drain output while a 0 turn the output on. This bit is set to 1 on power-on-reset.

CTC CTC bit, (bit 4), clears the CTCH and CTCL registers and the STC bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the CTC bit is cleared. This bit is cleared on power-on-reset.

DTC DTC bit, (bit 3), clears the DTCH and DTCL registers and the STD bit. A 1 clears the corresponding registers and bit. After the registers are cleared, the DTC bit is cleared. This bit is cleared on power-on-reset.

SCR SCR bit, (bit 2), clears both the SCRH and SCRL registers. Writing a 1 to this bit clears the SCRH and SCRL register. After these registers are cleared, the SCR bit is cleared. This bit is cleared on power-on-reset.

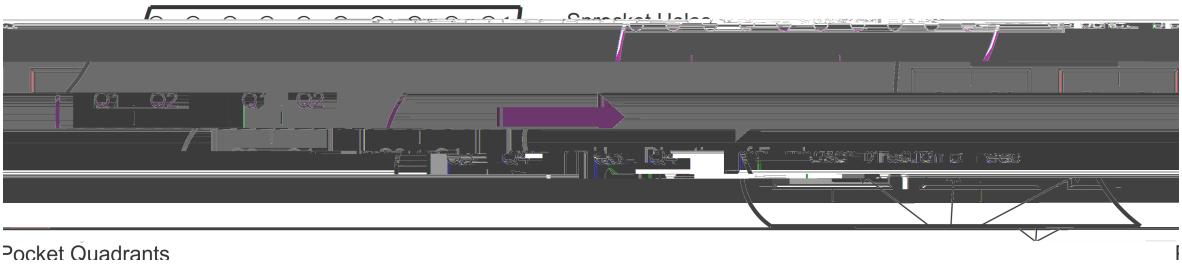
CCR CCR bit (bit 1) clears both the CCRH and CCRL registers. Writing a 1 to this bit clears the CCRH and CCRL registers. After these registers are cleared, the CCR bit is cleared. This bit is cleared on power-on-reset.

DCR DCR bit (bit 0) clears both the DCRH and DCRL register. Writing a 1 to this bit clears the DCRH and DCRL registers. After these registers are cleared, the DCR bit is cleared. This bit is cleared on power-on-reset.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples

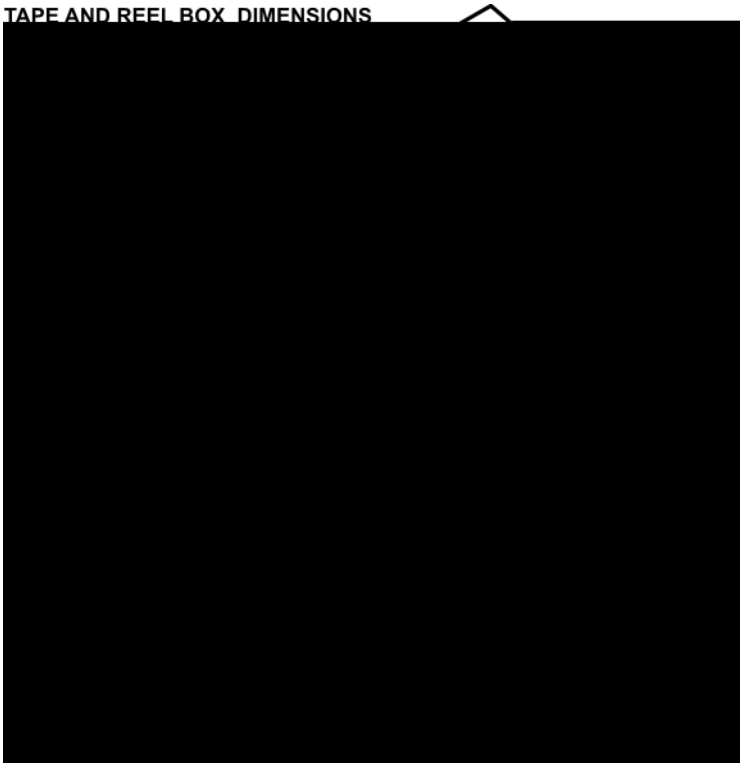
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ26200PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

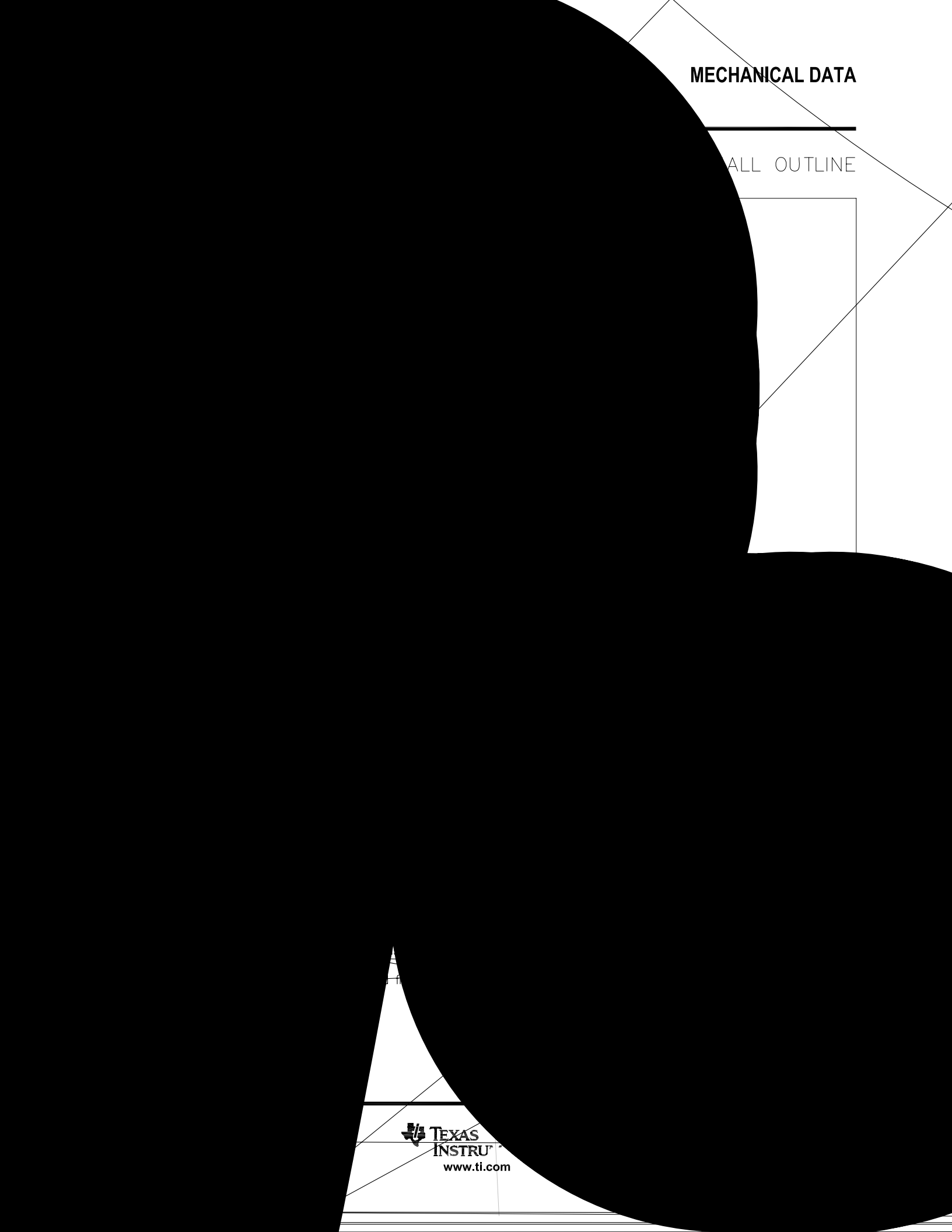


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ26200PWR	TSSOP	PW	8	2000	367.0	367.0	35.0

MECHANICAL DATA

ALL OUTLINE



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