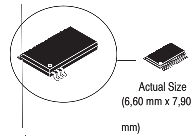


MULTICHEMISTRY BATTERY CHARGER CONTROLLER AND SYSTEM POWER SELECTOR

FEATURES

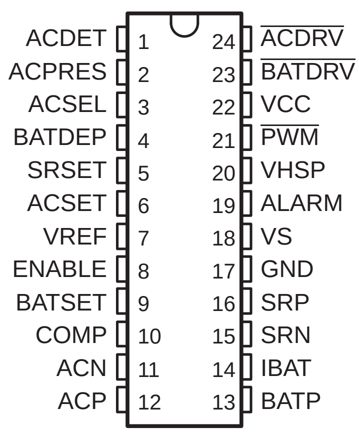
- **Dynamic Power Management, DPM Minimizes Battery Charge Time**
- **Integrated Selector Supports Battery Conditioning and Smart Battery Learn Cycle**
- **Zero Volt Operation**
- **Selector Feedlctor**

DESCRIPTION

The bq24702/bq24703 is a highly integrated battery charge controller and selector tailored for notebook and sub-notebook PC applications.

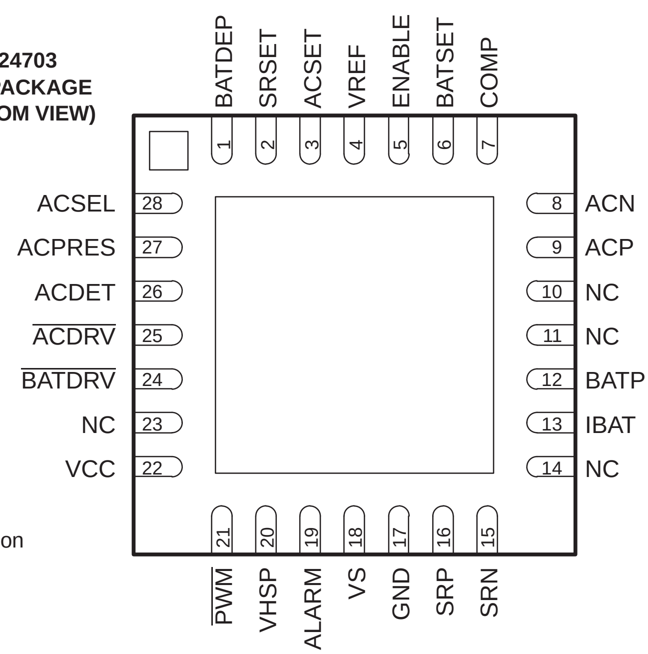
The bq24702/bq24703 uses dynamic power management (DPM) to minimize battery charge time

bq24702, bq24703
PW PACKAGE
(TOP VIEW)



NC - No internal connection

bq24703
RHD PACKAGE
(BOTTOM VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION (CONTINUED)

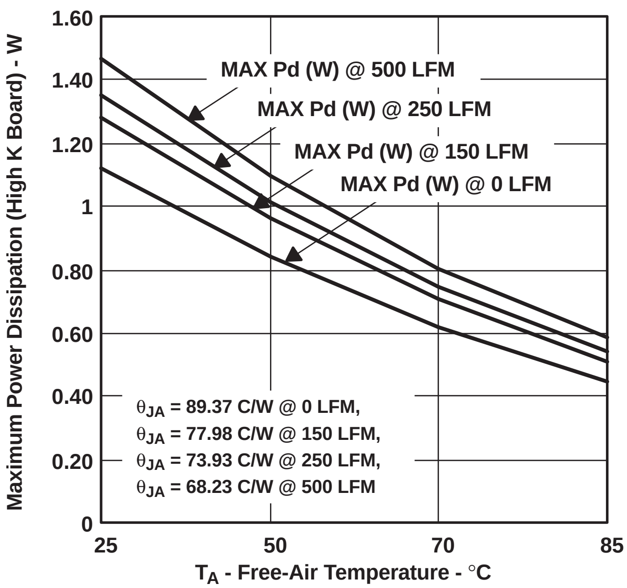
The battery voltage limit can be programmed by using the internal 1.196-V, ±0.5% precision reference, making it suitable for the critical charging demands of lithium-ion cells. Also, the bq24702/bq24703 provides an option to override the precision reference and drive the error amplifier either directly from an external reference or from a resistor divider off the 5 V supplied by the integrated circuit.

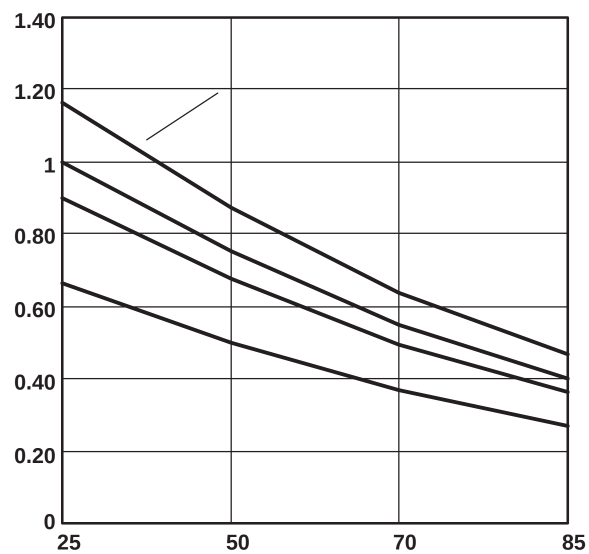
The selector function allows the manual selection of the system power source, battery or wall-adapter power. The bq24702/bq24703 supports battery-conditioning and battery-learn cycles through the ACSEL function. The ACSEL function allows manual selection of the battery or wall power as the main system power. It also provides autonomous switching to the remaining source (battery or ac power) should the selected system power source terminate (refer to Available Options table for the differences between the bq24702 and the bq24703). The bq24702/bq24703 also provides an alarm function to indicate a depleted battery condition.

The bq24702/bq24703 PWM controller is ideally suited for operation in a buck converter for applications when the wall-adapter voltage is greater than the battery voltage.

DISSIPATION RATINGS

MAXIMUM POWER DISSIPATION (HIGH K BOARD) vs FREE-AIR TEMPERATURE





A. The JEDEC low K (1s) board design used to derive this data was a 3-inch × 3-inch, two layer board with 2 ounce copper traces on top of the board.

B. The JEDEC high K (1s) board design used to derive this data was a 3-inch × 3-inch, multilayer board with 1 ounce internal power and ground planes and 2 ounce copper traces on top and bottom of the board.

AVAILABLE OPTIONS

CONDITION 20°C ≤ T_J ≤ 125°C	**SELECTOR OPERATION**	
	bq24702PW	**bq24703RHD**
BATTERY AS POWER SOURCE		
Battery removal	Automatically selects ac + alarm	Automatically selects ac + alarm
Battery reinserted	Selection based on selector inputs	Adapter latched until adapter is removed or ac select toggles.
AC AS POWER SOURCE		
AC removal	Automatically selects battery	Automatically selects battery
AC reinserted	Selection based on selector inputs	Selection based on selector inputs
POWER**20**		

ABSOLUTE MAXIMUM RATINGS

RECOMMENDED OPERATING CONDITIONS

ELECTRICAL CHARACTERISTICS

ELECTRICAL CHARACTERISTICS (Continued)

–40°C

(3) $I_{BAT} = \frac{SRSET}{R_{SENSE}} \times \frac{1}{A_V}$

measured gain, A_V. $\Delta c = \frac{SRSET}{A_V}$, Total accuracy in % $= \frac{(\Delta m - \Delta c)}{\Delta c} \times 100, I_{(SRP)} - I_{(SRN)} = 0$

[redacted]

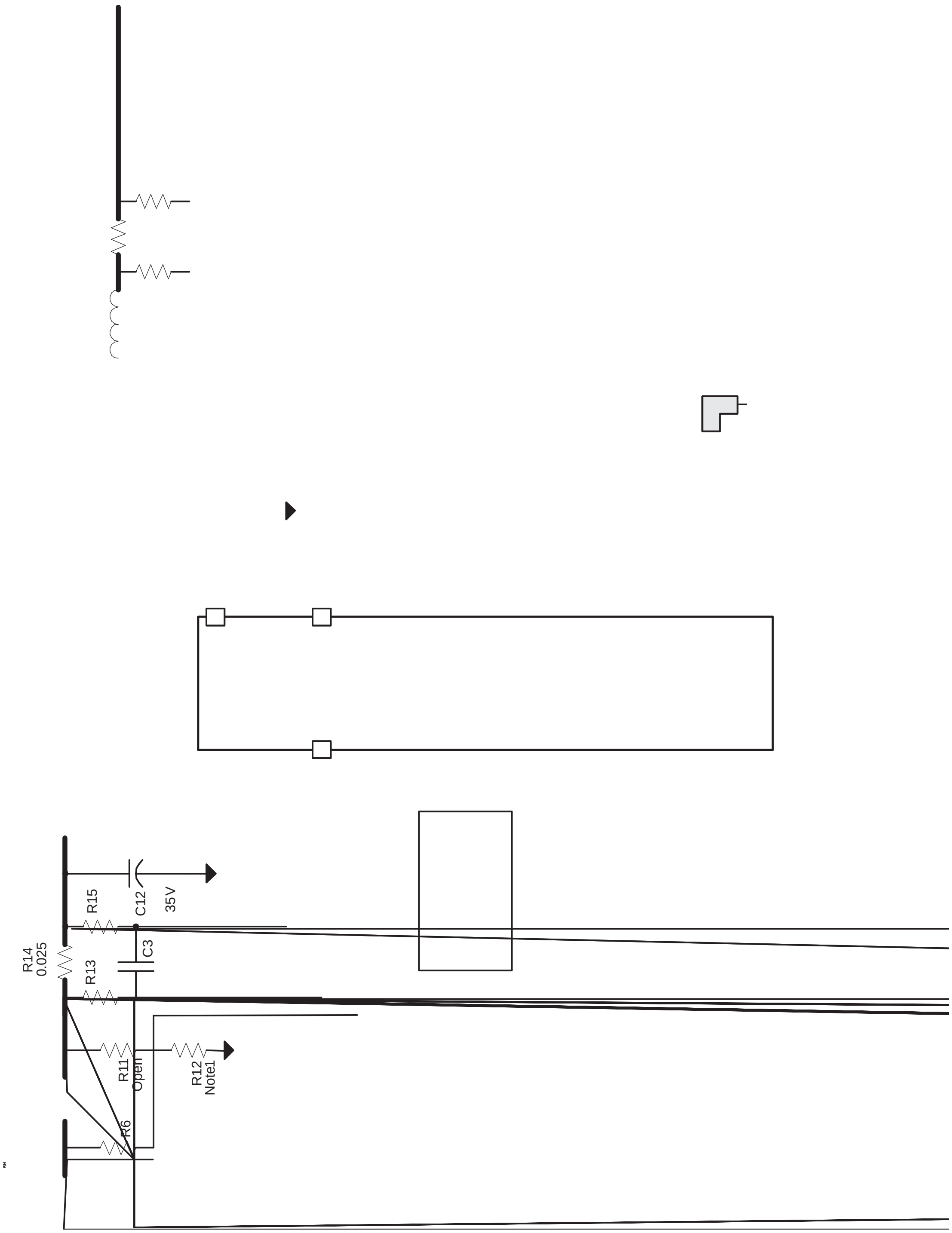
ELECTRICAL CHARACTERISTICS (Continued)

–40°C T_J 125°C, 7 V_{DC} V_{CC} 28 V_{DC}, all voltages relative to V_{SS} (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY CURRENT OUTPUT AMPLIFIER						
$G_{(TR)}$	Transfer gain	(SRP–SRN) = 5 mV[1]		20		V/V
$V_{I(BAT)}$	Battery current readback output voltage (IBAT)	(SRP–SRN) = 5 mV, SRP = 12 V, V_{CC} = 18 V, T_J = 25°C		100		mV
	Line rejection voltage	T_J = 25°C		10		mV/V
CM	Common-mode input range (SRP)		5		28	V
$V_{O(IBAT)}$	Battery current output voltage range (IBAT)		0		2.5	V
$I_{S(O)}$	Output source current (IBAT)	(SRP–SRN) = 100 mV	5	7.1	9.4	mA
	Total battery current readback full-scale accuracy	(SRP–SRN) = 50 mV, T_J = 25°C[1]	–3%		2.4%	
		(SRP–SRN) = 50 mV, 0°C T_J 85°C	–20%		20%	
		(SRP–SRN) = 100 mV, T_J = 25°C[1]	–1.5%		1.2%	
		(SRP–SRN) = 100 mV, 0°C < T_J < 85°C	–6%		8.5%	
5-V VOLTAGE REFERENCE						
V_{ref}	Output voltage (VREF)	T_J = 25°C	4.985	5	5.013	V
		T_J = 0°C to 85°C	4.946	5	5.013	
		T_J = 40°C to 85°C	4.946	5	5.03	V
		T_J = –40°C to 125°C	4.926	5	5.03	V
	Line regulation	I_{LOAD} = 5 mA		0.1	0.37	mV/V
	Load regulation	1 mA I_{LOAD} 5 mA		1.1	4	mV/mA
	Short circuit current		8	C		
				[redacted]		

(1) Battery readback transfer gain $G_{TR} = \frac{V_{IBAT}}{(SRP - SRN)}$

APPLICATION DIAGRAM



BLOCK DIAGRAM

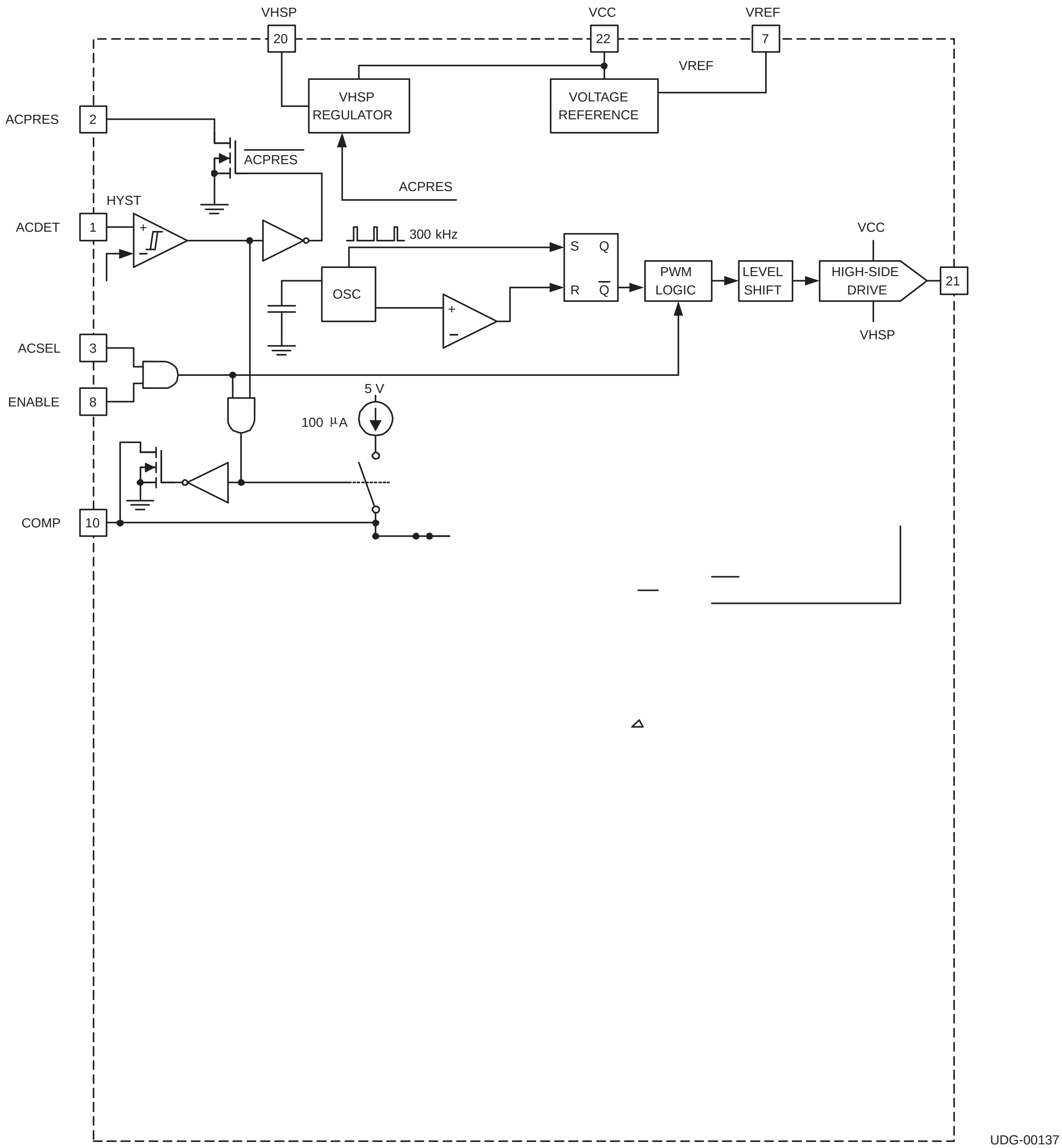


Table 1. TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	bq24702 (PW)	bq24703 (QFN)		
ACDET	1	26	I	AC or adapter power detection
$\overline{\text{ACDRV}}$	24	25	O	AC or adapter power source selection output
ACN	11	8	I	Negative differential input
ACP	12	9	I	Positive differential input
ACPRES	2	27	O	AC power indicator
ACSEL	3	28	I	AC adapter power select
ACSET	6	3	I	Adapter current programming voltage
ALARM	19	19	O	Alarm output
BATDEP	4	1	I	Depleted battery level
$\overline{\text{BATDRV}}$	23	24	O	Battery power source select output
BATP	13	12	I	Battery charge regulation voltage measurement input to the battery-voltage g_m amplifier
BATSET	9	6	I	External override to an internal precision reference
COMP	10	7	O	Inverting input to the PWM comparator
ENABLE	8	5	I	Charge enable
GND	17	17	O	Supply return and ground reference
IBAT	14	13	O	Battery current differential amplifier output
$\overline{\text{PWM}}$	21	21	O	Gate drive output
SRN	15	15	I	Negative differential battery current sense amplifier input
SRP	16	16	I/O	Positive differential battery current sense amplifier input
SRSET	5	2	I	Battery charge current programming voltage
VCC	22	22	I	Operational supply voltage
VHSP	20	20	O	Voltage source to drive gates of the external MOSFETs
VREF	7	4	O	Precision 5-V

PIN ASSIGNMENTS

ALARM: Depleted battery alarm output. This open-drain pin indicates that a depleted battery condition exists. A pullup on ALARM goes high when the voltage on the BATDEP pin is below V_{ACPRES}. On the bq24702, the ALARM output also activates when the selector inputs do not match the selector state.

BATDEP: Depleted battery level. A voltage divider network from the battery to BATDEP pin is used to set the battery voltage level at which depletion is indicated by the ALARM pin. See ALARM pin for more details. A battery depletion is detected when BATDEP is less than V_{ACPRES}. A no-battery condition is detected when the battery voltage is < 80% of the depleted threshold. In a no-battery condition, the bq24702 automatically selects ac as the input source. If ENABLE = 1, the PWM remains enabled.

$\overline{\text{BATDRV}}$: Battery power source select output. This pin drives an external P-channel MOSFET used to switch the battery as the system's power source. When the voltage level on the ACDET pin is less than V_{ACPRES}, the output of the $\overline{\text{BATDRV}}$ pin is driven low, GND. This pin is driven high (V_{CC}) when ACSEL is high and ACDET > V_{ACPRES}.

BATP: Battery charge regulation voltage measurement input to the battery-voltage g_m amplifier. The voltage on this pin is typically derived from a voltage divider network connected across the battery. In a voltage loop, BATP is regulated to the V_{FB} precision reference of the battery voltage g_m amplifier.

BATSET: An external override to an internal precision reference. When BATSET is > 0.25 V, the voltage level on the BATSET pin sets the voltage charge level. When BATSET 0.25 V, an internal V_{FB} reference is connected to the inverting input of the battery error amplifier. To ensure proper battery voltage regulation with BATSET, BATSET must be > 1.0 V. Simply ground BATSET to use the internal reference.

COMP: The inverting input to the PWM comparator and output of the g_m amplifiers. A type II compensation network between COMP and GND is recommended.

ENABLE: Charge enable. A high on this input pin allows PWM control operation to enable charging while a low on this pin disables and forces the PWM output to a high state. Battery charging is initiated by asserting a logic 1 on the ENABLE pin.

GND: Supply return and ground reference

IBAT: Battery current differential amplifier output. The output of this pin produces a voltage proportional to the battery charge current. This voltage is suitable for driving an ADC input.

$\overline{\text{PWM}}$: Gate drive output pin drives the P-channel MOSFET for PWM control. The PWM control is active when ACPRES, ACSEL, and ENABLE are high. $\overline{\text{PWM}}$ is driven low to V_{HSP} and high to V_{CC}.

SRN, SRP: Differential amplifier inputs for battery current sense. These pins feed back the battery charge current for PWM control. SRN is tied to the battery terminal. SRP is the source pin for zero volt operation.

SRSET: Battery charge current programmed voltage. The level on this pin sets the battery charge current limit.

VCC: Operational supply voltage.

VHSP: The VHSP pin is connected to a 1- F capacitor (close to the pin) to provide a stable voltage source to drive the gates of the external MOSFETs. VHSP = VCC – 10 V for VCC > 10.5 V and VHSP = VCC – 0.5 V for VCC <10.5 V. A 13-V Zener diode should be placed between VCC and VHSP to prevent MOSFET overstress during start-up.

VREF: Bypassed precision voltage 5-V output. It can be used to set fixed levels on the inverting inputs of any one of the three error amplifiers if desired. The tight tolerance is suitable for charging lithium-ion batteries.

VS: System (Load) voltage input pin. The voltage on this pin indicates the system voltage in order to insure a break before make transition when changing from ac power to battery power. The battery is protected from an over-voltage condition by disabling the P-channel MOSFET connected to the $\overline{\text{BATDRV}}$ pin if the voltage at VS is greater than BATP. This function can be eliminated by grounding the VS pin.

APPLICATION INFORMATION

PROGRAMMING THE THRESHOLDS

The input-referenced thresholds for battery depleted, ac detection and charge voltage are defined by dimensioning the external dividers connected to pins BATDEP, ACDET and BATP. This calculation is simple, and consists of assuming that when the input voltage equals the desired threshold value the voltage at the related pin is equal to the pin internal reference voltage:

Vinput = Vpin × (1 + Kres)

where:

Vinput = Target threshold, referenced to input signal

Vpin = Internal reference(1.196 V for BATP; 1.246 V for BATDEP, ACDET)

Kres = External resistive divider gain (for instance: R24/R25 for BATP)

When using external dividers with high absolute value the input bias currents for those pins must be included in the threshold calculation. On the bq24702/3 the input bias currents increase the actual value for the threshold voltage, when compared to the values calculated using the internal references and divider gain only:

Vinput = Vpin × (1+Kres) + Vbias

The increase on the threshold voltage is given by:

Vbias = Rdiv × Ipin

where:

Vbias = Voltage increase due to pin bias current

Rdiv = External resistor value for resistor connected from pin to input voltage

Ipin = Maximum pin leakage current

The effect of IB can be reduced if the resistor values are decreased.

DYNAMIC POWER MANAGEMENT

The dynamic power management (DPM) feature allows a cost effective choice of an ac wall-adapter that accommodates 90% of the system's operating-current requirements. It minimizes battery charge time by allocating available power to charge the battery (i.e. $I_{BAT} = I_{ADPT} - I_{SYS}$). If the system plus battery charge current exceeds the adapter current limit, as shown in Figure 1, the DPM feature reduces the battery

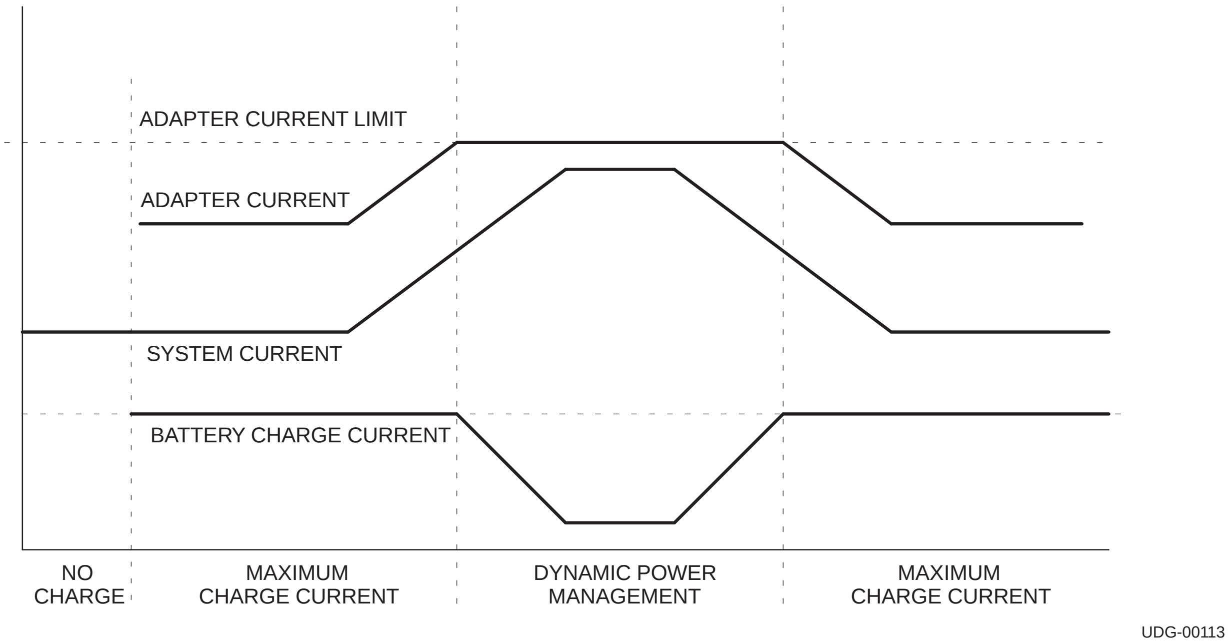


Figure 1. Dynamic Power Management

ACDET OPERATION

The ACDET function senses the loss of adequate adapter power. If the voltage on ACDET drops below the internal V_{ACPRES} reference voltage, a loss of ADAPTER power is declared and the bq24702/bq24703 switches to battery power as the main system power. In addition, the bq24702/bq24703 shuts down its 5-V VREF and enters a low power sleep mode.

BATTERY CHARGER OPERATION

The bq24702/bq24703 fixed-frequency, PWM controller is designed to provide closed-loop control of battery charge-current (I_{CH}) based on three parameters, battery-float voltage (V_{BAT}), battery-charge current, and adapter charge current (I_{ADPT}). The bq24702/bq24703 is designed primarily for control of a buck converter using a high side P-channel MOSFET device (SW, refer to Figure 2).

The three control parameters are voltage programmable through resistor dividers from the bq24702/bq24703 precision 5-V reference, an external or internal precision reference, or directly via a DAC interface from a keyboard controller.

Adapter and battery-charge current information is sensed and fed back to two transconductance (g_m) amplifiers via low-value-sense resistors in series with the adapter and battery respectively. Battery voltage information is sensed through an external resistor divider and fed back from the battery to a third g_m amplifier.

PRECHARGE OPERATION

The precharge operation must be performed using the PWM regulator. The host can set the precharge current externally by monitoring the ALARM pin to detect a battery depleted condition and programming SRSET voltage to obtain the desired precharge current level.

ZERO VOLT OPERATING

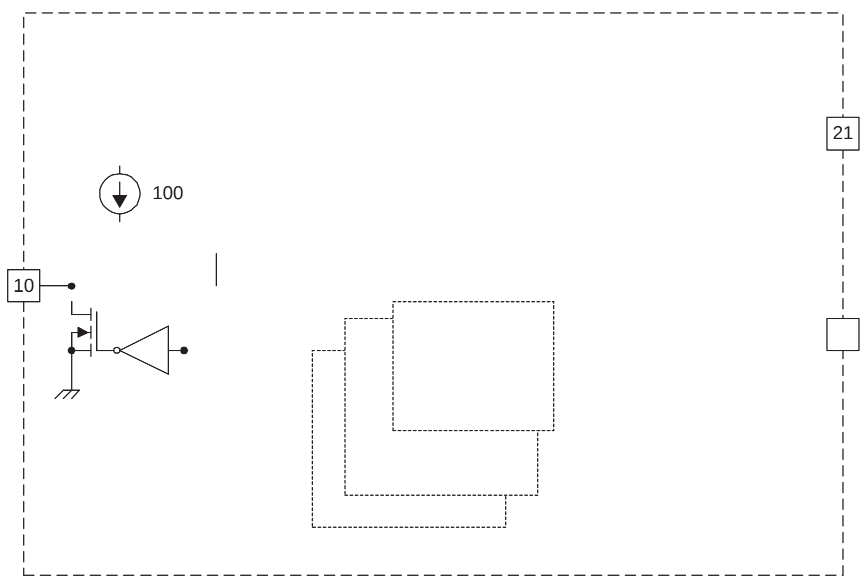
The zero volt operation is intended to provide a low current path to close open packs and protect the system in the event of a pack cell short-circuit condition or if a short is applied to the pack terminal. It is not designed to precharge depleted packs, as it is disabled at voltages that are not within normal pack operating range for precharge.

If the voltage at BATDEP pin is below the zero volt operation threshold , charge is enabled (EN=HI), and ac is selected (ACSEL=HI) the bq24702/3 enters the zero volt operation mode. When the zero volt operation mode is on, the internal PWM is disabled, and an internal power MOSFET connects SRP to V_{CC}. The battery charge current is limited by the filter resistor connected to SRP pin (R19). R19 must be dimensioned to withstand the worst case power dissipation when in zero volt operation mode.

The zero volt operation mode is disabled when BATDEP is above the zero volt operation threshold, and the main PWM loop is turned on if charge is enabled, regulating the current to the value set by SRSET voltage. To avoid errors on the charge current both resistors on the SRP, SRN filter must have the same value. Note, however, that R21 (connected to SRN) does not dissipate any power when in zero volt operation and can be of minimum size.

PWM OPERATION

The three open collector g



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SOFTSTART

Softstart is provided to ensure an orderly start-up when the PWM is enabled. When the PWM controller is disabled (ENABLE = Low), the 100-μA current source pullup is disabled and the COMP pin is actively pulled down to GND. Disabling the 100-μA pullup reduces current drain when the PWM is disabled. When the bq24702/bq24703 PWM is enabled (ENABLE = High), the COMP pin is released and the 100-μA pullup is enabled (refer to Figure 2). The voltage on the COMP pin increases as the pullup charges the external compensation network connected to the COMP pin. As the voltage on the COMP pin increases the PWM duty cycle increases linearly as shown in Figure 3.

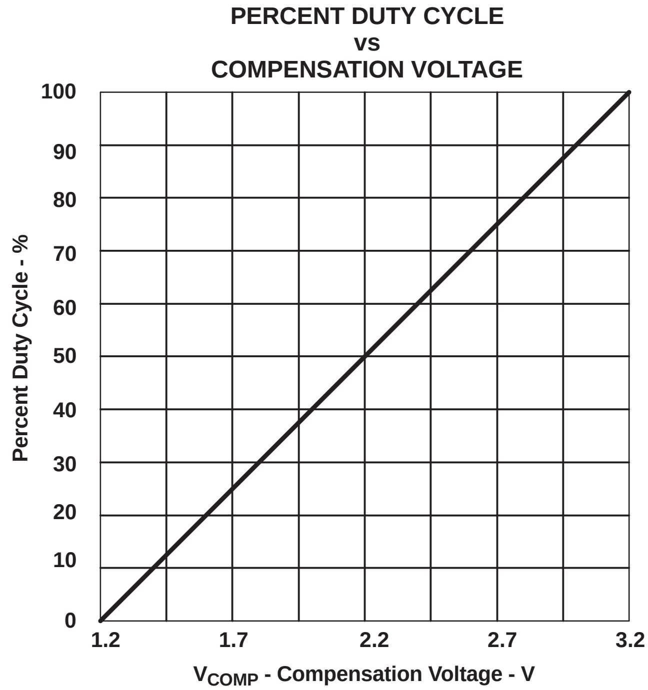


Figure 3.

As any one of the three controlling loops approaches the programmed limit, the g_m amplifier begins to shunt current away from the COMP pin. The rate of voltage rise on the COMP pin slows due to the decrease in total current out of the pin, decreasing the rate of duty cycle increase. When the loop has reached the programmed limit the g_m amplifier shunts the entire bias current (100 μA) and the duty cycle remains fixed. If any of the control parameters tries to exceed the programmed limit, the g_m amplifier shunts additional current from the COMP pin, further reducing the PWM duty cycle until the offending parameter is brought into check.

SETTING THE BATTERY CHARGE REGULATION VOLTAGE

The battery charge regulation voltage is programmed through the BATSET pin, if the internal precision reference is not used. The BATSET input is a high-impedance input that is driven by either a keyboard controller DAC or via a resistor divider from a precision reference (see Figure 4).

The battery voltage is fed back to the g_m amplifier through a resistor divider network. The battery charge regulation voltage can be defined as:

$$V_{BATTERY} = \frac{(R1 + R2) \times V_{BATSET}}{R2} V + I_{BATP} \times R1 \quad (1)$$

where I_{BATP} = input bias current for pin BATP

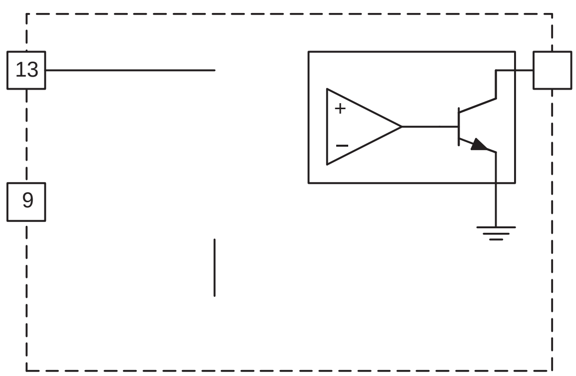
The overall accuracy of the battery charge regulation voltage is a function of the bypassed 5-V reference voltage tolerance as well as the tolerances on R1 and R2. The precision voltage reference has a 0.5% tolerance making it suitable for the tight battery voltage requirements of Li-ion batteries. Tolerance resistors of 0.1% are recommended for R1 and R2 as well as any resistors used to set BATSET.

The bq24702/bq24703 provides the capability of using an internal precision voltage reference through the use of a multiplexing scheme, refer to Figure 4, on the BATSET pin. When BATSET voltage is less than 0.25 V, an internal reference is switched in and the BATSET pin is switched out from the g_m amplifier input. When the BATSET voltage is greater than 0.25 V, the BATSET pin voltage is switched in to the input of the g_m amplifier and the voltage reference is switched out.

NOTE:

The minimum recommended BATSET is 1.0 V, if BATSET is used to set the voltage loop.

(a) $V_{BATSET} < 0.25$ V



(b) $V_{BATSET} > 1$ V

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Figure 4. Battery Error Amplifier Input Multiplexing Scheme

PROGRAMMING THE BATTERY CHARGE CURRENT

The battery charge current is programmed via a voltage on the SRSET pin. This voltage can be derived from a resistor divider from the 5-V VREF or by means of an DAC. The voltage is converted to a current source that is used to develop a voltage drop across an internal offset resistor at one input of the SR $g_m$amplifier. The charge current is then a function of this voltage drop and the sense resistor (R_S), refer to Figure 5.

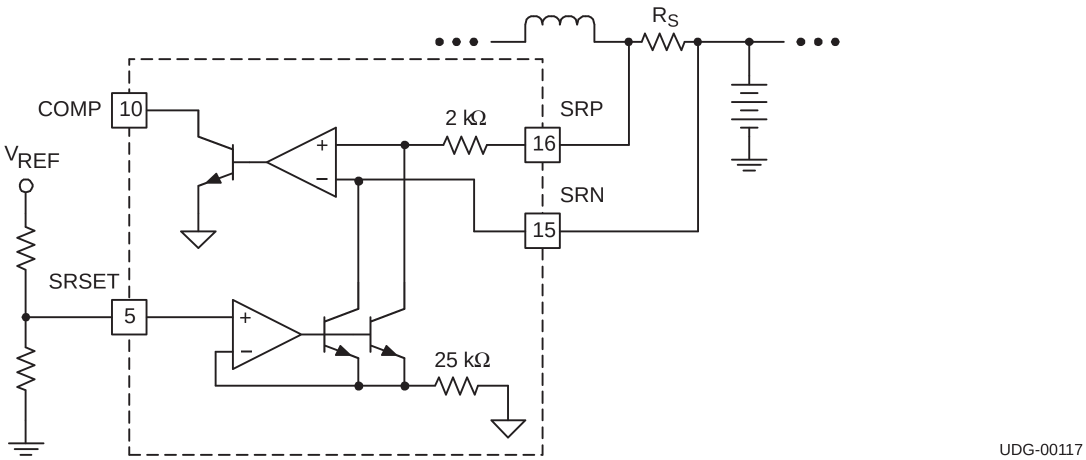

Figure 5. Battery Charge Current Input Threshold Function

The battery charge current can be defined as:

$$I_{BAT} = \frac{V_{SRSET}}{25 \times R_S} \tag{2}$$

where V_{SRSET} is the programming voltage on the SRSET pin. V_{SRSET} maximum is 2.5 V.

PROGRAMMING THE ADAPTER CURRENT

Like the battery charge current described previously, the adapter current is programmed via a voltage on the ACSET pin. That voltage can either be from an external resistor divider from the 5-V VREF or from an external DAC. The adapter current is defined as:

$$I_{ADPT} = \frac{V_{ACSET}}{25 \times R_{S2}} \tag{3}$$

Selecting an Output Capacitor

For this application the output capacitor is used primarily to shunt the output ripple current away from the battery. The output capacitor should be sized to handle the full output ripple current as defined as:

$$I_C\,(RMS) = \frac{\left(V_{IN} - V_{BAT}\right) \times D}{F_S \times L} \quad A_{RMS} \tag{8}$$

Selecting an Input Capacitor

The input capacitor is used to shunt the converter ripple current on the input lines. The capacitor(s) must have a ripple current (RMS) rating of:

$$I_{RMS} = \sqrt{[Ichg \times (1–D)]^2 \times D + [Ichg \times D]^2 \times (1–D)} \quad A_{RMS} \tag{9}$$

In addition to shunting the converter input ripple when the PWM is operating,

Compensating the Loop

$$F_Z = \frac{1}{2} \times \left(\frac{1}{\pi \times R_{COMP} \times C_Z}\right)\ Hz \tag{10}$$

$$F_P = \frac{1}{2} \times \left(\frac{1}{\pi \times R_{COMP} \times C_P}\right)\ Hz \tag{11}$$

SELECTOR OPERATION

UDG-00119

Figure 6. Selector Control Switches

AUTONOMOUS SELECTION OPERATION

Adapter voltage information is sensed

SMART LEARN CYCLES WHEN ADAPTER POWER IS PRESENT

Smart learn cycles can be conducted when adapter power is present by asserting and maintaining the ACSEL pin low. The adapter power can be

SYSTEM BREAK BEFORE MAKE FUNCTION

BATTERY DEPLETION DETECTION

SELECTOR/ALARM TIMING EXAMPLE

The selector and ALARM timing example in Figure 7 illustrates the battery conditioning support.

NOTE:

For manual selection of wall power as the main power source, both the ACPRES and ACSEL signals must be a logic high.

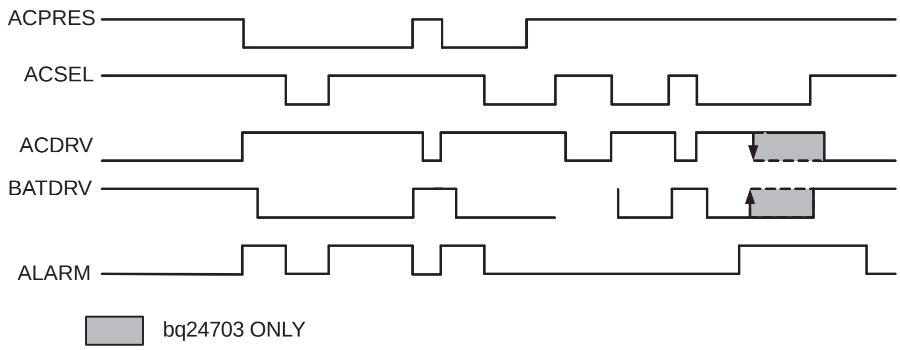

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Figure 7. Battery Selector and ALARM Timing Diagram

PWM SELECTOR SWITCH GATE DRIVE

Because the external P-channel MOSFETs (as well as the internal MOSFETs) have a maximum gate-source voltage limitation of the input voltage, VCC, cannot be used directly to drive the MOSFET gate under all input conditions. To provide safe MOSFET-gate-drive at input voltages of less than an intermediate gate drive voltage rail was established (VSHP). Where V_{HSP} = VCC – 10 V. This ensures adequate enhancement voltage across all operating conditions.

An external zener diode (D3) connected between VCC and VHSP is required for transient protection; its breakdown voltage should be above the maximum value for internal VHSP/VCC clamp voltage for all operating conditions.

TRANSIENT CONDITIONS AT SYSTEM, OVER-VOLTAGE AT SYSTEM TERMINAL

Overshoot conditions can be observed at the system terminal due to fast load transients and inductive characteristics of the system terminal to load connection. An overshoot at the system terminal can be directly coupled to the VCC and VBAT nodes, depending on the switch mode of operation. If the capacitors at VBAT and VCC can not reduce this overshoot to values below the absolute maximum ratings, it is recommended that an additional capacitor is added to the system terminal to avoid damage to IC or external components due to voltage overstress under those transient conditions.

AC ADAPTER COLLAPSING DUE TO TRANSIENT CONDITIONS

The ac adapter voltage collapses when the ac switch is on and a current load transient at the system exceeds the adapter current limit protection. Under those conditions the ac switch is turned off when the ac adapter voltage falls below the ac adapter detection threshold. If the system terminal to load impedance has an inductive characteristic, a negative voltage spike can be generated at the system terminal and coupled into the battery line via the battery switch backgate diode.

In normal operation, with a battery present, this is not an issue, as the low battery impedance holds the voltage at battery line. However, if a battery is not present or the pack protector switches are open the negative spike at the system terminal is directly coupled to the SRP/SRN pins via the R19/R21 resistors.

Avoid damage to the SRP/SRN pins if this transient condition happens in the application. If a negative voltage spike happens at system terminal and R19/R21 limit the current sourced from the pin to less than –50 mA (Ipin = Vsystem/R19), the pins SRP/SRN are not damaged and the external protection schottky diodes are not required. However, if the current under those transient conditions exceeds –50 mA, external schottky diodes must be added to clamp the voltage at pins SRP/SRN so they do not exceed the absolute maximum ratings specified (-0.3 V).

IBAT AMPLIFIER

A filter with a cutoff frequency smaller than 10 kHz should be added to the IBAT output to remove switching noise.

POWER DISSIPATION CALCULATION

During PWM operation, the power dissipated internally to the IC increases as the internal driver is switching the PWM FET on/off. The power dissipation figures are dependent on the external FET used, and can be calculated using the following equation:

$$Pd(max) = [IDDOP + Qg \times Fs(max)] \times VADAP$$

where:

Qg = Total gate charge for selected PWM MOSFET

IDDOP = Maximum quiescent current for IC

VADAP = Maximum adapter voltage

Fs(max) = Maximum PWM switching frequency

The maximum junction temperature for the IC must be limited to 125°C, under worst case conditions.

TYPICAL CHARACTERISTICS

ERROR AMPLIFIER REFERENCE vs JUNCTION TEMPERATURE

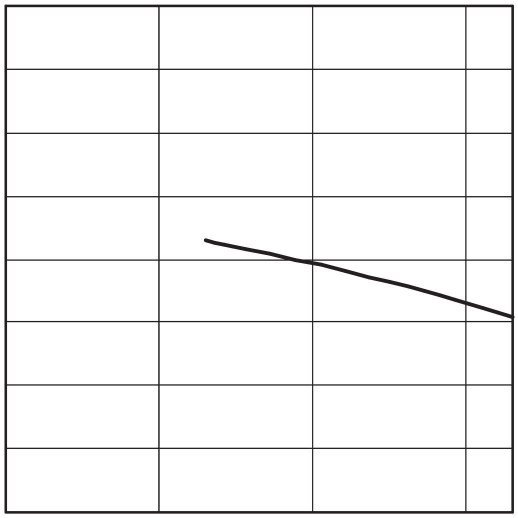

Figure 8.

BYPASSED 5-V REFERENCE vs JUNCTION TEMPERATURE

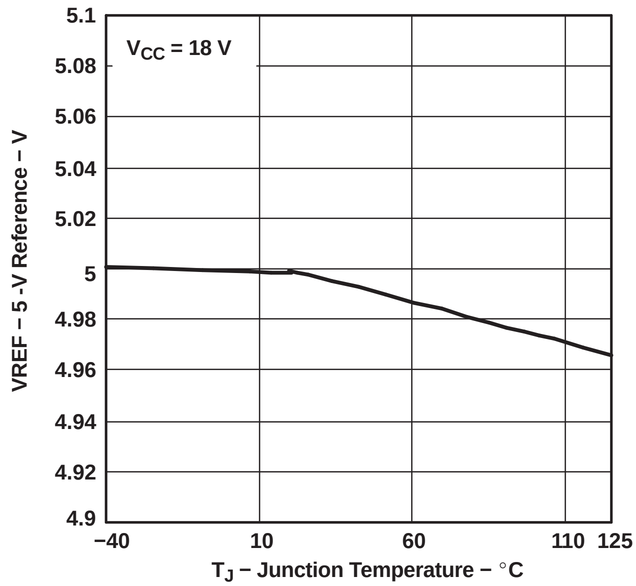

Figure 9.

TOTAL SLEEP CURRENT vs JUNCTION TEMPERATURE

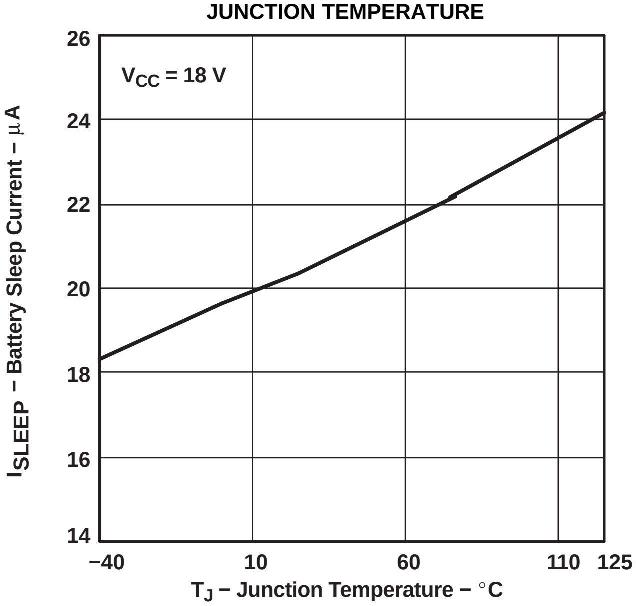

Figure 10.

OSCILLATOR FREQUENCY vs JUNCTION TEMPERATURE

T_J

Figure 11.

TYPICAL CHARACTERISTICS (continued)

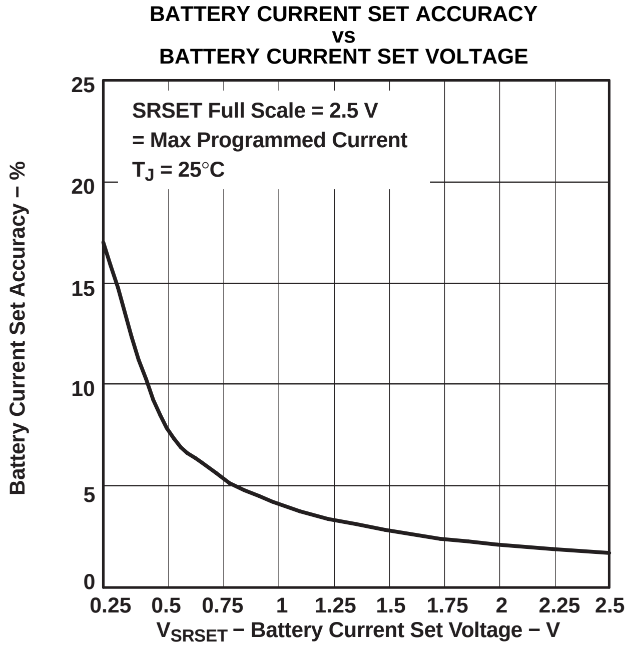

Figure 12.

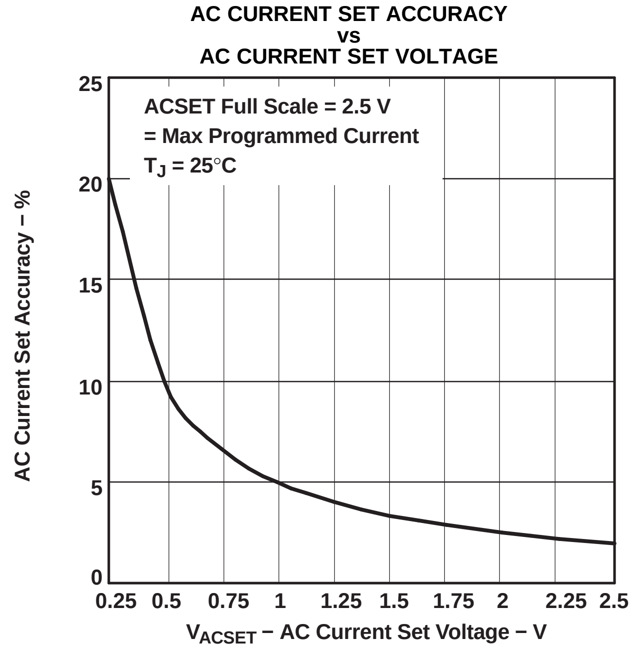

Figure 13.

BOARD LAYOUT GUIDELINES

Recommended Board Layout

Follow these guidelines when implementing the board layout:

1. Do not place lines and components dedicated to battery/adapter voltage sensing (ACDET,BATDEP, VS), voltage feedback loop (BATP, BATSET if external reference is used) and shunt voltage sensing (SRP/SRN/ACP/ACN) close to lines that have signals with high dv/dt (PWM, BATDRV, ACDRV, VHSP) to avoid noise coupling.
2. Add filter capacitors for SRP/SRN (C8) and ACP/ACN (C3) close to IC pins
3. Add Reference filter capacitor C1 close to IC pins
4. Use an isolated, clean ground for IC ground pin and resistive dividers used in voltage sensing; use an isolated power ground for PWM filter cap and diode (C11/D4). Connect the grounds to the battery PACK- and adapter GND.
5. Place C7 close to VCC pin.
6. Place input capacitor C12 close to PWM switch (U3) source and R14.
7. Position ac switch (U2) to minimize trace length from ac switch source to input capacitor C12.
8. Minimize inductance of trace connecting PWM pin and PWM external switch U3 gate
9. Maximize power dissipation planes connected to PWM switch
10. Maximize power dissipation planes connected to SRP resistor if steady state in zero volt mode is possible
11. Maximize power dissipation planes connected to D1

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
BQ24702PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24702PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24702PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24702PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24703PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24703PWG4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24703PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24703PWRG4	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
BQ24703RHDR	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24703RHDRG4	ACTIVE	VQFN	RHD	28	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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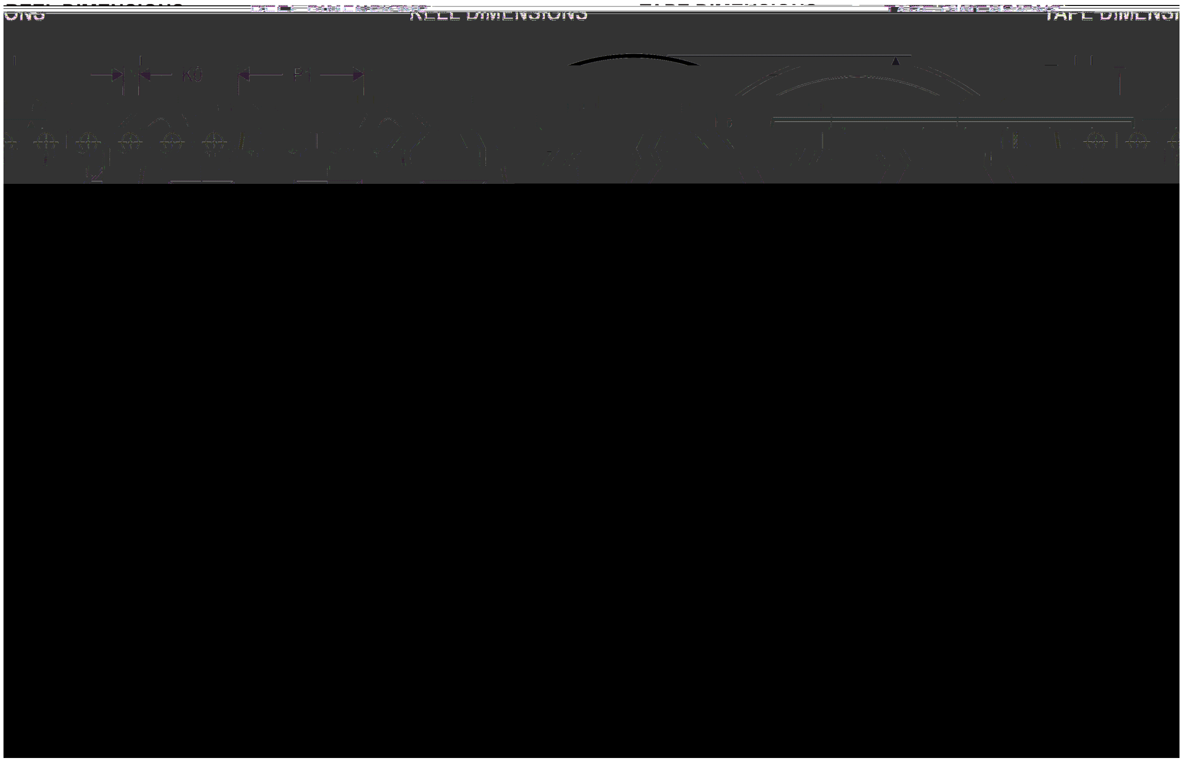
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ

[redacted]

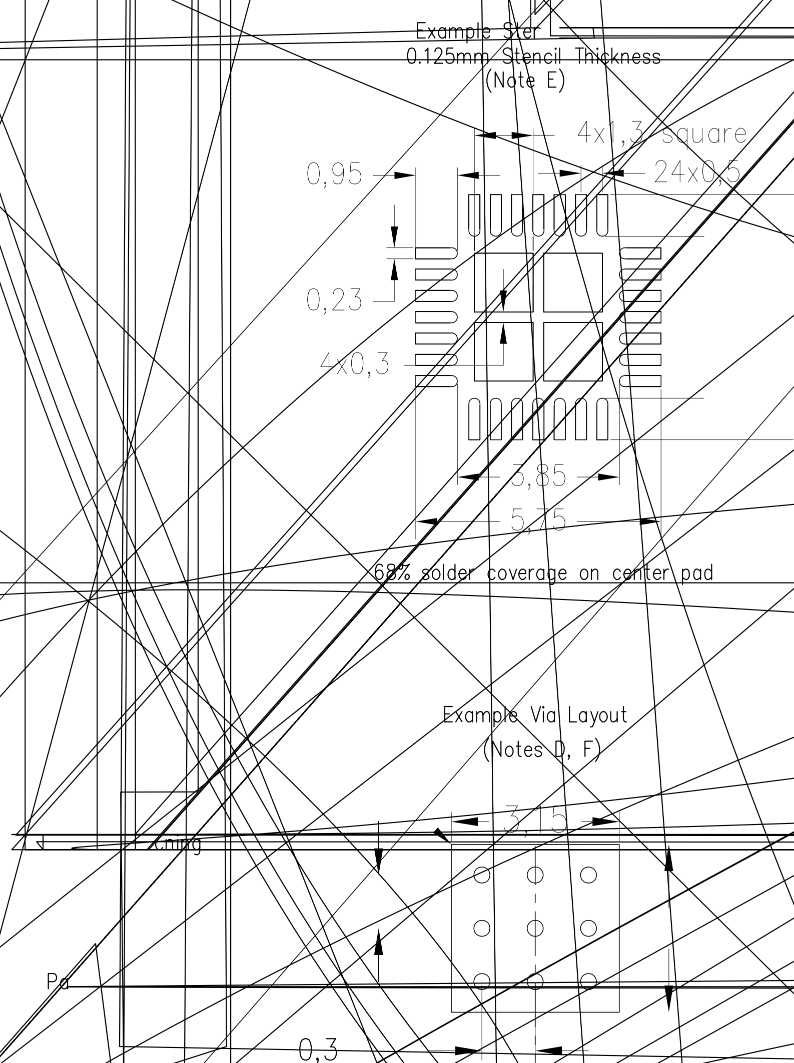
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24702PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
BQ24703PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
BQ24703RHDR	VQFN	RHD	28	3000	367.0	367.0	35.0

[redacted]

LAND PATTERN D

RHD (S-PVQFN-N28) PLASTIC QUAD FLATPACK NO-LEAD



C. Publication IPC-7351 is recommended for altern

D. This package is designed to be soldered to a thermal pad o

se documents are available at

E. omers

design considerations.

oard fabrication site for recommended solder mask tolerances and via tenting

recommendations for vias placed in thermal pad.

XAS
RUMENTS

IMPORTANT NOTICE

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