INTEGRATED CHARGE CONTROLLER FOR LEAD-ACID BATTERIES

Check for Samples: bq24450

FEATURES

- **Regulates Both Voltage and Current During Charging**
- **Precision Temperature-Compensated Reference:**
  - **Maximizes Battery Capacity Over Temperature**
  - **Ensures Safety While Charging Over Temperature**
- **Optimum Control to Maximize Battery Capacity and Life**
- **Supports Different Configurations**
- **Minimum External Components**
- **Available in 16-Pin SOIC (DW)**

APPLICATIONS

- **Emergency Lighting Systems**
- **Security and Alarm Systems**
- **Telecommunication Backup Power**
- **Uninterruptible Power Supplies**

DESCRIPTION

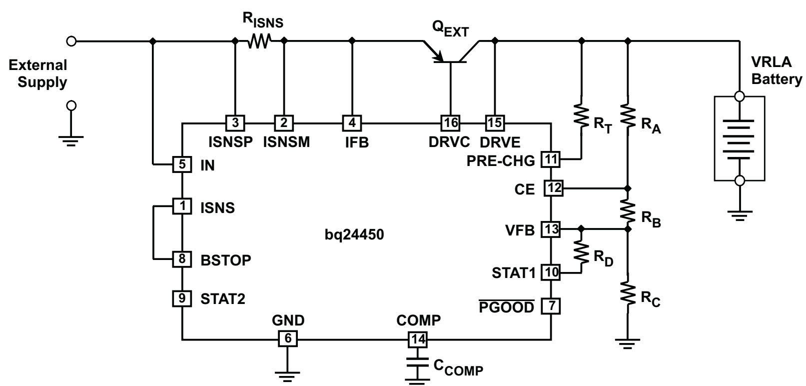
The bq24450 contains all the necessary circuitry to optimally control the charging of valve-regulated lead-acid batteries. The IC controls the charging current as well as the charging voltage to safely and efficiently charge the battery, maximizing battery capacity and life. Depending on the application, the IC can be configured as a simple constant-voltage float charge controller or a dual-voltage float-cum-boost charge controller.

The built-in precision voltage reference is especially temperature-compensated to track the characteristics of lead-acid cells, and maintains optimum charging voltage over an extended temperature range without using any external components. The ICs low current consumption allows for accurate temperature monitoring by minimizing self-heating effects.

The IC can support a wide range of battery capacities and charging currents, limited only by the selection of the external pass transistor. The versatile driver for the external pass transistor supports both NPN and PNP types and provides at least 25mA of base drive.

In addition to the voltage- and current-regulating amplifiers, the IC features comparators that monitor the charging voltage and current. These comparators feed into an internal state machine that sequences the charge cycle. Some of these comparator outputs are made available as status signals at external pins of the IC. These status and control pins can be connected to a processor, or they can be connected up in flexible ways for standalone applications.

Figure 1. TYPICAL APPLICATION SCHEMATIC



A dual-level Float-cum-Boost Charger with Pre-Charge

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

DEVICE PACKAGE	PACKING	ORDERABLE PART NUMBER	MARKING
SOIC (D)	Tube of 50	bq24450D	bq24450D
	Reel of 2500	bq24450DR	bq24450D

ABSOLUTE MAXIMUM RATINGS[(1)] [(2)] [(3)]

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
Input Voltage	IN	0.3 to 40	V
	PGOOD, STAT1, STAT2, ISNS	0.3 to 40	V
	VFB, IFB, ISNSP, ISNSM	0.3 to 40	V
	BSTOP	0.3 to 40	V
Voltage	PRE-CHG (with respect to IN)	32	V
Input Current	ISNS	80	mA
	STAT1, STAT2, PGOOD	20	mA
Output Current	PRE-CHG	40	mA
Input Current	DRVC	80	mA
Output Current	DRVE	80	mA
Power Dissipation at T_A = 25 C		1000	mW
Junction temperature, T_J		40 to 150	C
Storage temperature, T_{STG}		65 to 150	C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the ground terminal (pin 6) unless otherwise noted.
(3) Positive currents are into, and negative currents out of, the specified terminal.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNITS
V_{IN}	IN voltage range	5	40	V
I_{STAT1}, I_{STAT2}, I_{PGOOD}	Input current, open-collector status pins		5	mA
I_{ISNS}	Input current, open-collector ISNS comparator output		25	mA
T_J	Junction Temperature	40	70	C

[redacted]

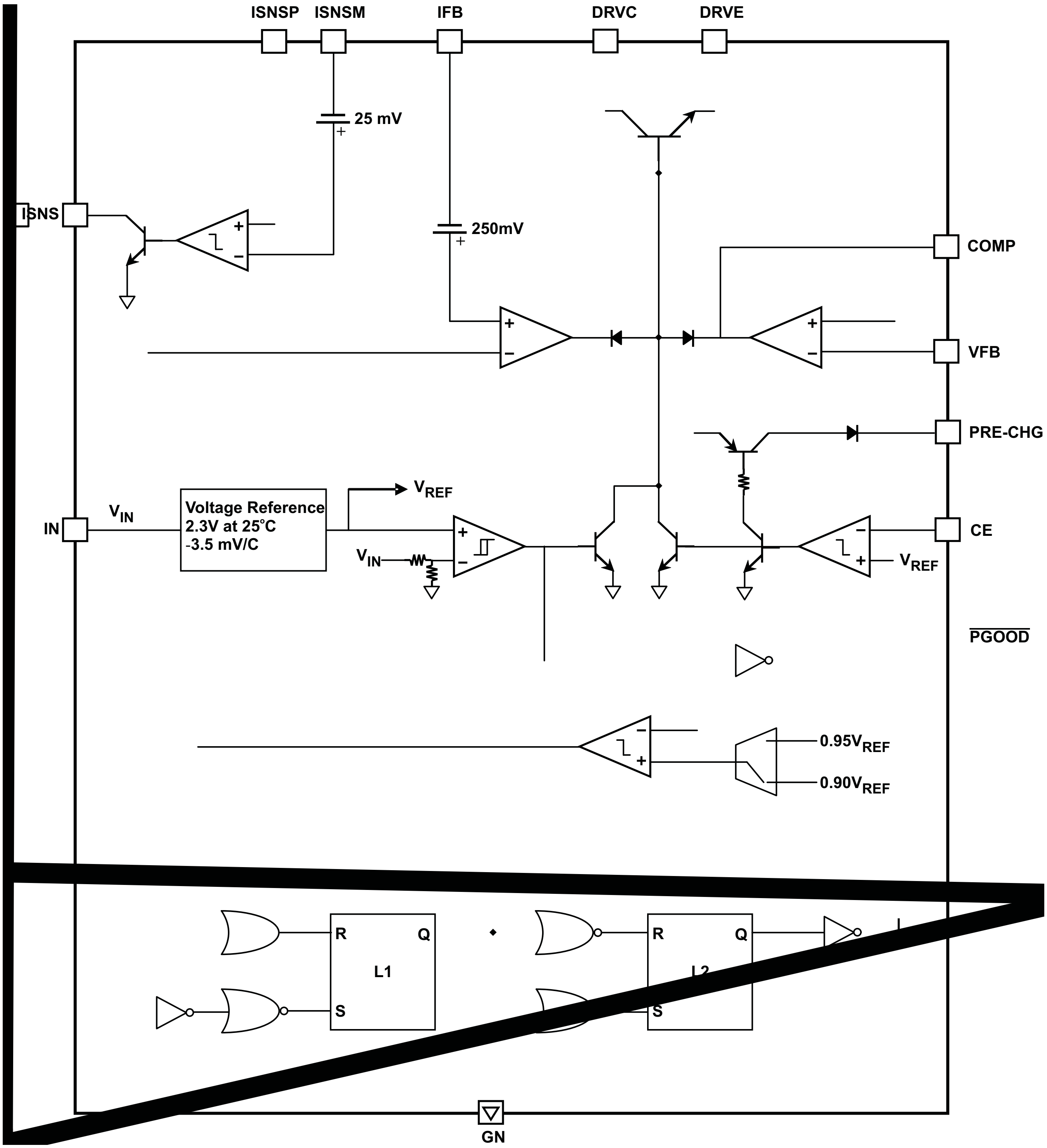


Figure 2. Simplified Block Diagram

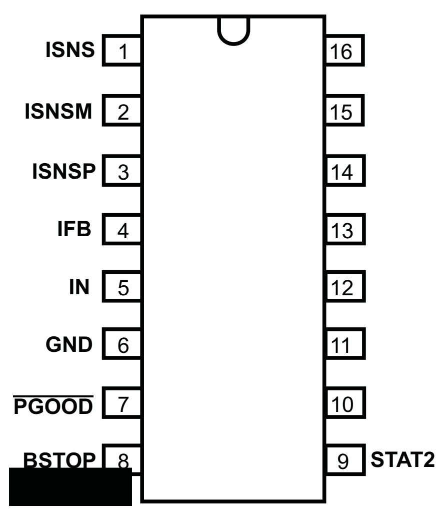
PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NO.	NAME		
1	ISNS	O	Output of the current-sense comparator. Open-Collector.
2	ISNSM	I	Negative input of the current-sense comparator.
3	ISNSP	I	Positive input of the current-sense comparator.
4	IFB	I	Input for the current-regulating loop. External resistor between IN and IFB sets the charging current value.
5	IN	I	Supply voltage pin. Connect to external DC source.
6	GND		Ground terminal.
7	PGOOD	O	Open-collector output, indicates supply status at IN pin. Active low.
8	BSTOP	I	Control input. Taking this pin from low to high transitions the charger from Boost Mode to Float Mode. Internally pulled up through a 10 A current source.
9	STAT2	O	Open-collector status outputs. See table below.
10	STAT1	O	
11	PRE-CHG	O	Can be used to trickle-charge the battery till its voltage rises to a safe value. PRE-CHG will source current as long as the control voltage on the CE pin is below VREF. If using, connect to battery pack through external resistor.
12	CE	I	Charge enable control. If the voltage on the CE pin is below VREF, the driver transistor will be off and the PRE-CHG pin will source current.
13	VFB	I	Voltage feedback pin. Connect to battery through external resistive divider.
14	COMP	I/O	Compensation terminal for voltage loop. Connect a capacitor from this pin to GND.
15	DRVE	O	Emitter of the internal (NPN) driver transistor.
16	DRVC	I	Collector of the internal (NPN) driver transistor.

STAT1	STAT2	CONDITION
On	Hi-Z	Bulk Charge
On	On	Boost Mode

PINOUT

STAT1	STAT2	



Tf 1d 65 vdBT / rg 6335ITnTd ((8 Td (I21 (below)TiVIEWistor.d 65 396 E.83 0 Td (FEBRUARY)Ti3 13.Ti 30.85 pvrighpd (O0 0

TYPICAL OPERATING PERFORMANCE

Compensated Voltage Reference vs Temperature

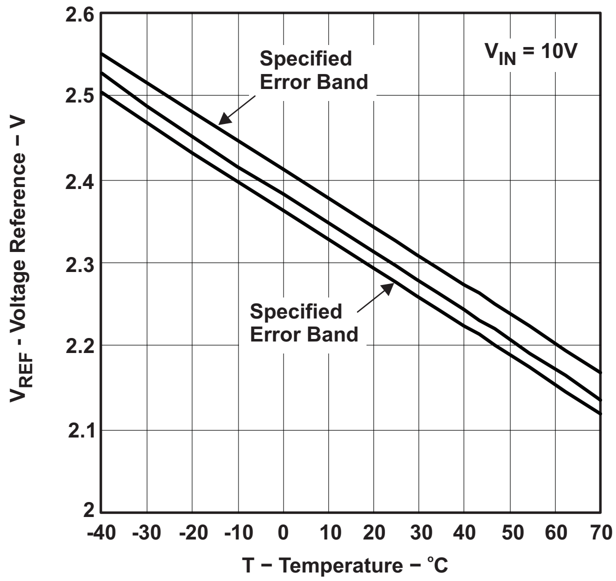


Figure 3. -

DETAILED FUNCTIONAL DESCRIPTION

The bq24450 contains all the necessary circuitry to optimally control the charging of sealed lead-acid batteries. The IC controls the charging current as well as the charging voltage to safely and efficiently charge the battery, maximizing battery capacity and life. Depending on the application, the IC can be configured in various ways: examples are a constant-voltage float charger, a dual-voltage float-cum-boost charger or a dual step current charger.

Only an external pass transistor and minimum number of external passive components are required along with the IC to implement a charger for sealed lead-acid batteries. The IC's internal driver transistor Q1 (see Figure 2) supports NPN as well as PNP pass transistors, and provides enough drive current (25mA specified) to support a wide range of charging rates.

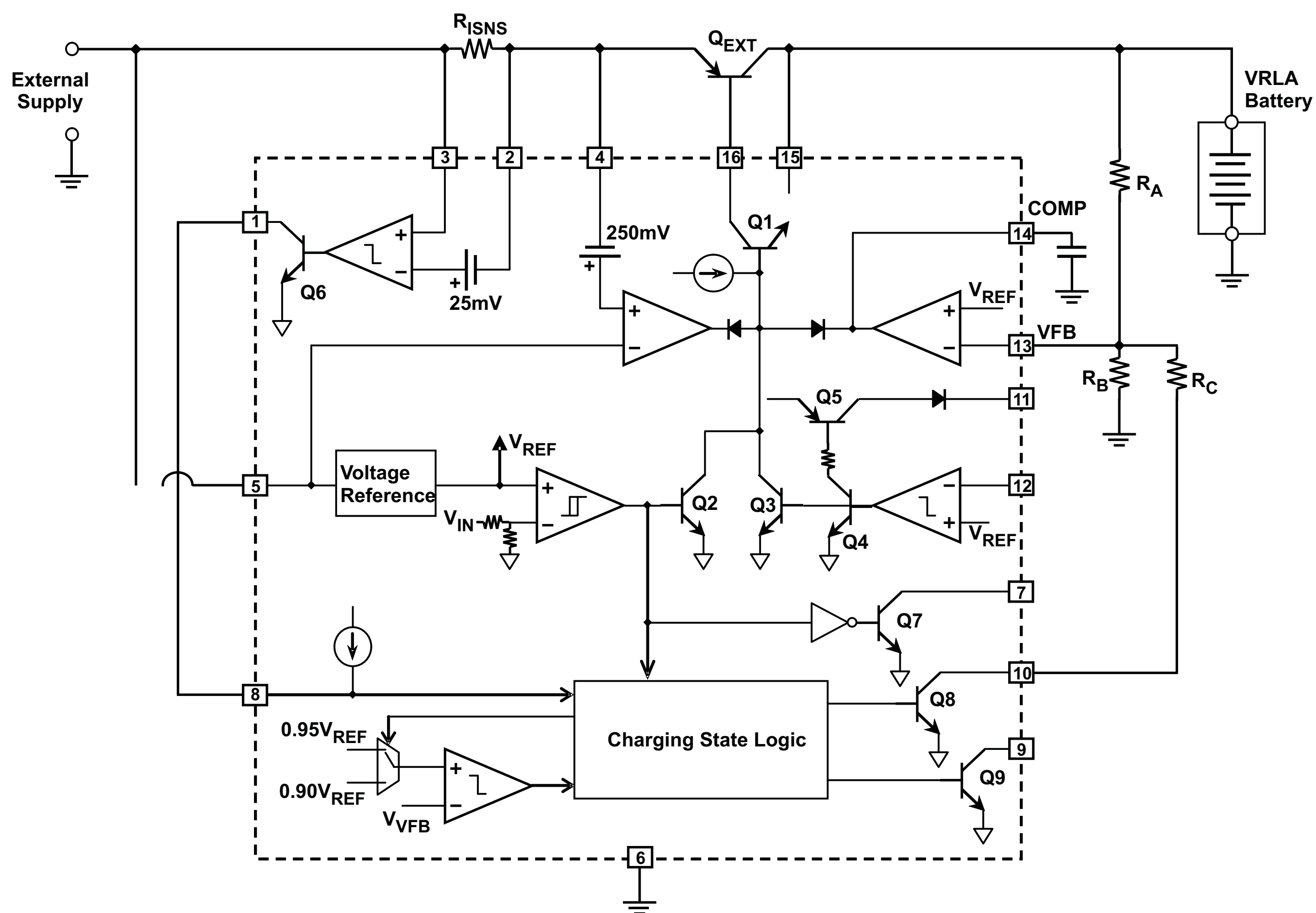
The driver transistor is controlled by a voltage regulating loop and a current limiting

DETAILED OPERATION AND APPLICATION INFORMATION

A Simple Dual-Level Float-Cum-Boost Charger

Figure 4 shows the bq24450 configured as a simple dual-level float-cum-boost charger. Figure 5 shows the sequence of events that occur in a normal charge cycle. At (1) in Figure 5, power is switched ON. As long as the input voltage V_{IN} is below the undervoltage lockout threshold UVLO, Q2 is ON, disabling the driver transistor Q1. As the input voltage V_{IN} ramps up and rises above UVLO Q2 turns OFF. This enables Q1 and thus the external transistor Q_{EXT}. At the same time, Q7 turns ON, latch L1 is forced to RESET and latch L2 is SET (see Figure 2 for the internals of the Charging State Logic).

The voltage regulating amplifier tries to force the voltage at the VFB pin to V_{REF} by turning Q1 and thus Q_{EXT}



As charging proceeds, the voltage at the VFB pin increases further to V_{REF}. At this point, the voltage regulating amplifier prevents the voltage at the VFB pin from rising further, maintaining the battery voltage at V_{BOOST}. [(4) in Figure 4].

$V_{BOOST} = V_{REF} \quad (R_A + R_B//R_C) \quad R_B//R_C$

I_{CHG} keeps flowing into the battery. As the battery approaches full charge, the current into the battery decreases, while the battery terminal voltage is maintained at V_{BOOST}.

At (5), the charging current I_{CHG} reduces to a value I_{TAPER} such that the voltage across R_{ISNS} becomes less than V_{ISNS} (25mV typical)

$I_{TAPER} = V_{ISNS} \quad R_{ISNS}$

Q6 at the output of the current sense comparator turns OFF. The internal current source pulls the BSTOP pin HIGH, latch L1 is forced to SET, in turn forcing L2 to SET. The reference voltage on the voltage sense comparator is now $0.9V_{REF}$. STAT1 turns OFF, and the voltage on the battery settles to:

$V_{FLOAT} = V_{REF} \quad (R_A + R_B) \quad R_B$

As long as the peak load current is less than $I_{MAX\text{-}CHG}$, it will be supplied by Q_{EXT}, and the voltage across the battery will be maintained at V_{FLOAT}. But if the peak load current exceeds $I_{MAX\text{-}CHG}$, the battery will have to provide the excess current, and the battery terminal voltage will drop. Once it drops below $0.9V_{REF}$, at (6) in Figure 4, a new charge cycle is initiated. The battery voltage V_{BAT} at this point, V_{RCH}, is given by:

$V_{RCH} = 0.9V_{REF} \quad (R_A + R_B) / R_B$

Figure 5.

An Improved Dual-Level Float-Cum-Boost Charger with Pre-Charge

The problem with the charger circuit shown in Figure 4 is that even with deeply discharged batteries, charging starts at full current level $I_{MAX-CHG}$. This can sometimes be hazardous, resulting in out-gassing from the battery. The bq24450 can be configured to pre-charge the battery till the voltage levels rise to levels safe enough to per4778sd(i)Tj 2075 -120 Td (MAX-CHG)Tj /F2 10 Tf 38(Figure)Tj 118.440 Td (38RBT/F1 14 Tf 75 Tz 0 0 5e-4 1 54 741.6 Td (i·d (APR

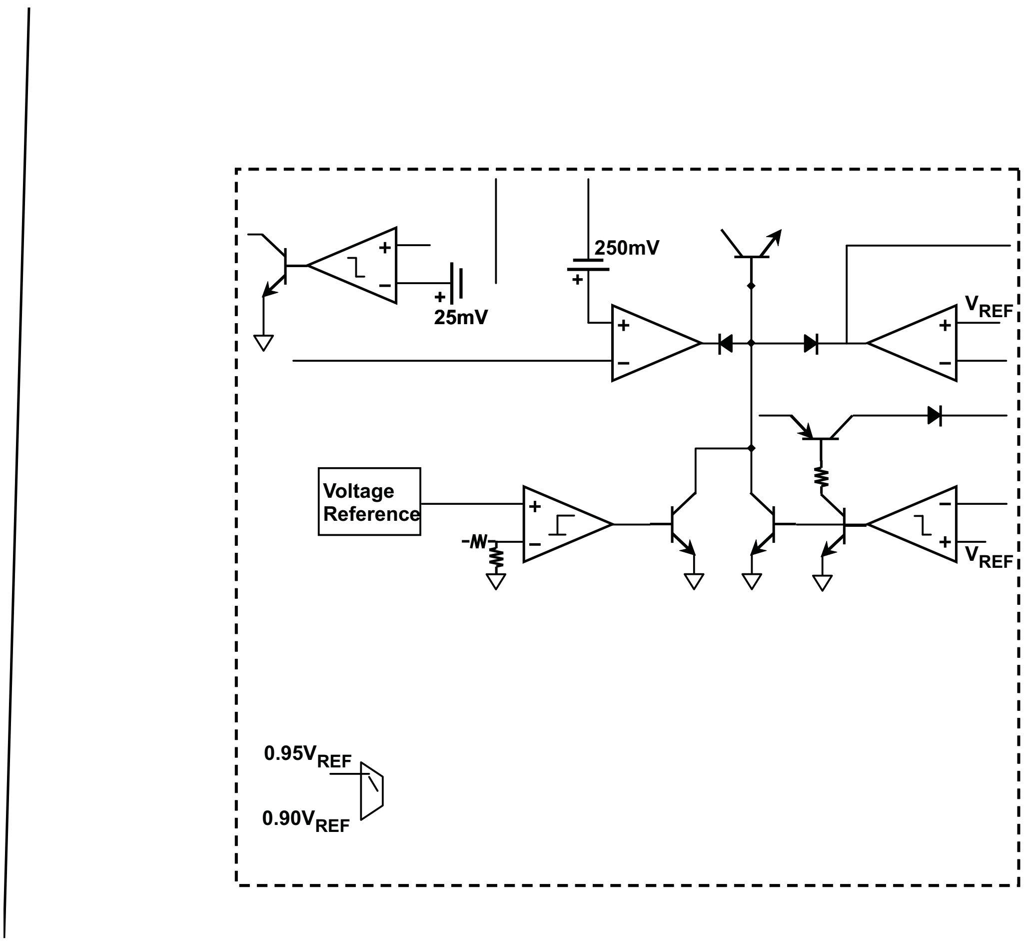


Figure 7.

Further Improvements to the Circuit of Figure 6

In applications where the load current is low, the current through the V_{BAT} voltage divider can be a non-negligible proportion of the load current. Current flowing back thorough Q_{EXT} when the input power is removed constitutes another drainage path. The modifications in Figure 8 fix both these issues.

The addition of D_{EXT} (see Figure 8) fixes the reverse current problem. Returning the voltage feedback divider chain to the PGOOD pin instead of to GND ensures that the divider does not draw any current when the input supply is not present. (When sinking 50 A, the saturation voltage of the PGOOD transistor is typically only 30mV).

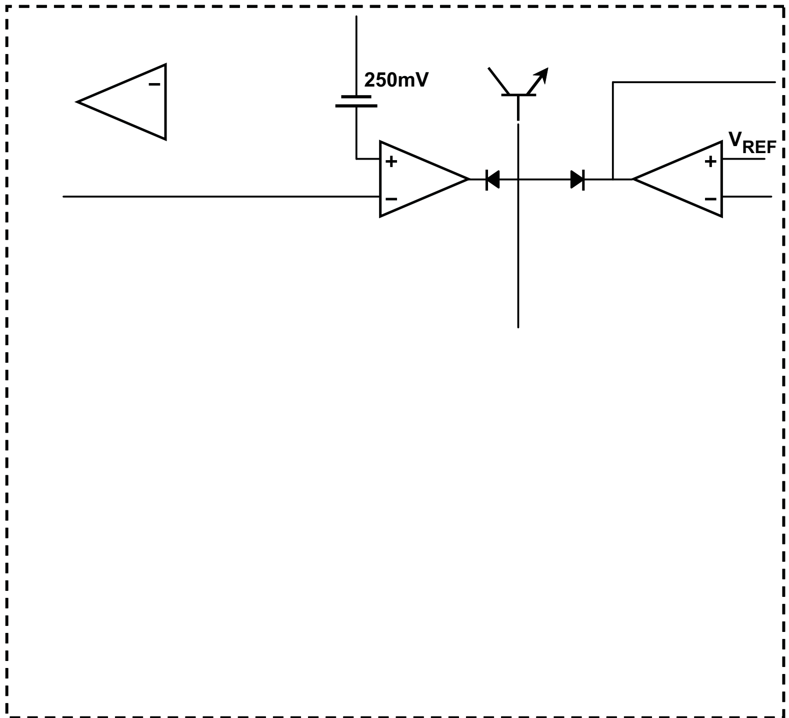
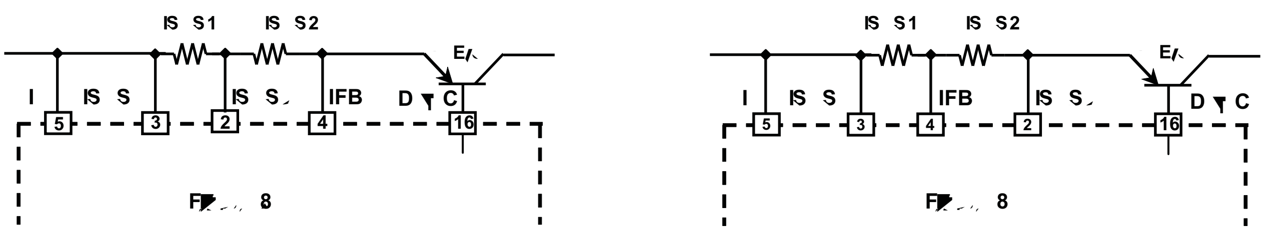


Figure 8.

Changing the value of I_{TAPER} for a given $I_{MAX\text{-}CHG}$

In the examples above, I_{TAPER} is 10% of $I_{MAX\text{-}CHG}$, because V_{ILIM} is 250mV and V_{ISNS} is 25mV (typical values), and the same resistor is used for both, the taper comparator and the current-loop amplifier. In most applications, setting I_{TAPER} to 10% of $I_{MAX\text{-}CHG}$ is perfectly fine. But if, for some reason, a different value of I_{TAPER} is required, it can be achieved, as shown in Figure 9(a) and Figure 9(b).



$I_{MAX\text{-}CHG} = V_{ILIM} \div (R_{ISNS1} + R_{ISNS2})$

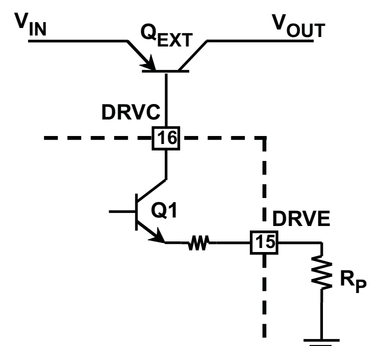
$I_{TAPER} = V_{ISNS} \div R_{ISNS2}$

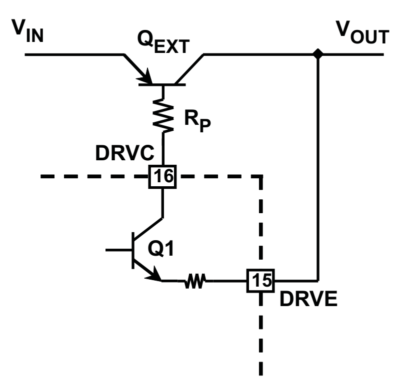
$I_{MAX\text{-}CHG} = V_{ILIM} \div R_{ISNS1}$

$I_{TAPER} = V_{ISNS} \div (R_{ISNS1} + R_{ISNS2})$

Figure 9.

SelectnC


VIN
QEXT
VOUT
DRVC
16
Q1
DRVE
15
RP

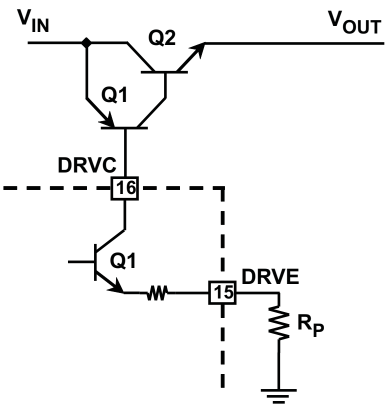

VIN
QEXT
VOUT
RP
DRVC
16
Q1
15
DRVE

External Quasi-Darlington

$I_{MAX\text{-}CHG}$ range: 0.6A to 15A

Minimum V: 1.2V

R_P = ($V_{IN(MIN)}$ 0.7 V) $I_{MAX\text{-}CHG}$ $h_{FE1(MIN)}h_{FE2(MIN)}$
P_D = ($V_{IN(MAX)}$ 0.7 V) (h_{FE1} h_{FE2}) $I_{MAX\text{-}CHG}$ $(I_{MAX\text{-}CHG})^2$ $(h_{FE1}$ $h_{FE2})^2$ R_P
C_{COMP} = 0.22 F with 470 series resistor to GND

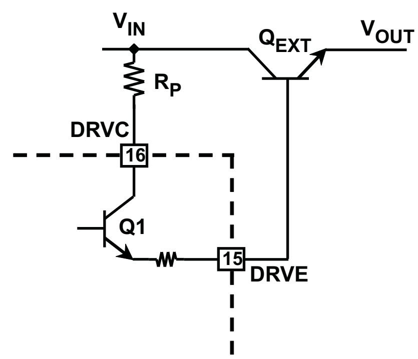


NPN Emitter-Follower

$I_{MAX\text{-}CHG}$ range: 25mA to 1000mA

Minimum V: 2.7V

R_P = ($V_{IN(MIN)}$ $V_{OUT(MAX)}$ 1.2 V) $I_{MAX\text{-}CHG}$ $h_{FE(MIN)}$
P_D = ($V_{IN(MAX)}$ V_{OUT} 0.7 V) h_{FE} $I_{MAX\text{-}CHG}$ $(I_{MAX\text{-}CHG})^2$ $(h_{FE})^2$ R_P
C_{COMP} = 0.01 F to 0.047 F



DESIGN EXAMPLE

This section covers the design of a dual-level charger for a 6V 4Ah sealed lead-acid battery. The application is a system where the battery is used in standby mode, and the load on the battery when it powers the system is 250mA (0.06C).

The battery parameters are (see References 1 and 2)

Final discharge voltage	1.75V per cell	5.25V	V_{TH}
Float voltage	2.30V per cell	6.9V	V_{FLOAT}
Voltage in boost mode	2.45V per cell	7.35V	V_{BOOST}
Charge rate	0.05C to 0.3C	Use 0.15C = 600 mA	$I_{MAX\text{-}CHG}$
$V_{BAT(MIN)}$		4V	
Trickle charge rate		10 mA	

The charger is required to operate from a supply voltage of 9V to 13V. Therefore, the minimum input to output differential is 1.65V. To block reverse current from the battery to the input supply use a blocking diode as in Figure 8. This leaves only 0.65V as the differential across the external transistor, forcing the use of the Common-Emitter PNP topology.

Figure 10 is the schematic for this charger (from Figure 8, with the pass transistor topology changed), with the

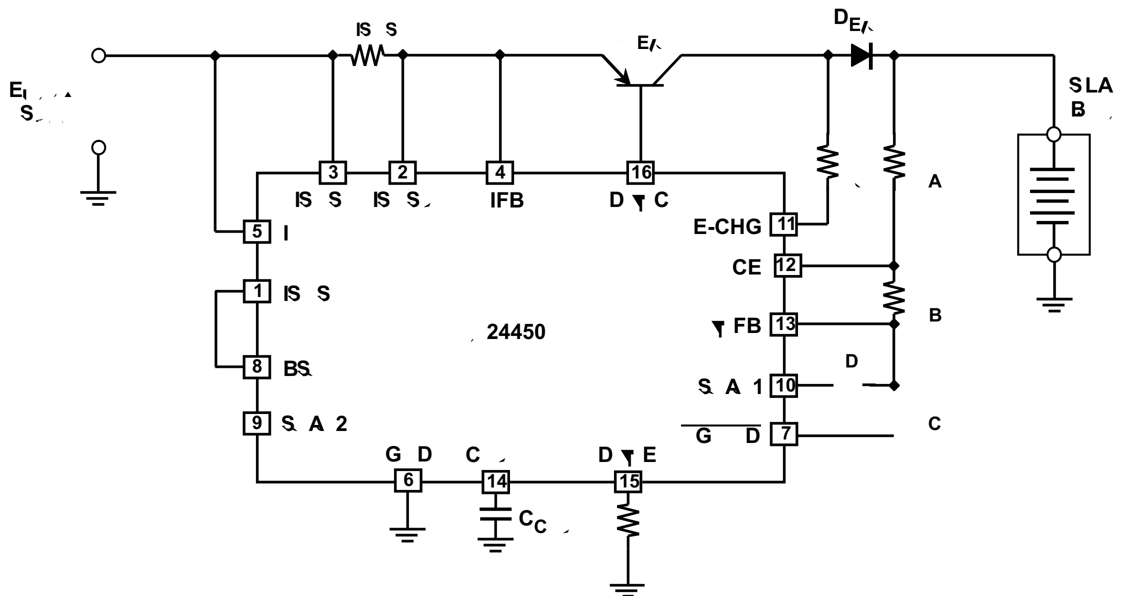


Figure 10.

The first step is to decide on the value of the current in the voltage divider resistor string in FLOAT mode. This should be substantially higher than the input bias current in the CE and VFB pins and the leakage current in the STAT1 pin, but low enough such that the voltage on the PGOOD pin does not introduce errors. A value of 50 A is suitable.

In FLOAT mode, STAT1 is OFF, so there is no current in R_D. The voltage on the VFB pin (V_{REF}) is 2.3V.

R_C = 2.30V   50 A = 46k . The closest 1% value is 46.4k .

V_{FLOAT} = V_{REF} (R_A + R_B + R_C) R_C R_A + R_B = 2

REVISION HISTORY

NOTE: Page numbers of previous versions may differ from current version.

Changes from Original (April 2009) to Revision A **Page**

- Deleted PDIP package option from Features 1
- Deleted PDIP package from Ordering Information table 2
- Changed equations to correct typo/formatting errors (3 equations) 8
- Changed equations to correct typo/formatting errors 9
- Changed equation to correct typo/formatting errors 10
- Changed three equations to correct typo/formatting errors 15
- Changed component values in Design Example calculations. 15

Changes from Revision A (January 2010) to Revision B **Page**

- Added V_{PRE} with definition 10
- Changed compenent values in the I_{PRE} calculations 15

Changes from Revision B (October 2010) to Revision C **Page**

- Changed compenent values in the I_{PRE} calculations in FLOAT mode description..... FROM 332 TO 634 ; FROM 5) /332 = 16mA TO 4)/634 = 10mA 15

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ24450DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
BQ24450DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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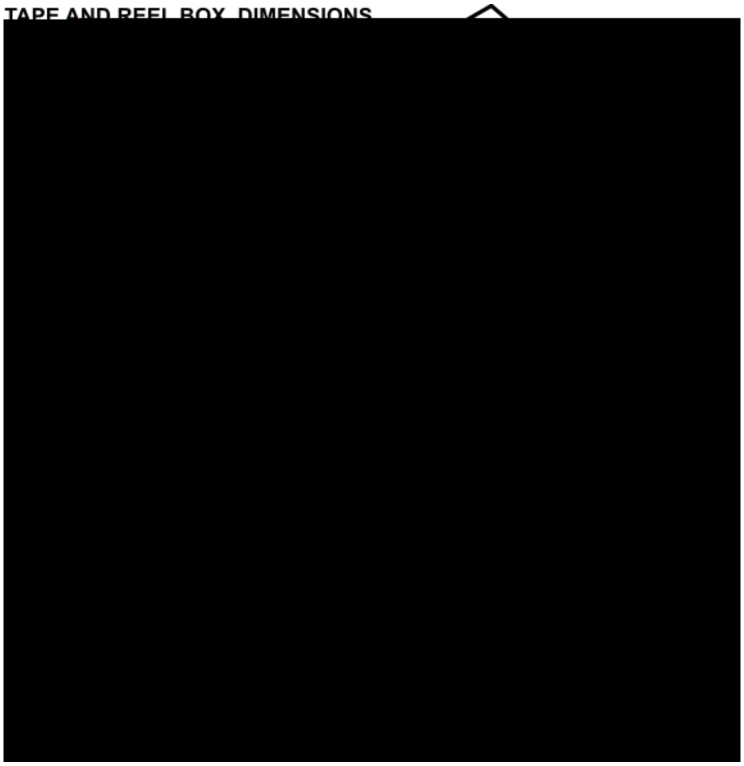
TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ24450DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

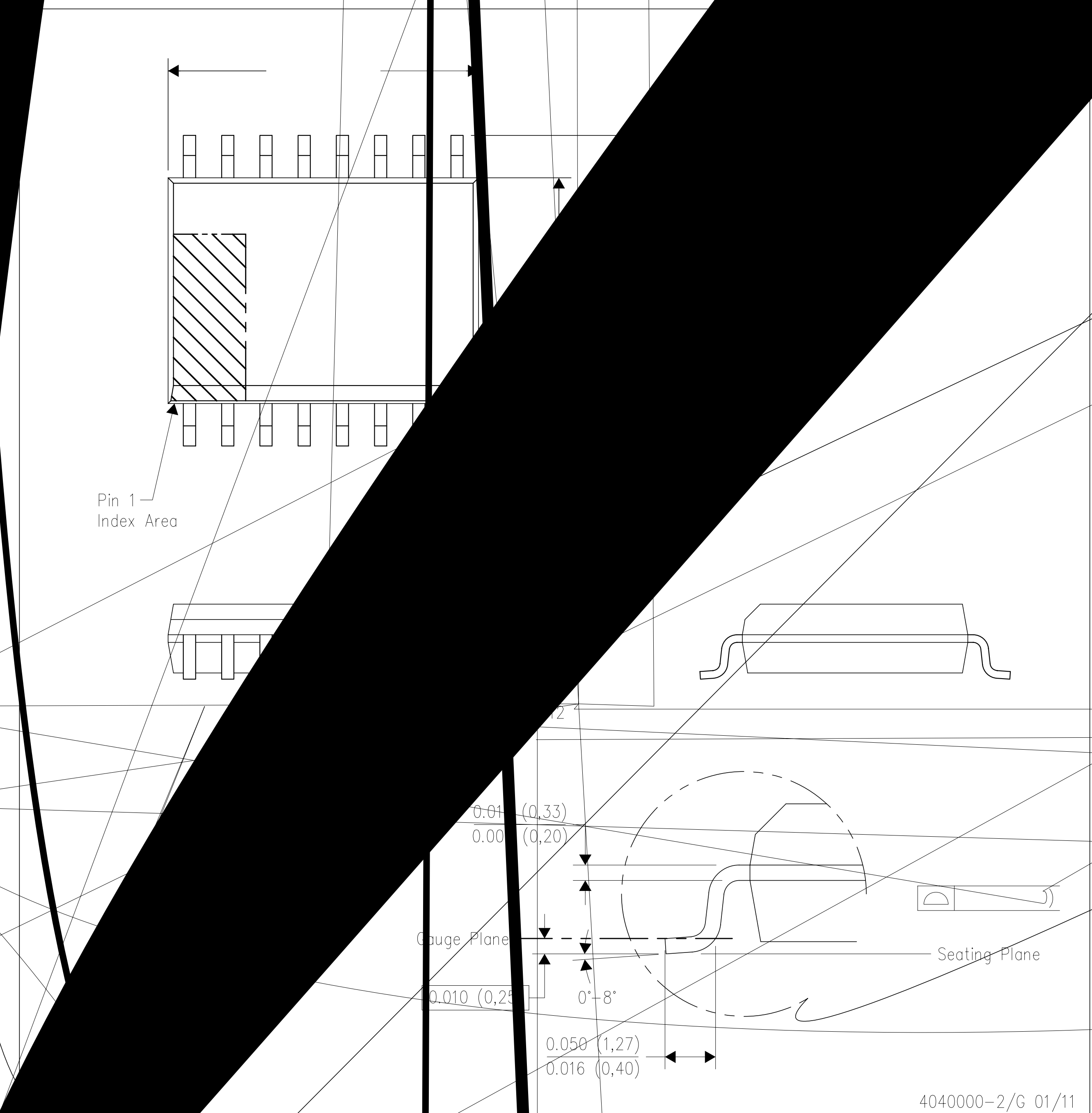
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

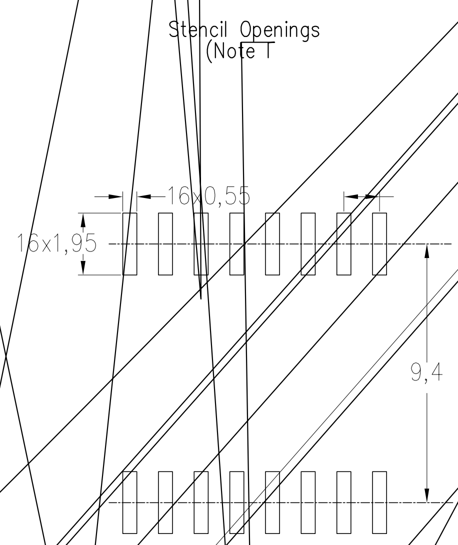
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24450DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

[redacted] (R-PDSO-G16)



[redacted] drawing is subject to change without notice.
[redacted] dimensions do not include mold [redacted] not to exceed 0.006 (0,15).
[redacted] Falls [redacted] MS-013 variation AA.

DW[redacted] PLASTIC SMALL OUTLINE



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NO[redacted]

[redacted] so rounding corners will offer better paste re
[redacted] recomm
[redacted] e for solder mask tolerances between and around signal pads.

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