3-Phase Brushless Motor Driver

Check for Samples: DRV3202-Q1

FEATURES

- **3-Phase Pre-drivers for N-channel MOS Field Effect Transistors (MOSFETs)**
- **Pulse Width Modulation (PWM) Frequency up to 20 kHz**
- **Fault Diagnostics**
- **Charge Pump**
- **Phase Comparators**
- **Phase Monitoring Sample and Hold Op-Amps**
- **Central Processing Unit (CPU) Reset Generator**
- **Serial Port I/F (SPI)**
- **Motor Current Sense**
- **80-pin HTQFP**
- **Controller Area Network (CAN)**
- **5-V Regulator**

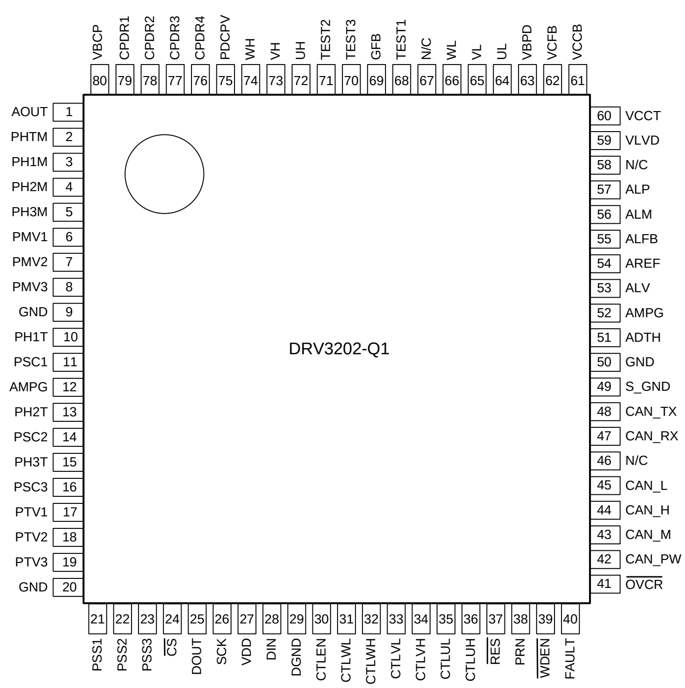
APPLICATIONS

- **Automotive**

DESCRIPTION

The DRV3202-Q1 device is a field effect transistor (FET) pre-driver designed for 3-phase motor control and its application such as an oil pump or a water pump. It is equipped with three high-side pre-FET drivers and three low-side drivers which are controlled by an external microcontroller (MCU). The power for the high side is supplied by a charge pump and no bootstrap cap is needed. For commutation, this integrated circuit (IC) sends a conditional motor drive signal and output to the MCU. Diagnostics provide undervoltage, overvoltage, overcurrent, overtemperature and power bridge faults. The motor current can be measured using an integrated current sense amplifier and comparator in a battery common-mode range, which allows the motor current to be used in a high-side current sense application. Gain is attained by external resistors. If the MCU does not have enough bandwidth, the phase monitoring sample and hold amplifiers can hold phase information until the MCU is ready to process it. The interfaces include SPI and CAN. The pre-driver and other internal settings can be configured through the SPI. The CAN is used to communicate with other electronic control units (ECUs).

PIN OUT



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN FUNCTIONS

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
1	AOUT	O	–0.3–6 V	Test mode output
2	PHTM	I	–1–40 V	Phase comparator reference input
3	PH1M	I	–1–40 V	Phase comparator input
4	PH2M	I	–1–40 V	Phase comparator input
5	PH3M	I	–1–40 V	Phase comparator input
6	PMV1	O	–0.3–6 V	Phase comparator output
7	PMV2	O	–0.3–6 V	Phase comparator output
8	PMV3	O	–0.3–6 V	Phase comparator output
9, 20, 50	GND	I	–0.3–0.3 V	GND
10	PH1T	I	–2–40 V	Phase amplifier input
11	PSC1	O	–0.3–6 V	Sample and hold filter output
12	AMPG	I	–0.3–0.3 V	Quiet GND
13	PH2T	I	–2–40 V	Phase amplifier input
14	PSC2	O	–0.3–6 V	Sample and hold filter output
15	PH3T	I	–2–40 V	Phase amplifier input
16	PSC3	O	–0.3–6 V	Sample and hold filter output
17	PTV1	O	–0.3–6 V	Phase amplifier output
18	PTV2	O	–0.3–6 V	Phase amplifier output
19	PTV3	O	–0.3–6 V	Phase amplifier output
21	PSS1	I	–0.3–6 V	Sample and hold control signal input
22	PSS2	I	–0.3–6 V	Sample and hold control signal input
23	PSS3	I	–0.3–6 V	Sample and hold control signal input
24	$\overline{CS}$	I	–0.3–6 V	SPI chip select
25	DOUT	O	–0.3–6 V	SPI data output
26	SCK	I	–0.3–6 V	SPI clock
27	VDD	O	–0.3–3.6 V	Digital supply output
28	DIN	I	–0.3–6 V	SPI data input
29	DGND	I	–0.3–0.3 V	Digital GND
30	CTLEN	I	–0.3–6 V	Pre-driver parallel enable input
31	CTLWL	I	–0.3–6 V	Pre-driver parallel input
32	CTLWH	I	–0.3–6 V	Pre-driver parallel input
33	CTLVL	I	–0.3–6 V	Pre-driver parallel input
34	CTLVH	I	–0.3–6 V	Pre-driver parallel input
35	CTLUL	I	–0.3–6 V	Pre-driver parallel input
36	CTLUH	I	–0.3–6 V	Pre-driver parallel input
37	$\overline{RES}$	O	–0.3–6 V	Reset output
38	PRN	I	–0.3–6 V	Pulse input
39	$\overline{WDEN}$	I	–0.3–6 V	Reset generator enable input
40	FAULT	O	–0.3–6 V	Diagnosis output
41	$\overline{OVCR}$	I	–0.3–6 V	Over current reset input
42	CAN_PW	I	–0.3–6 V	CAN supply input
43	CAN_M	O	–27–40 V	CAN transceiver middle point terminal

PIN FUNCTIONS (continued)

PIN			MAX RATING	FUNCTION
NO.	NAME	TYPE		
44	CAN_H	IO	–27–40 V	CAN transceiver positive terminal
45	CAN_L	IO	–27–40 V	CAN transceiver negative terminal
46, 58, 67	N/C	—	—	Not connected
47	CAN_RX	O	–0.3–6 V	CAN digital output
48	CAN_TX	I	–0.3–6 V	CAN digital input
49	S_GND	I	–0.3–0.3 V	CAN GND
51	ADTH	I	–0.3–6 V	Motor overcurrent threshold input
52	AMPG	I	–0.3–0.3 V	Quiet GND
53	ALV	O	–0.3–6 V	Motor current sense amp output
54	AREF	O	–0.3–40 V	Motor current sense reference output
55	ALFB	O	–0.3–40 V	Motor current sense amp feedback
56	ALM	I	–0.3–40 V	Motor current sense amp negative input
57	ALP	I	–0.3–40 V	Motor current sense amp positive input
59	VLVD	I	–0.3–6 V	V_{CC} undervoltage threshold input
60	VCCT	I	–0.3–6 V	V_{CC} supply input
61	VCCB	O	–0.3–40 V	V_{CC} regulator base drive for PNP external transistor
62	VCFB	I	–0.3–40 V	V_{CC} regulator current sense input
63	VBPD	I	–0.3–40 V	VB input
64	UL	O	-0.3–20 V	Pre-driver output
65	VL	O	-0.3–20 V	Pre-driver output
66	WL	O	-0.3–20 V	Pre-driver output
68	TEST1	I	–0.3–6 V	Test input
69	GFB	I	–0.3–0.3 V	Power GND
70	TEST3	I	-0.3–20 V	Test input
71	TEST2	I	–0.3–6 V	Test input
72	UH	O	–0.3–40 V	Pre-driver output
73	VH	O	–0.3–40 V	Pre-driver output
74	WH	O	–0.3–40 V	Pre-driver output
75	PDCPV	O	–0.3–40 V	Charge pump output
76	CPDR4	O	–0.3–40 V	Charge pump output
77	CPDR3	O	–0.3–40 V	Charge pump output
78	CPDR2	O	–0.3–40 V	Charge pump output
79	CPDR1	O	–0.3–40 V	Charge pump output
80	VBCP	I	–0.3–4 0V	VB input

BLOCK DIAGRAM

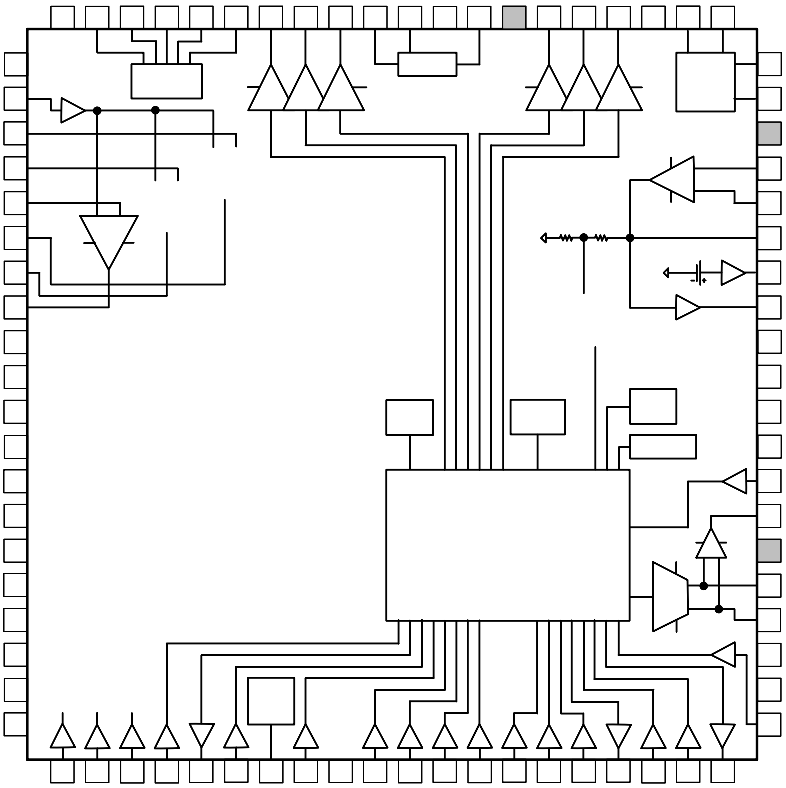


Figure 1. Top Block Diagram

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNITS
ESD (1)					
ESD all pins	ESD performance of all pins to any other pin	HBM model	–2	2	kV
		CDM model	–500	500	V
TEMPERATURE					
T_A	Operating temperature range		-40	125	degree
T_J	Junction temperature		-40	150	degree
T_s	Storage temperature		–55	150	degree

(1) ESD testing is performed according to the ACE-Q100 standard.

THERMAL INFORMATION

THERMAL METRIC[1]		DRV3202-Q1 HTQP (80-PIN)	UNIT
JA	Junction-to-ambient thermal resistance	23.0	°C/W
JCtop	Junction-to-case (top) thermal resistance	7.5	
JB	Junction-to-board thermal resistance	7.6	
JT	Junction-to-top characterization parameter	0.2	
JB	Junction-to-board characterization parameter	7.4	
JCbot	Junction-to-case (bottom) thermal resistance	0.3	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

SUPPLY VOLTAGE AND CURRENT

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
SUPPLY INPUT						
VB	VB Supply voltage		5.3	12	18	V
I_{VB}	VB Operating current	VB = 5.3 ~18 V, CAN_TX = High, No PWM		20	35	mA

WATCHDOG

Description

The watchdog monitors the PRN signal and V_{CC} supply level and generates a reset to the MCU through the $\overline{\text{RES}}$ pin if the status of the PRN is not normal or the V_{CC} is lower than the specified threshold level. The watchdog can be disabled if $\overline{\text{WDEN}}$ is set high.

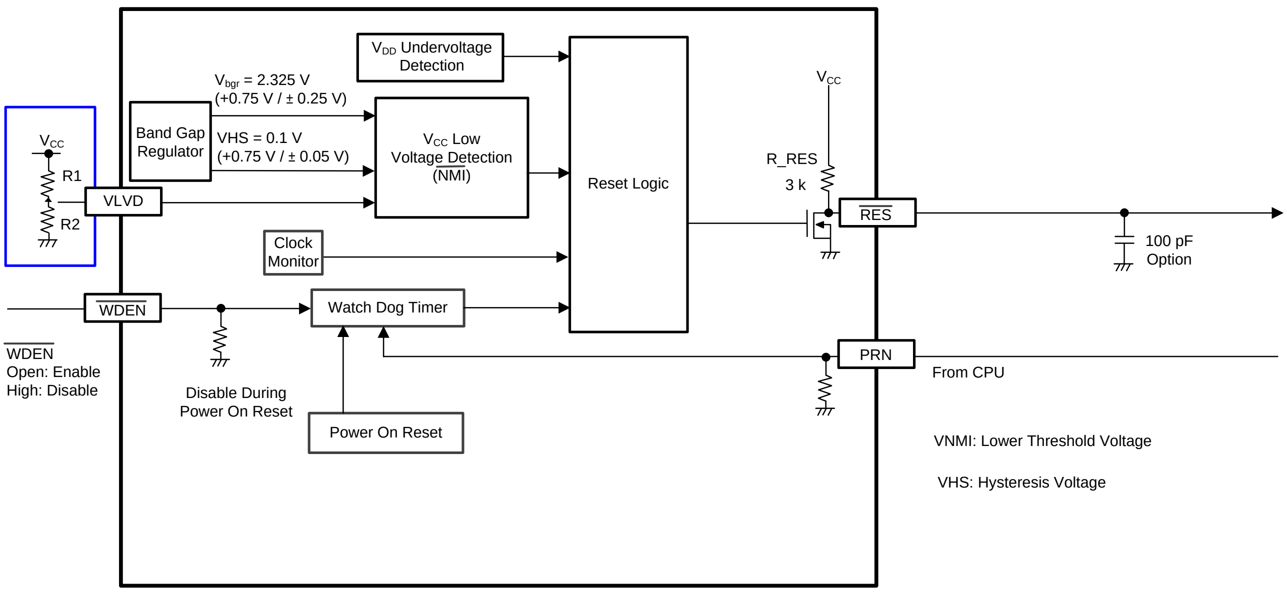
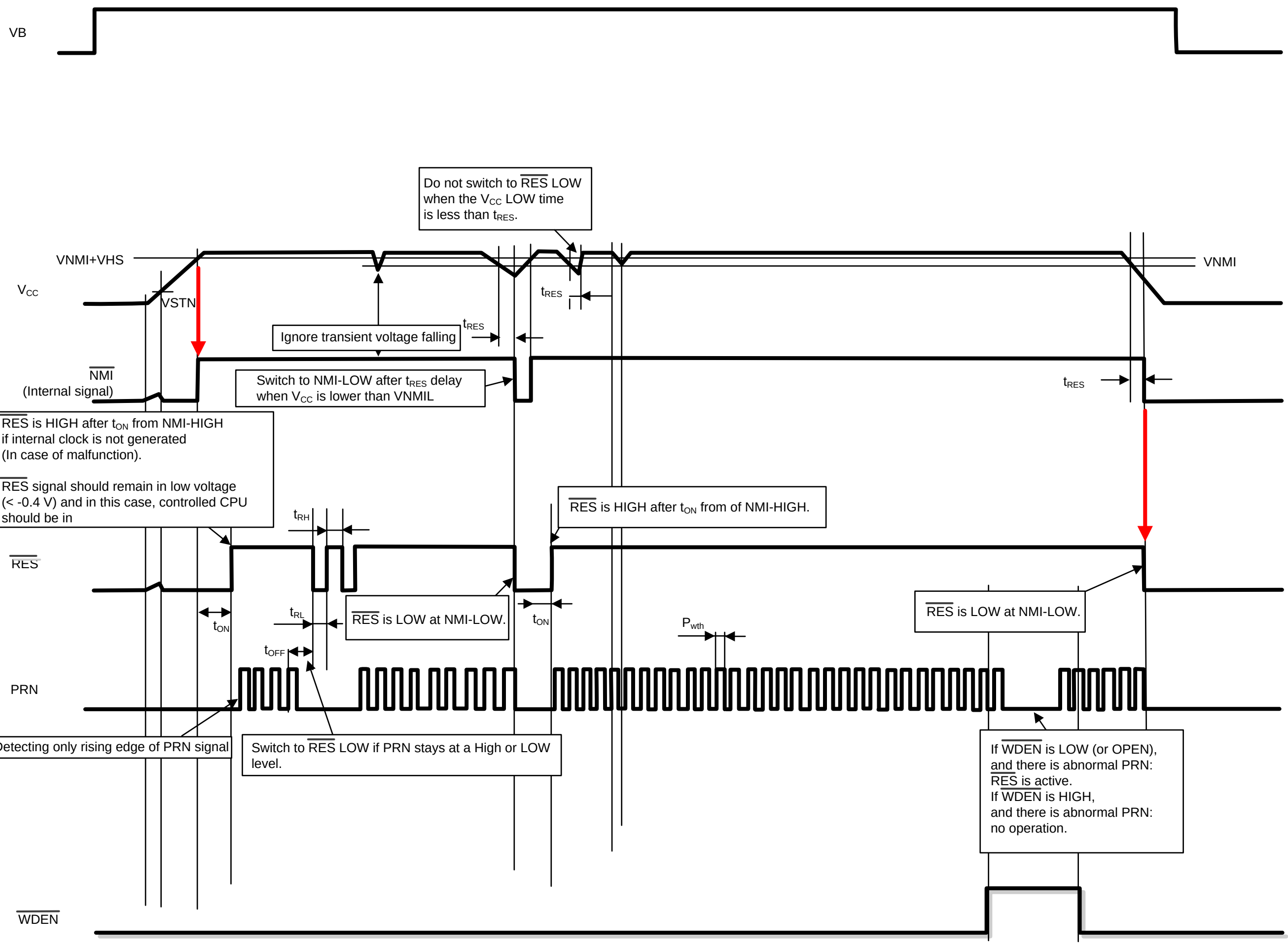


Figure 2. Watchdog Block Diagram



NOTE: $\overline{\text{WDEN}}$ = High, V_{CC} undervoltage condition sets $\overline{\text{RES}}$ = Low

Figure 3. Watchdog Timing Chart

WATCHDOG ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER(2)	CONDITIONS	MIN	

ELECT16.7 1.8 Td 5 0 Td (condition)T

SERIAL PORT I/F

Description

The SPI is used to receive an input byte from CPU and to transmit an output byte to CPU. Four signals are utilized according to the timing chart of Figure 4.

Figure 4. Block Diagram of SPI

- **$\overline{\text{CS}}$ – Chip Select**
  - This input signal is utilized to select this IC by CPU.
  - This input signal is normally high and the communication is possible only when it is forced low.
  - When this input signal falls, the communication between this IC and the CPU starts.
  - Transmitted data is latched and the DOUT pin comes out of high impedance.
  - When this input signal rises, the communication stops.
  - The DOUT pin goes into high impedance. Then, the internal input register updates with the received bits (only if the clock pulse numbers are right and the key bit of the DIN signals is correct).
  - The next falling edge starts another communication.
  - There is a minimum waiting time between two communications (T_{wait}).
  - The pin has an internal pullup.
- **SCK – Synchronization Serial Clock**
  - This input signal is utilized to synchronize the communication by CPU.
  - It is normally high and the correct clock pulse number is 16.
  - At each falling edge, the CPU writes a new bit on the DIN input and this IC writes a new bit on the DOUT pin. At each rising edge, this IC reads the new bit on the DIN pin and the CPU reads the new bit on the DOUT pin.
  - The maximum clock frequency is 4 MHz.
  - The pin has an internal pullup.
- **DIN – Serial Input Data**

  - This input signal is used to receive 16-bit data.
  - The bits are received in order from the MSB (first) to the LSB (last).
  - The pin has an internal pullup.
- **DOUT – Serial Output Data**
  - This output signal is used to transmit 16-bit data.
  - It is a 3-state output and it is in high impedance mode when $\overline{CS}$ is high.
  - The serial data bits are transmitted in order from the MSB (first) to the LSB (last).

SPI ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER[1]		CONDITIONS	MIN	TYP	MAX	UNITS
SPI						
F_{op}	Operating frequency	Refer to Figure 6	DC	–	4	MHz
T_{lead}	Enable lead time		100	–	–	ns
T_{wait}	Wait time between two successive communications		5	–	–	µs
T_{lag}	Enable lag time		100	–	–	ns
T_{pw}	SCLK pulse width		100	–	–	ns
T_{su}	Data setup time		80	–	–	ns
T_h	Data hold time		80	–	–	ns
T_{dis}	Disable time		–	–	80	ns
T_{del}	Data delay time (SCK to DOUT)	C_L = 50 pF, Refer to Figure 6	–	–	80	ns

(1) Specified by design

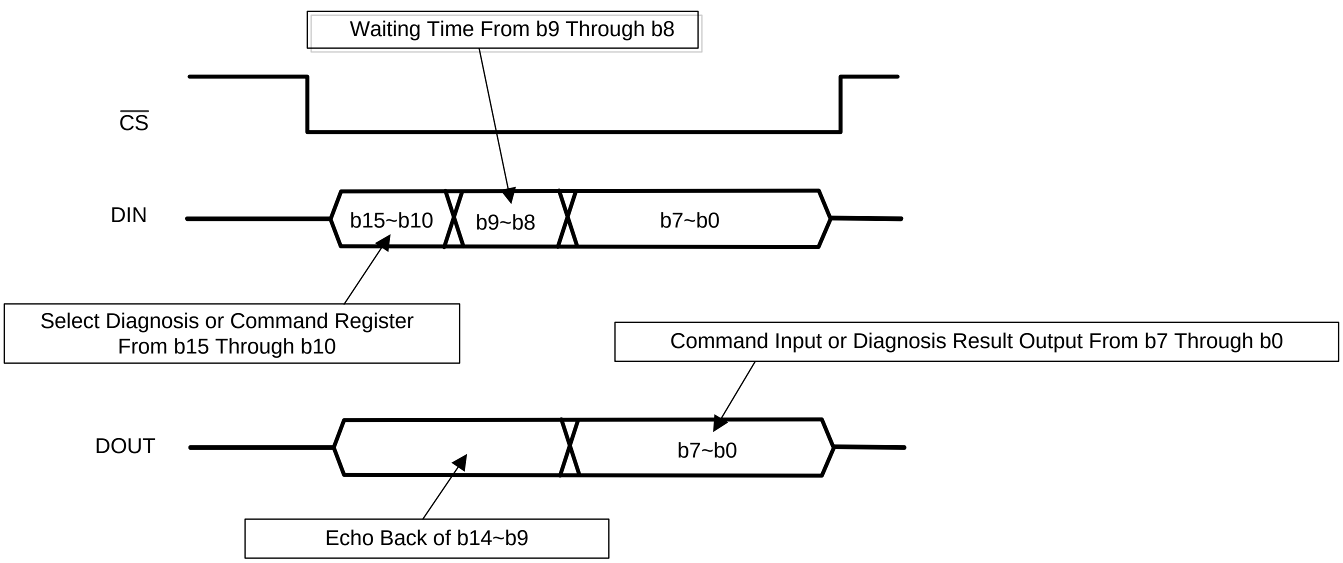


Figure 5. SPI Bit Sequence

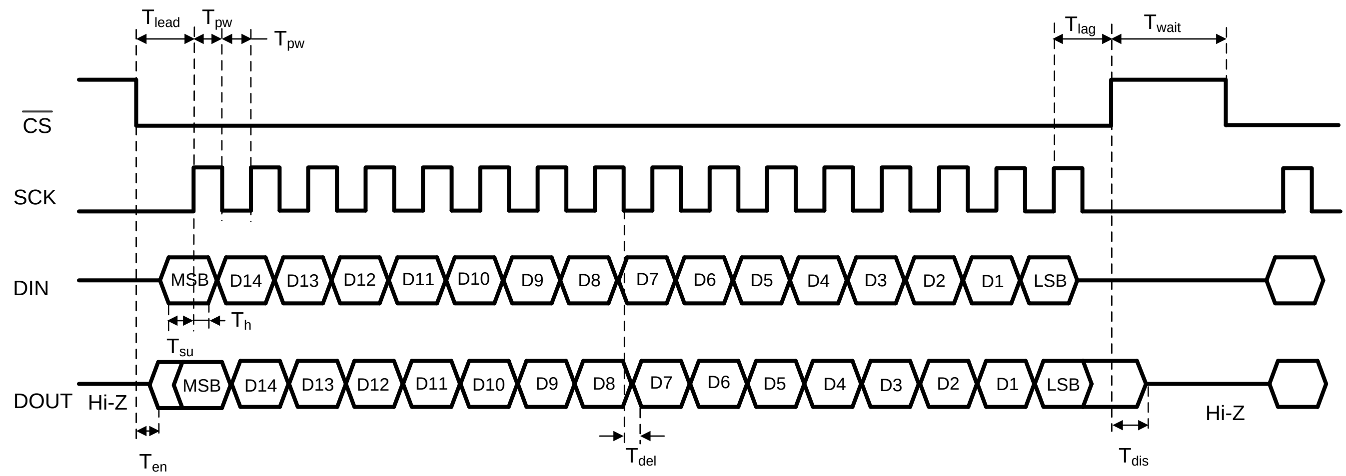


Figure 6. SPI AC Timing Definitiose 0 0 0 rg f 529.4 479.3 28.5 0.35 0.3 re 0 0 0 rg f

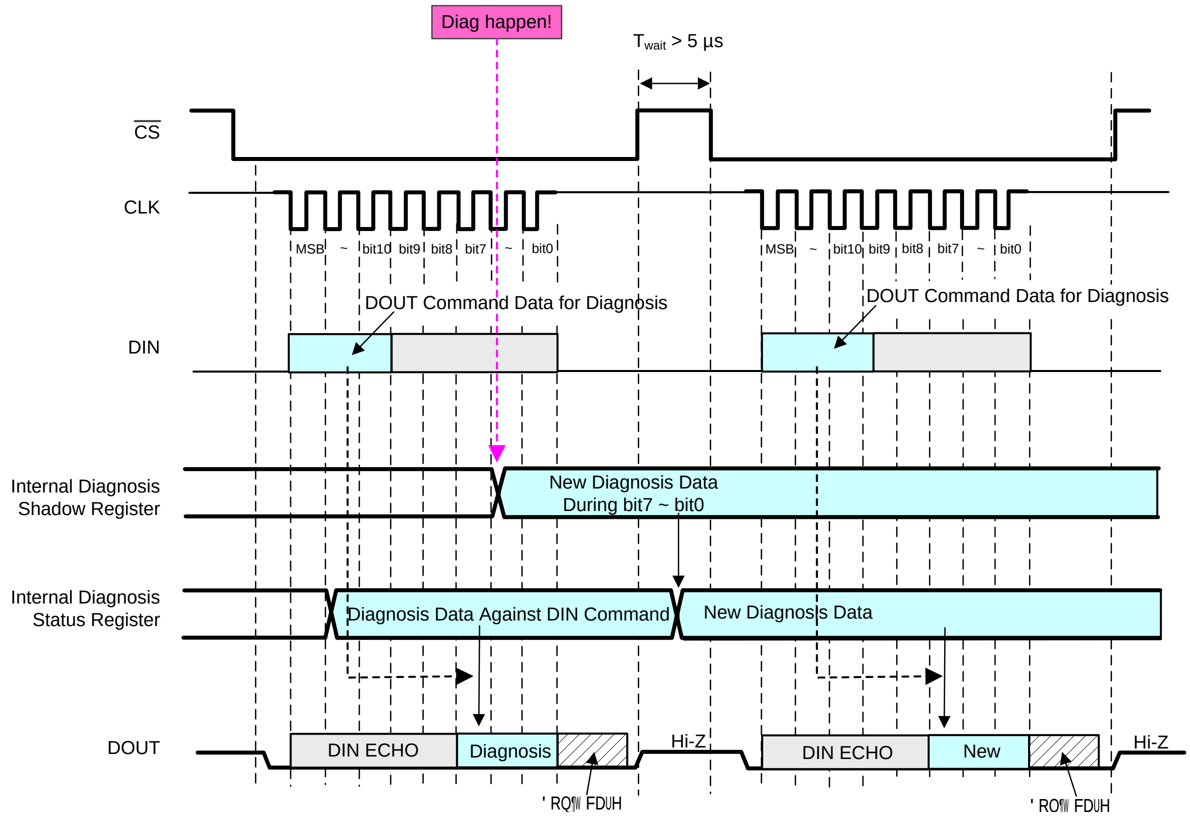


Figure 7. DIAG_READ

Internal Diagnosis Register (Status Register and Shadow Register)

If the diagnosis happens during the SPI communication, the function follows this protocol:

The diagnosis information is stored in the shadow register when the diagnosis happens.

After the output of the previous information a new diagnosis is sent from the shadow to the status register, and both registers are output through the DOUT pin.

In this case, a FAULT signal continues to be output until a new diagnosis is read by the CPU.

All diagnosis bits read by the DIAG_READ1 command happen before the $\overline{CS}$ falling edge. So, all the diagnosis events that happen right after the $\overline{CS}$ falling edge are not read by the current DIAG_READ1 command, instead they are read by the next DIAG_READ1 command.

CAN

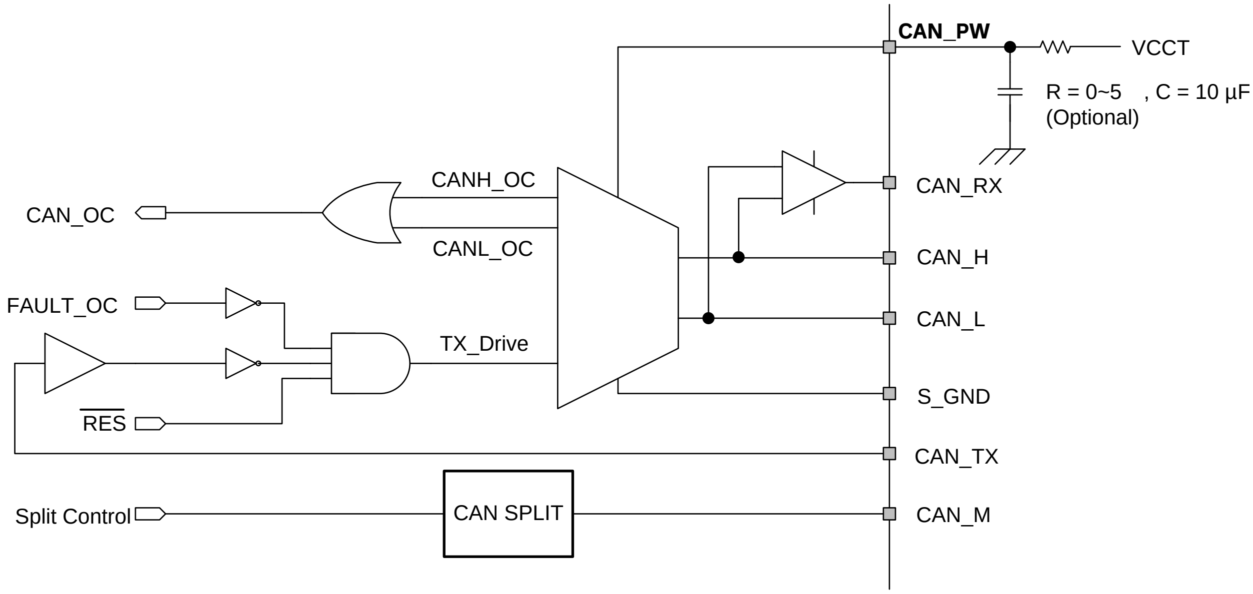


Figure 8. CAN Block Diagram

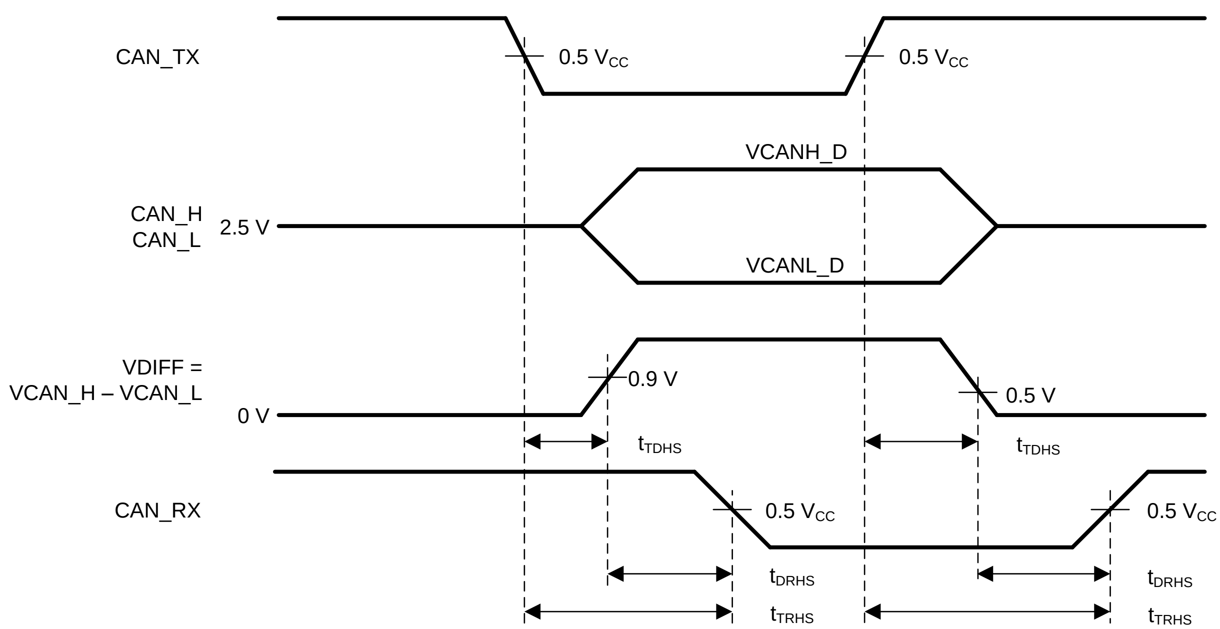
Description

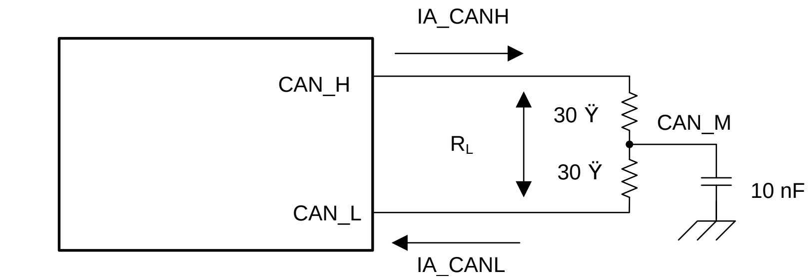
The CAN data from CAN control logic is transmitted to other systems through the CAN bus. The receiver compares the CAN_H–CAN_L voltage levels against an internally generated reference and the result is output through CAN_TX. It has overcurrent protection, shown in Figure 12.

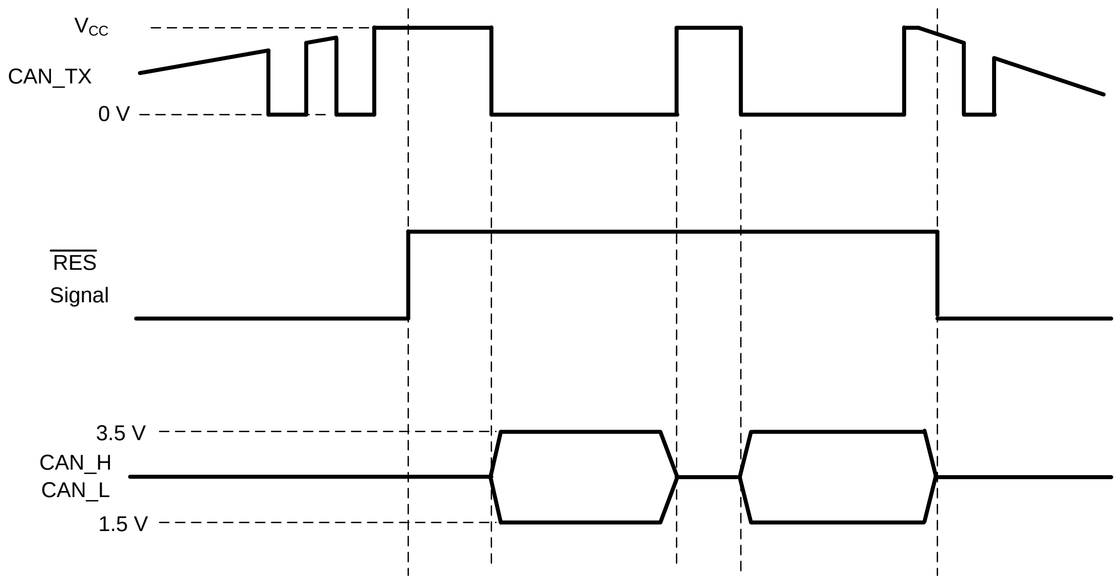
CAN ELECTRICAL CHARACTERISTICS

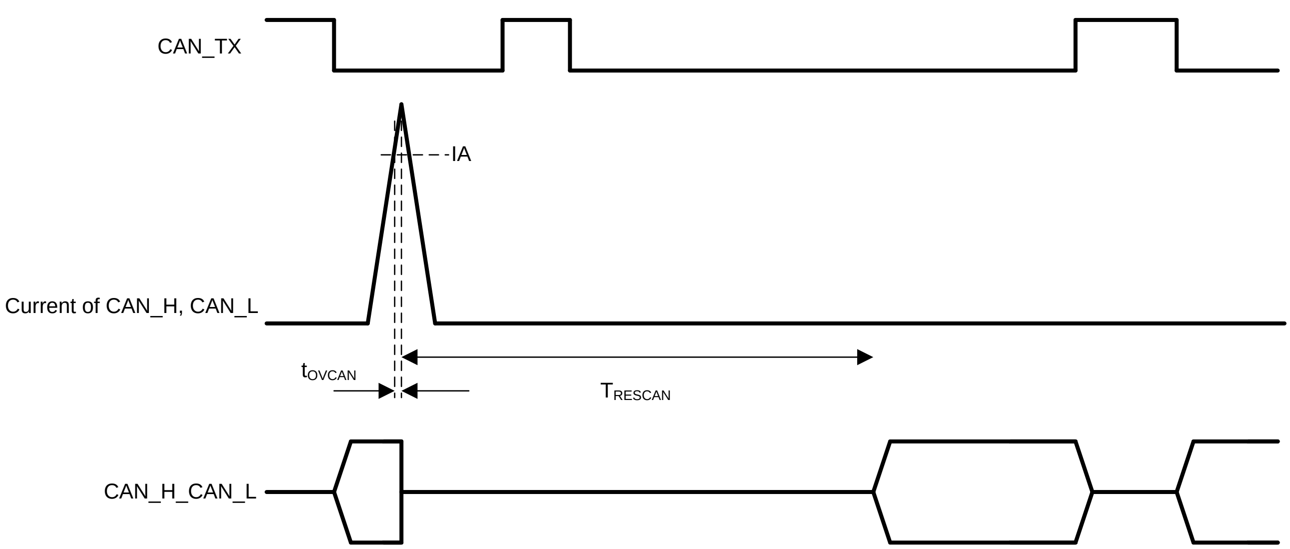
VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CAN (TRANSMITTER SECTION)						
VCAN_H	Bus voltage recessive	CAN_TX = V_{CC}, I_{CANH} = I_{CANL} = 0, see Figure 9	2	2.5	3	V
VCAN_L	Bus voltage recessive		2	2.5	3	V
VDIFF = (VCAN_H – VCAN_L)	Differential output voltage		–500	0	50	mV
VCAN_H	Bus voltage recessive 2	CAN_TX = VCCRL = 60 between CAN_H and CAN_L, see Figure 9 and Figure 10	2.25	2.5	2.75	V
VCAN_L	Bus voltage recessive 2		2.25	2.5	2.75	V
VCANH_D	Dominant state CAN_H output voltage	CAN_TX = 0 V, R_L = 60 between CAN_H and CAN_L, see Figure 9	2.75	3.5	4.5	V
VCANL_D	Dominant state CAN_L output voltage		0.5	1.5	2.25	V
VDIFF = (VCANH_D – VCANL_D)	Differential output voltage	CAN_TX = 0 V, R_L = 60 between CAN_H and CAN_L	1.5	2	3	V
IA_CANH	CAN_H short circuit threshold current	CAN_TX = 0 V	70	–	160	mA
IA_CANL	CAN_L short circuit threshold current	CAN_TX = 0 V	70	–	160	mA
t_{OVCAN}	Overcurrent to output switch-off delay	Refer to Figure 12	200			ns
T_{RESCAN}	Self recovery time	Refer to Figure 12	8	25	50	µs
CAN (RECEIVER SECTION)						
V_{DOM}	Differential input voltage for dominant state (VDIFF = VCAN_H – VCAN_L)	VCAN_L = –12 V to 12 V, CAN_TX = V_{CC}	900			mV
V_{REC}	Differential input voltage for recessive state (VDIFF = VCAN_H – VCAN_L)	VCAN_L = –12 V to 12 V, CAN_TX = V_{CC}			500	mV
V_{hys}	Differential input hysteresis		80	150	–	mV
V_{com} = (VCAN_H - VCAN_L) / 2	Input common mode voltage range		–12	–	12	V


CAN_TX
0.5 VCC
0.5 VCC
VCANH_D
CAN_H
CAN_L
2.5 V
VCANL_D
VDIFF =
VCAN_H – VCAN_L
0 V
0.9 V
0.5 V
tTDHS
tTDHS
CAN_RX
0.5 VCC
0.5 VCC
tDRHS
tDRHS
tTRHS
tTRHS


IA_CANH
CAN_H
30 Ÿ
CAN_M
R_L
30 Ÿ
10 nF
CAN_L
IA_CANL


V_{CC}
CAN_TX
0 V
RES
Signal
3.5 V
CAN_H
CAN_L
1.5 V


CAN_TX
IA
Current of CAN_H, CAN_L
t_{OVCAN}
T_{RESCAN}
CAN_H_CAN_L

CHARGE PUMP

Description

The charge pump block generates the supply for high-side and low-side pre-drivers to maintain the gate voltage on the external FETs. External storage cap (CCP) and bucket caps (C1, C2) are used to support pre-driver slope and switching frequency requirements. R1 and R2 can reduce switching current if required. The charge pump has a voltage supervisor for over and undervoltage, and a selectable stop condition for pre-drivers.

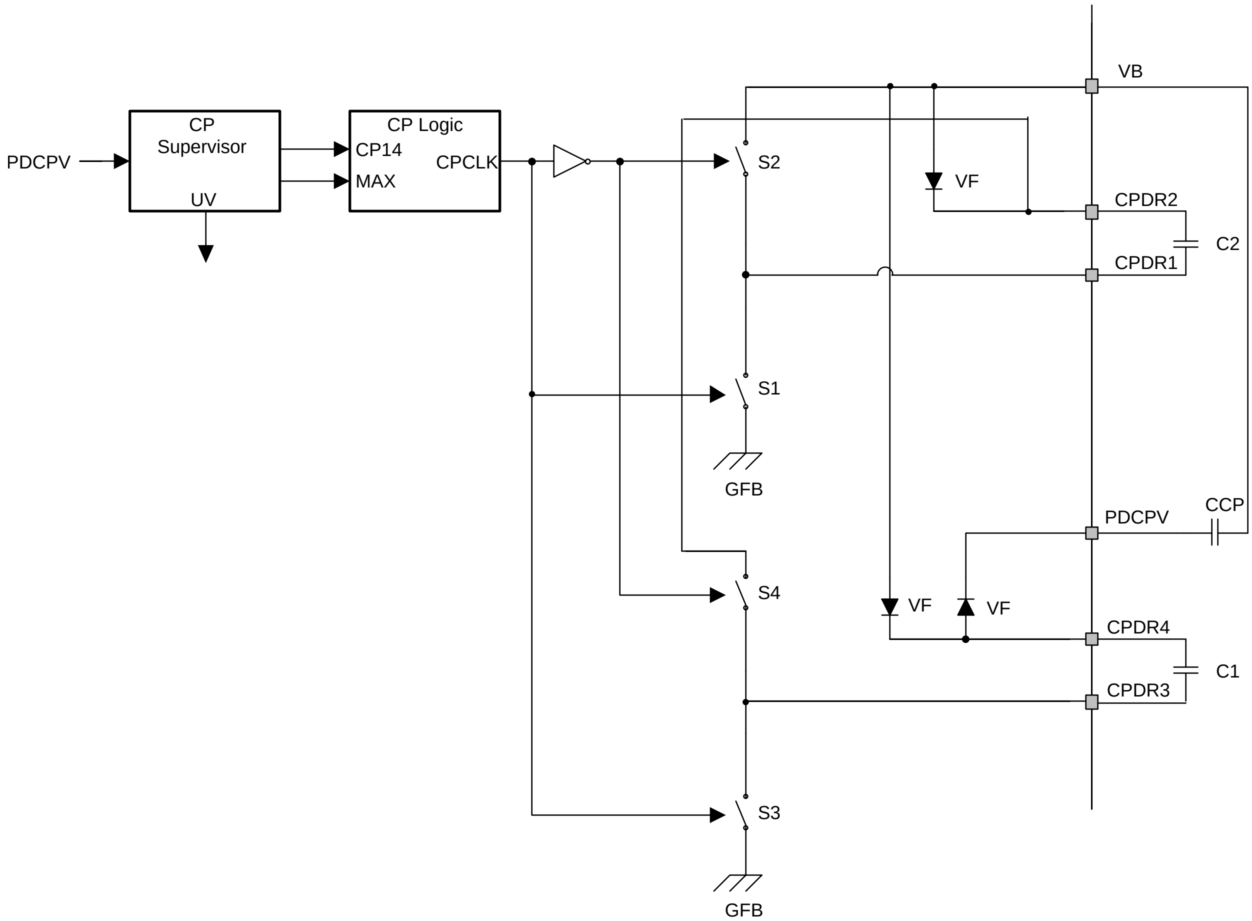


Figure 13. Charge Pump Block Diagram

CHARGE PUMP ELECTRICAL CHARACTERISTICS[1]

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
CHARGE PUMP						
V_{chv1_0}	Output voltage	VB = 5.3 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 7	VB + 8	VB + 9	V
V_{chv1_1}		VB = 5.3 V, I_{load} = 5 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 6	VB + 7	VB + 8	V
V_{chv1_2}		VB = 5.3 V, I_{load} = 8 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 5	VB + 6	VB + 7	V
V_{chv2_0}		VB = 12 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv2_1}		VB = 12 V, I_{load} = 11 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv2_2}		VB = 12 V, I_{load} = 18 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 12.5	VB + 13.5	VB + 15	V
V_{chv3_0}		VB = 18 V, I_{load} = 0 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv3_1}		VB = 18 V, I_{load} = 13 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chv3_2}		VB = 18 V, I_{load} = 22 mA, C1 = C2 = 47 nF, CCP = 2.2 µF	VB + 13	VB + 14	VB + 15	V
V_{chvmax}	Maximum voltage		35	37.5	40	V
V_{chvUV}	Undervoltage detection threshold		VB + 4	VB + 4.5	VB + 5	V
T_{chv}[2]	Rise time	VB = 5.3 V, C1 = C2 = 47 nF, CCP = 2.2 µF, V_{chvUV} released		1	2	ms
R_{on}	On resistance S1~S4			8		

(1) No variation of the external components
(2) Specified by design

PRE-DRIVER

Description

The pre-driver block provides three high-side pre-drivers and three low-side pre-drivers to drive external N-channel MOSFETs. The turn on side of the high-side pre-drivers supply the large N-channel transistor current to quickly charge and PMOS support output voltage up to PDCPV. The turn off side supplies the large N-channel transistor current to quickly discharge, while the low-side pre-drivers supply the large N-channel transistor current for charge and discharge. The output voltage of the low-side pre-driver is controlled by VB and it has VGS protection to make less than 18 V. The pre-driver has a stop condition in some fault conditions ($16 Error Detection).

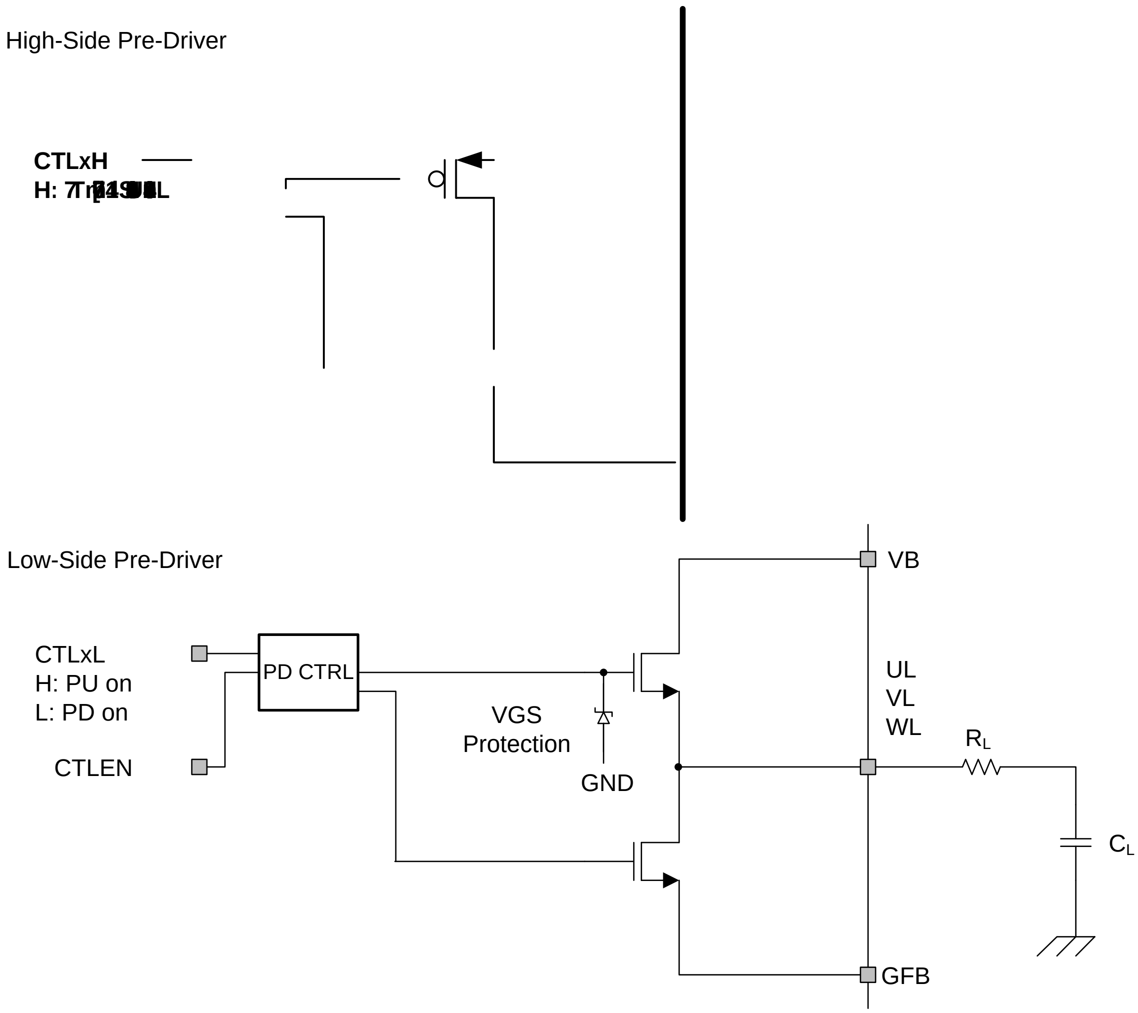


Figure 14. Pre-driver Block Diagram

PRE-DRIVER ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
HIGH SIDE PRE-DRIVER						
V_{OH_H}	Output voltage high	I_{sink} = 10 mA, U(V/W)H – GFB	V_{chv} – 2.7	V_{chv} – 1.35		V
V_{OL_H}	Output voltage low	I_{source} = 10 mA, U(V/W)H – GFB		60	120	mV
R_{ONH_HP}	ON resistance pull up (Pch)	U(V/W)H = PDCPV - 1 V		135	270	
R_{ONH_HN}	ON resistance pull up (Nch)	U(V/W)H = PDCPV - 2.5 V		8	16	
R_{ONL_H}	ON resistance pull down			6	12	
T_{on_h} (1)	Turn-on time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 from 20% to 80%	100	300	500	ns
T_{off_h} (1)	Turn-off time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 from 80% to 20%	100	300	500	ns
$T_{h\text{-}ondly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 to 20%, see Figure 15	100	200	400	ns
$T_{h\text{-}offdly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 11 nF, R_L = 0 to 80%, see Figure 15	100	200	400	ns
LOW SIDE PRE-DRIVER						
V_{OH_L}	Output voltage high	I_{sink} = 10 mA, U(V/W)L – GFB	VB – 0.14	VB-0.07		V
V_{OL_L}	Output voltage low	I_{source} = 10 mA, U(V/W)L – GFB		70	140	mV
R_{ONH_L}	ON resistance pull up			7	14	
R_{ONL_L}	ON resistance pull down			7	14	
T_{on_l} (1)	Turn-on time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 from 20% to 80%	100	300	800	ns
T_{off_l} (1)	Turn-off time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 from 80% to 20%	100	300	800	ns
$T_{l\text{-}ondly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 to 20%, see Figure 15	100	200	400	ns
$T_{l\text{-}offdly}$ (1)	Output delay time	VB = 5.3 ~ 18 V, C_L = 22 nF, R_L = 0 to 80%, see Figure 15	100	200	400	ns
V_{CLAMP}	VGS protection voltage		16	18	20	V
T_{diff1} (1)	Differential time 1	VB = 5.3 ~ 18 V ($T_{h\text{-}on}$)–($T_{l\text{-}off}$), see Figure 15	–300		300	ns
T_{diff2} (1)	Differential time 2	VB = 5.3 ~ 18 V ($T_{l\text{-}on}$)–($T_{h\text{-}off}$), see Figure 15	–300		300	ns

(1) Specified by design

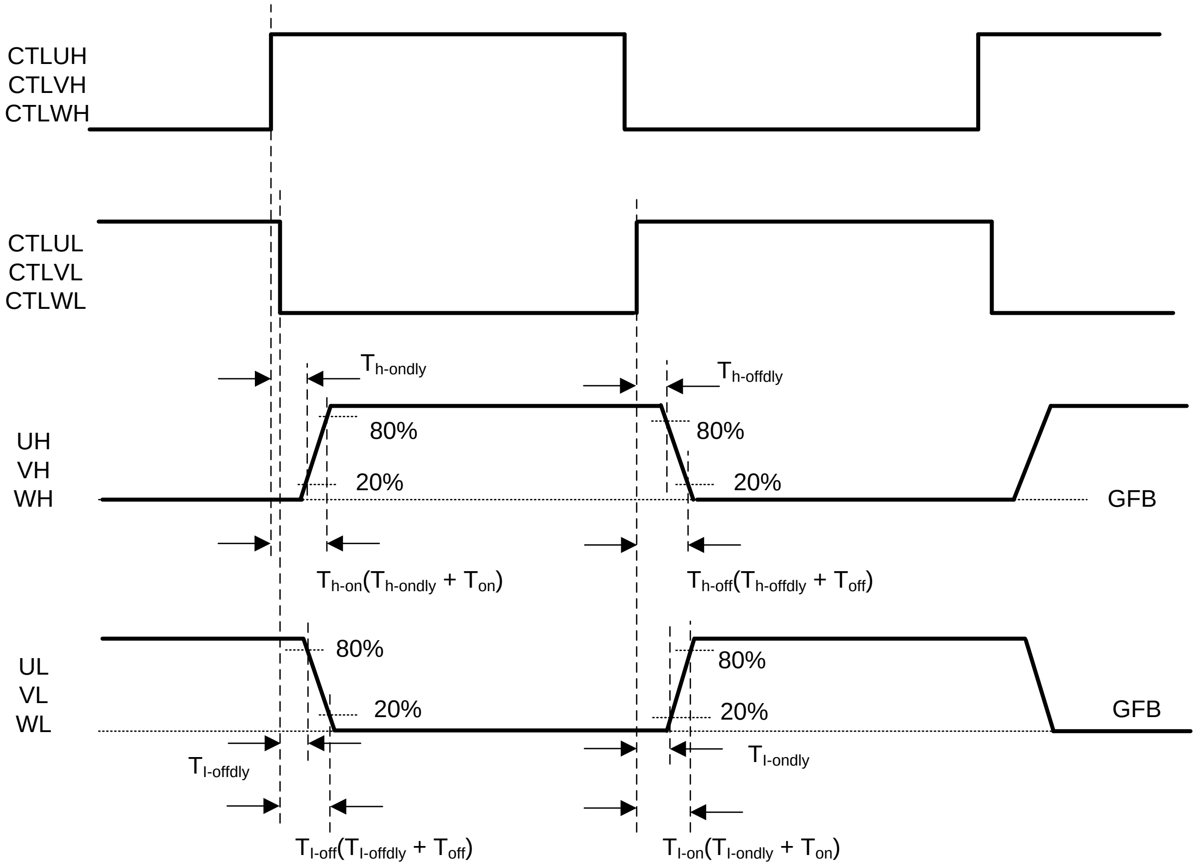


Figure 15. Delay Time from Input to Output

PHASE COMPARATOR

Description

A 3-channel comparator module monitors the external FET by detecting voltage across the drain-source for high-side and low-side FETs. PHTM is the threshold level of comparators usable for sensorless communication. Figure 16 shows an example of the threshold level. There is no detection when CTLEN = Low.

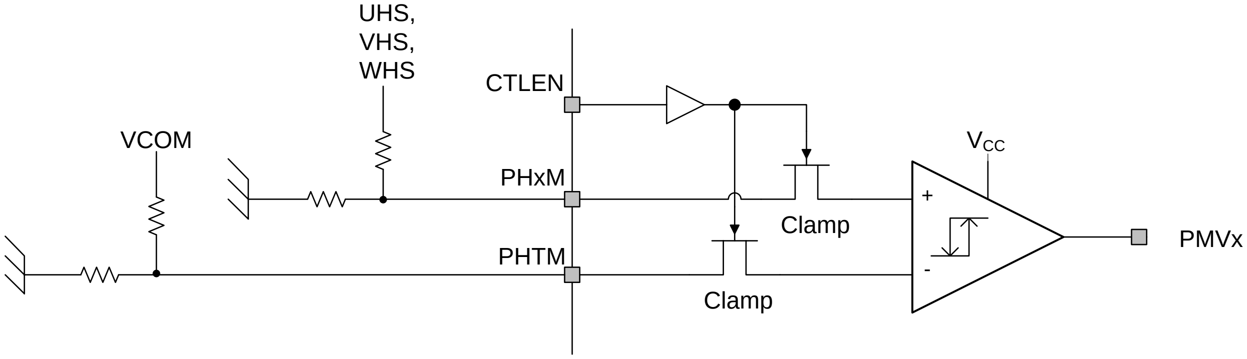


Figure 16. Phase Comparator Block Diagram

PHASE COMPARATORS ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
PHASE COMPARATOR						
V_{iofs}	Input offset voltage		–15	–	15	mV
V_{inp}	Input voltage range (PHTM)	VB = 5.3 ~18 V	1.325	–	4.5	V
V_{inm}	Input voltage range (PHxM)		–1	–	VB	V
V_{ihys}	Input hysteresis voltage		100	200	400	mV
V_{OH}	Output high voltage	I_{sink} = 2.5 mA	0.9 × V_{CC}	–	–	V
V_{OL}	Output low voltage	I_{source} = 2.5 mA	–	–	0.1 × V_{CC}	V
T_{res_tr} (1)	Response time (rising)	C_L = 100 pF	–	0.2	0.5	µs
T_{res_tf} (1)	Response time (falling)	C_L = 100 pF	–	0.4	1	µs

(1) Specified by design

MOTOR CURRENT SENSE

Description

The operational amplifier is operating with an external resistor network for higher flexibility to adjust the current measurement to application requirements. The first stage amplifier is operating with the external resistor and the output voltage up to VB at ALFB. The gain of the amplifier is adjustable by external resistors from x10 to x30. The second stage amplifier is a buffer to MCU at ALV. Current sense has a comparator for motor overcurrent (OVAD). ADTH is the overcurrent threshold level and sets the value by the external resistor as well. Figure 18 shows the curve of the detection level. ALFB is divided by 2, compare this value with ADTH. In the recommended application, zero-point adjustment is required as a large error offset in the initial condition.

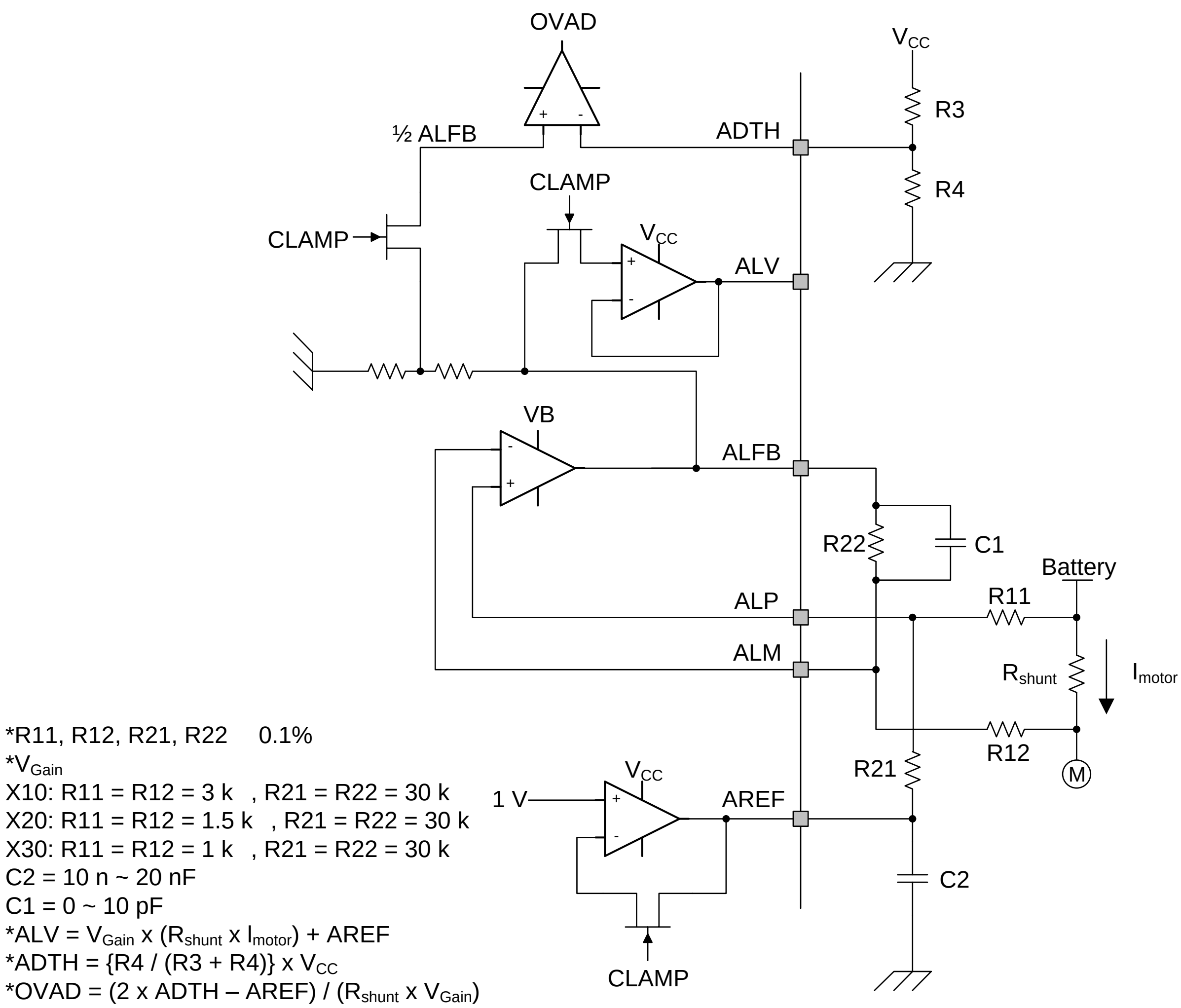


Figure 17. Motor Current Sense Block Diagram

MOTOR CURRENT SENSE ELECTRICAL CHARACTERISTICS(1)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
MOTOR CURRENT(2) SENSE						
V_{Ofs}	Input offset voltage		–5		5	mV
V_{O_0}	Output voltage (ALV)	VB = 5.3 ~ 18 V, I_{motor} = 0 A		1		V

(1) No variation of the external components
(2) Motor current is converted to voltage in test

MOTOR CURRENT SENSE ELECTRICAL CHARACTERISTICS(1) (continued)

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
V_{Line}	Linearity (ALV)	VB = 5.3 ~ 18 V, R_{shunt} = 1 m , R11 = R12 = 1 k , R21 = R22 = 30 k	–2%	30	2%	mV/A
V_{Gain}	Gain		10		30	
T_{set_TR1}	Settling time (Rise) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 m , C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 k , R21 = R22 = 30 k , I_{motor} = 0 30 A, (ALV : 1 1.9 V)	–	1	2.5	µs
T_{set_TR2}	Settling time (Rise) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 m , C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 k , R21 = R22 = 30 k , I_{motor} = 0 100 A, (ALV : 1 4 V)	–	1	2.5	µs
T_{set_TF1}	Settling time (Fall) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 m , C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 k , R21 = R22 = 30 k , I_{motor} = 30 0 A, (ALV : 1.9 1 V)	–	1	2.5	µs
T_{set_TF2}	Settling time (Fall) ALV ±1%	VB = 5.3 ~ 18 V, R_{shunt} = 1 m , C1 = 4.7 pF, C_L = 100 pF, R11 = R12 = 1 k , R21 = R22 = 30 k , I_{motor} = 100 0 A, (ALV : 4 1 V)	–	1	2.5	µs
OVAD	Overcurrent threshold	150-A detection, R_{shunt} = 1 m , R11 = R12 = 1 k , R21 = R22 = 30 k , R3 = 8.2 k , R4 = 10 k	–10%	150	10%	A
TDEL_OVAD(3)	Propagation delay (Rise or fall)		–	–	1.5	µs

(3) Specified by design

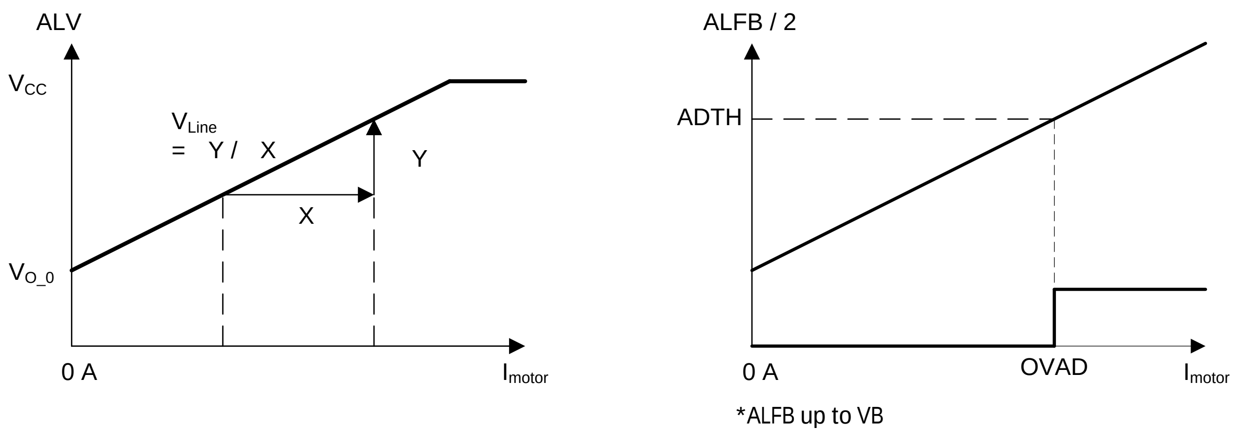


Figure 18. Motor Current Sense and Overcurrent

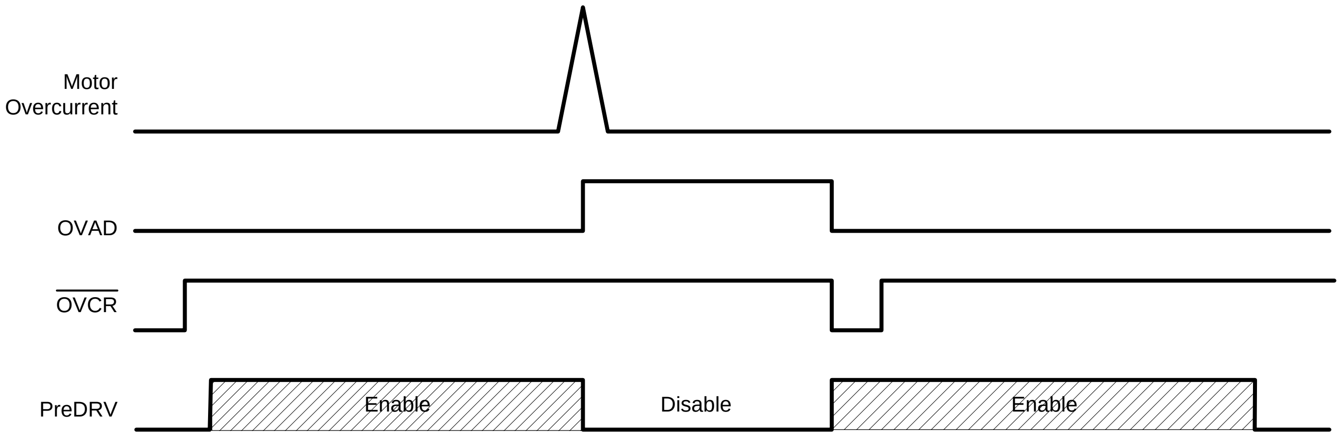


Figure 19. Motor Overcurrent Event

Table 3. Motor Overcurrent Truth Table

$\overline{\text{RES}}$	$\overline{\text{OVCR}}$	MOTOR OVERCURRENT	OVAD	PRE-DRIVER ENABLE OR DISABLE
0	–	–	0 (Clear)	Disable(1)
1	0	–	0 (Clear)(2)(3)	Enable
	1	0	Keep	Enable
		1	1 (Set)	Disable

(1) The CTLEN goes to Hi-Z because the external CPU will not drive it when $\overline{\text{RES}}$ = 0, then all the pre-drivers are turned off because CTLEN is internally pulled down.
(2) The OVAD is not set, even if a motor overcurrent error is generated during $\overline{\text{OVCR}}$ = 0.
(3) The OVAD is cleared if $\overline{\text{OVCR}}$ = 0 even when the motor overcurrent error is generated.

PHASE AMPLIFIER (Sample and Hold Mode and Through Mode)

Description

The 3-channel amplifier module monitors the drain-source for high-side and low-side FETs. Two modes (selected by the SPI) are provided: sample and hold mode, and through mode. Sample and hold is controlled by PSSx at the external pins and PSCx connects the charging capacitor. Through mode is real-time detection and the amplifier has x1–x4 gain control.

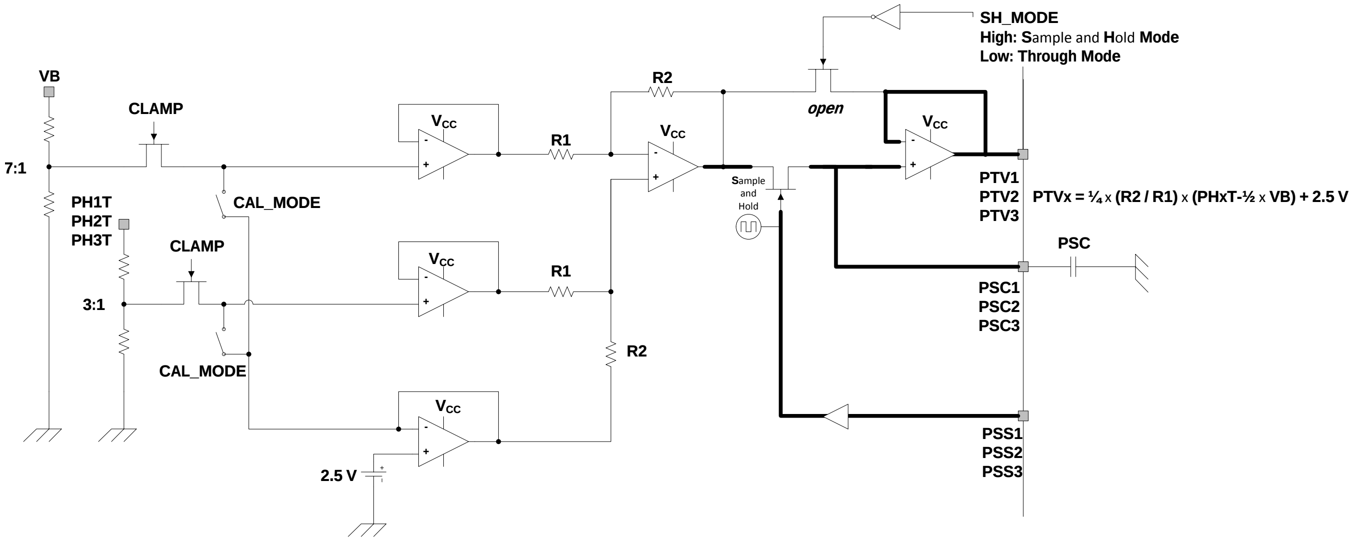


Figure 20. Sample and Hold Mode Block Diagram

Figure 21. Through Mode Block Diagram

Figure 22. Short Mode (Optional) Block Diagram

PHASE AMPLIFIER ELECTRICAL CHARACTERISTICS[1]

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
PHASE AMPLIFIER						
V_{ofs_SH}	Output offset voltage, sample and hold mode	VB = 5.3–18 V, Gain = 1	–50	–	50	mV
V_{ofs_TH}	Output offset voltage, through mode	VB = 5.3–18 V, Gain = 1	–50	–	50	mV
V_{in_cm}	Common mode input range	VB = 5.3–18 V, Gain = 1–4	1.5		VB – 1.5	V
V_{out_max}	Maximum output voltage	VB = 5.3–18 V, Gain = 1–4	4.5	–	–	V
V_{out_min}	Minimum output voltage	VB = 5.3–18 V, Gain = 1–4	–	–	0.5	V
V_{gain}[2]	Gain		–	1 2 3 4	–	
V_{out_SH0}	Output voltage, sample and hold mode	VB = 5.3–18 V, Gain = 1–4, PHxT = VB / 2	–	2.5	–	V
V_{out_TH0}	Output voltage, through mode	VB = 5.3–18 V, Gain = 1–4 PHxT = VB / 2	–	2.5	–	V
V_{out_SH1}	Output voltage, sample and hold mode	VB = 12 V, Gain = 1, PHxT = 1.5 V	–	1.375	–	V
V_{out_TH1}	Output voltage, through mode	VB = 12 V, Gain = 1, PHxT = 1.5 V	–	1.375	–	V
V_{out_SH2}	Output voltage, sample and hold mode	VB = 12 V, Gain = 1, PHxT = 10.5 V	–	3.625	–	V
V_{out_TH2}	Output voltage, through mode	VB = 12 V, Gain = 1, PHxT = 10.5 V	–	3.625	–	V
STL_SHTR	Settling time (rise), sample and hold mode PTVx ±1%	VB = 12 V, Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 1.5 V 10.5 V, (PTVx = 1.375 V 3.625 V), see Figure 25		1.5	3	µs
STL_THTR	Settling time (rise), through mode PTVx ±1%	VB = 12 V, Gain = 1, PTVx = 100 pF, PHxT = 1.5 V 10.5 V, (PTVx = 1.375 V 3.625 V), see Figure 26		1.5	3	µs
STL_SHTF	Settling time (fall), sample and hold mode PTVx ±1%	VB = 12 V, Gain = 1, PSC = 470 pF, PTVx = 100 pF, PHxT = 10.5 V 1.5 V, (PTVx = 3.625 V 1.375 V), see Figure 25		1.5	3	µs
STL_THTF	Settling time (fall), through mode PTVx ±1%	VB = 12 V, Gain = 1, PTVx = 100 pF, PHxT = 10.5 V 1.5V, (PTVx = 3.625 V 1.375 V), see Figure 26		1.5	3	µs
SH Error Voltage	Falling voltage	VB = 5.3–18 V, PSC = 470 pF, TH = 1 mS, see Figure 24		5	75	mV

(1) No variation of the external components.
(2) V_{gain} is an SPI setting

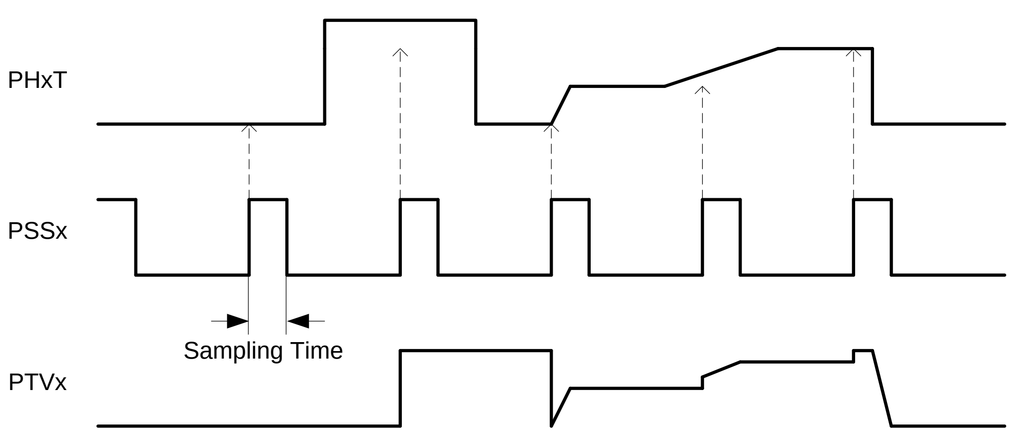


Figure 23. Sampling Timing Chart

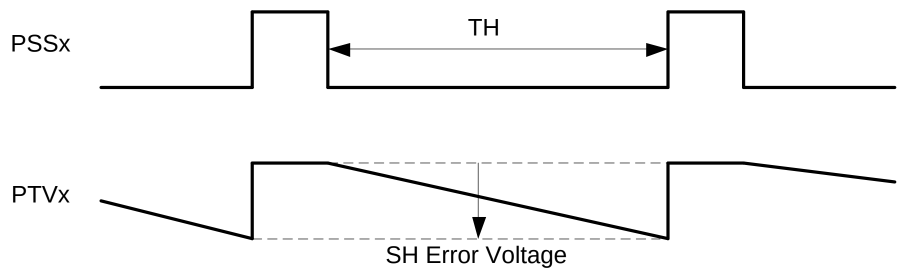


Figure 24. Holding Timing Chart

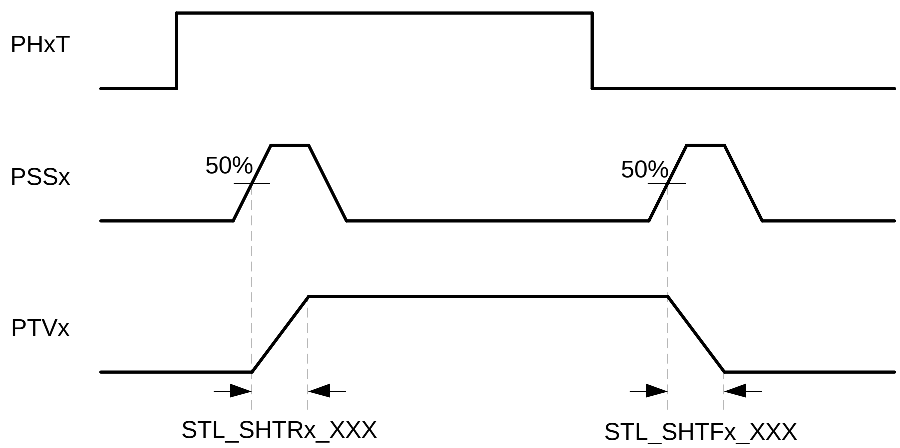


Figure 25. Settling Time Timing Chart (Sample and Hold Mode)

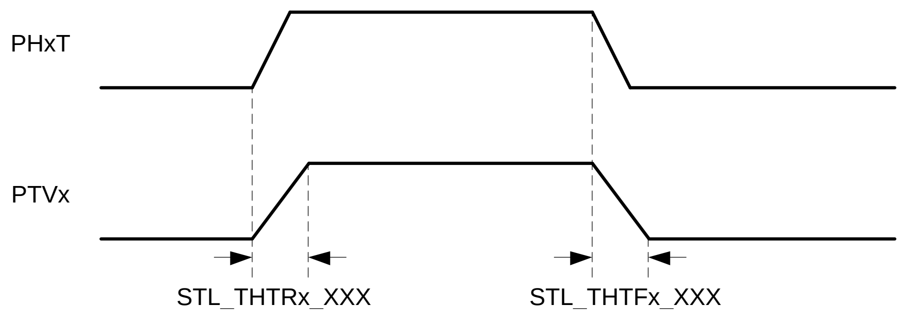
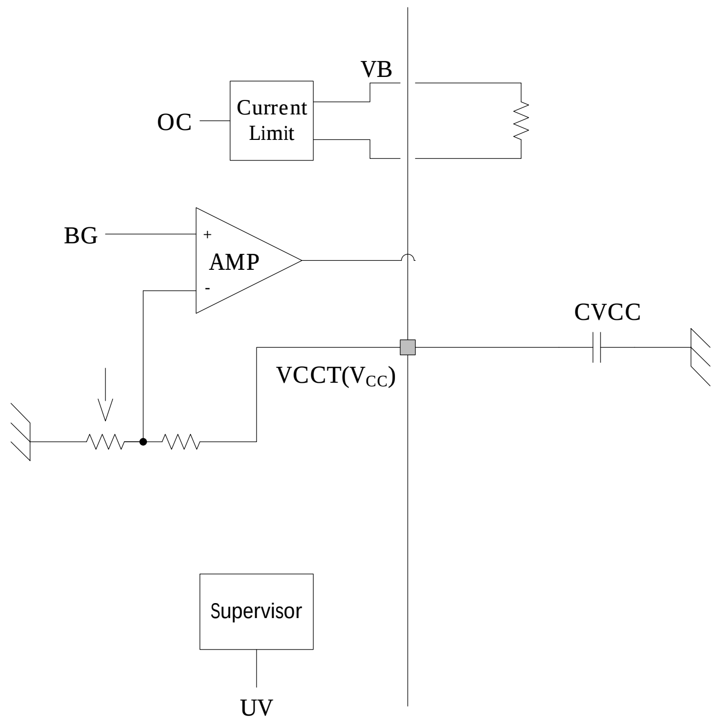
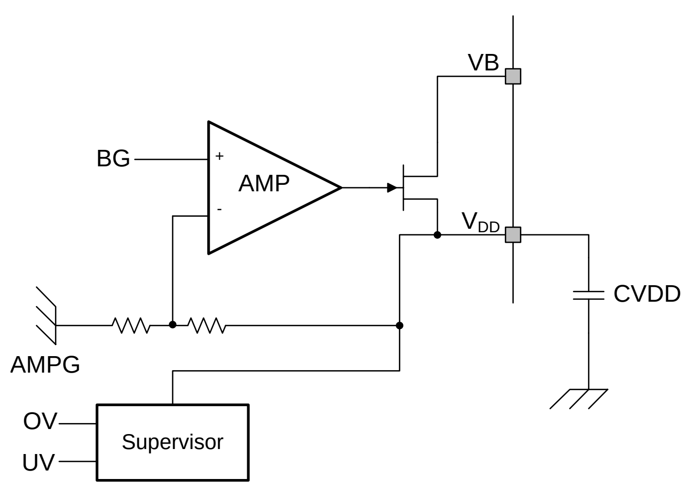
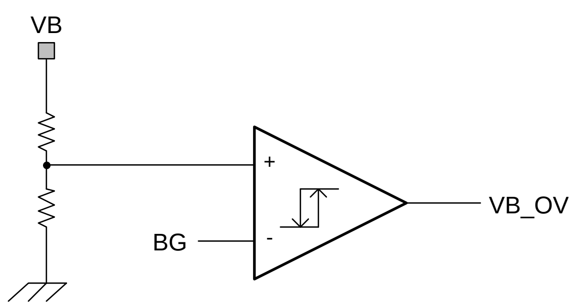


Figure 26. Settling Time Timing Chart (Through Mode)


VB
OC
Current
Limit
BG
AMP
+
-
CVCC
VCCT(VCC)
Supervisor
UV


VB
BG
AMP
+
-
VDD
CVDD
AMPG
OV
UV
Supervisor


VB
+
-
BG
VB_OV

THERMAL SHUTDOWN

Description

The device has temperature sensors that produce a pre-driver stop condition if the chip temperature exceeds 175°.

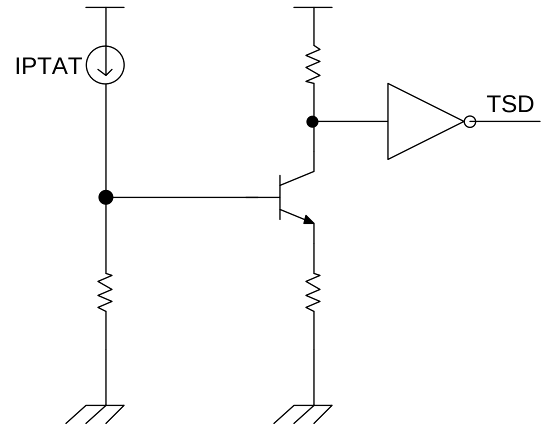


Figure 30. Thermal Shutdown Block Diagram

THERMAL SHUTDOWN ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

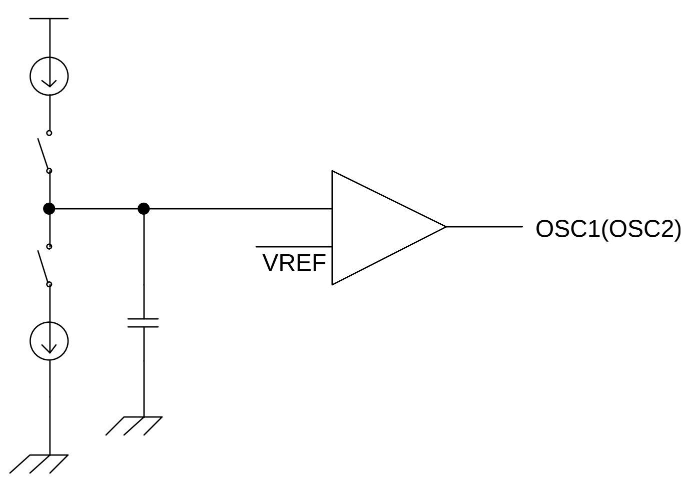
PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
THERMAL SHUT DOWN						
TSD[(1)]	Thermal shut down threshold		155	175	195	°C

(1) Specified by design

OSCILLATOR

Description

Oscillator block generates two 10-MHZ clock signals. OSC1 is the main clock used for internal logic synchronization and timing control. OSC2 is the seco[illegible]



OSCILLATOR ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
OSCILLATOR						
OSC	OSC frequency		9	10	11	MHz

I/O

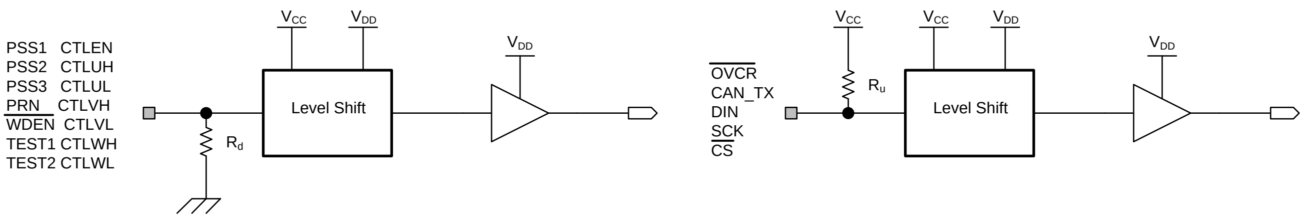


Figure 32. Input Buffer 1 Block Diagram

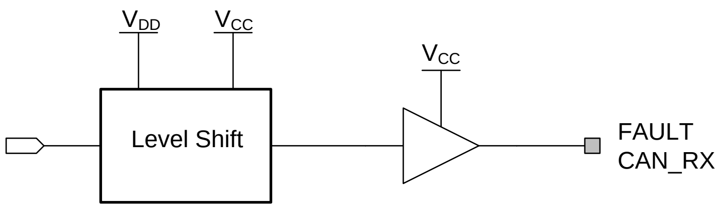


Figure 33. Output Buffer 1 Block Diagram

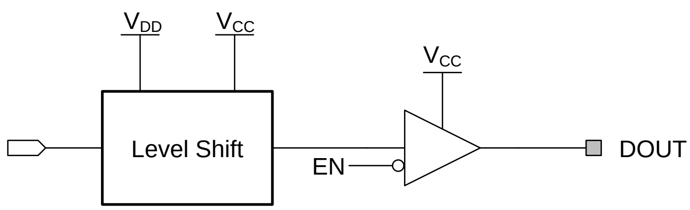


Figure 34. Output Buffer 2 Block Diagram

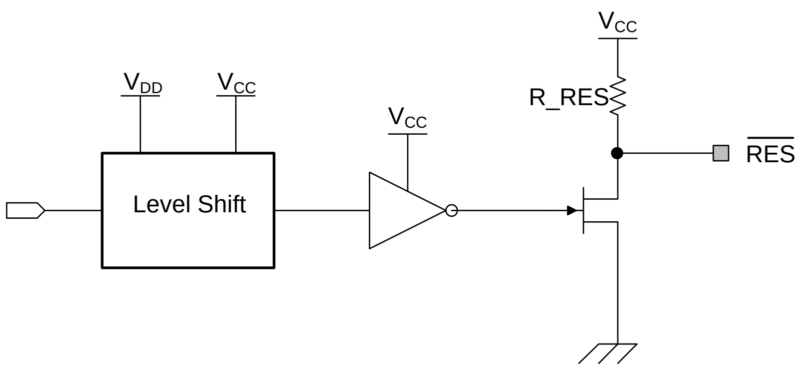


Figure 35. Output Buffer 3 Block Diagram

ELECTRICAL CHARACTERISTICS

VB = 12 V, T_A = –40°C to 125°C (unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
INPUT BUFFER 1						
V_{IH}	Input threshold logic high		0.7 × V_{CC}			V
V_{IL}	Input threshold logic low				0.3 × V_{CC}	V
R_u	Input pullup resistance		50	100	150	k
R_u (CAN_TX)	Input pullup resistance		12.5	25	37.5	k
R_d	Input pulldown resistance		50	100	150	k
OUTPUT BUFFER 1 AND 2						
V_{OH}	Output level logic high	I_{sink} = 2.5 mA	0.9 × V_{CC}			V
V_{OL}	Output level logic low	I_{source} = 2.5 mA			0.1 × V_{CC}	V
OUTPUT BUFFER 3						
R_RES	Pullup resistor		1.5	3	4.5	k
V_{OL}	Output level logic low	I_{source} = 2 mA			0.1 × V_{CC}	V

ERROR DETECTION

Table 4. Error Detection

ITEMS	SPI	PRE-DRIVER	FAULT SIGNAL	$\overline{RES}$
VB – Overvoltage	–	STOP	L	H
CP – Overvoltage	–	STOP	L	H
CP – Undervoltage	Error Bit (CPLV)	–	L	H
V_{CC} – Overvoltage	Error Bit (VCO)	–	L	H
V_{CC} – Undervoltage	–	STOP	L	L
V_{CC} – Overcurrent	Error Bit (V_{CC})	–	H	H
Motor – Overcurrent	Error Bit (OVAD)	STOP	H	H
V_{DD} – Overvoltage	Error Bit (VDO)	–	L	H
V_{DD} – Undervoltage	–	STOP	L	L
Thermal Shut Down	Error Bit (TD)	STOP	H	H
Watchdog	–	–	L	L
EEPROM Data Check	Error Bit (EEP)	–	L	H
Clock Monitor	–	–	L	L
CAN Overcurrent	Error Bit (CCD)	–	L	H
SPI	Error Bit (SPI)	–	L	H

REVISION HISTORY

Changes from Original (October, 2012) to Revision A **Page**

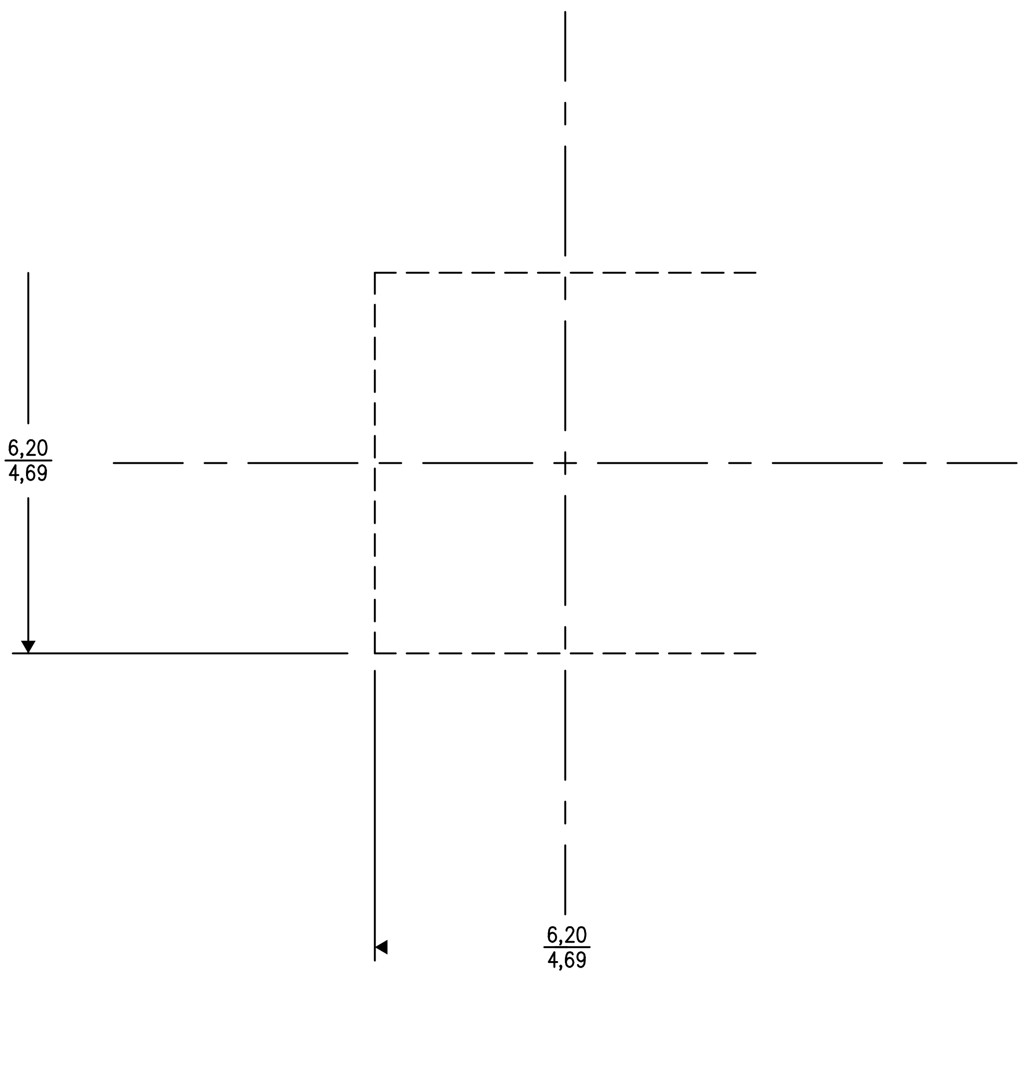
- Changed max rating for PHTM, PH1M, PH2M, and PH3M from -2 –40 V to -1–40 V. 2
- Changed O to IO for pin 44 and 45. 3
- Deleted Table 1 Pin Equivalent Circuits. 3
- Changed max I_{VB} from 40 to 35 mA. 6
- Changed CANH and CANL to CAN_H and CAN_L in description section; changed CANH, CANL, and CANM to CAN_H, CAN_L, and CAN_M in block diagram. 13
- Changed VCANH and VCANL to VCAN_H and VCAN_L in CAN receiver section. 13
- Changed VCANH and VCANL to VCAN_H and VCAN_L in CAN AC characteristic section. 14
- Changed CANH_D to VCANH_D, CANL_D to VCANL_D, and VCANH - VCANL to VCAN_H - VCAN_L in CAN timing chart. 14
- Changed ICANH to IA_CANH and ICANL to IA_CANL in CAN testing condition image. 15
- Changed CANTX to CAN_TX and CANH and CANL to CAN_H and CAN_L in CAN reset function image. 15
- Changed charge pump description. 16
- Changed V_{chv1_12} to V_{chv1_1}, V_{chv1_20} to V_{chv1_2}, V_{chv2_12} to V_{chv2_1}, V_{chv2_20} to V_{chv2_2}, V_{chv3_12} to V_{chv3_1}, V_{chv3_20} to V_{chv3_2}. 17
- Added min and typ values to V_{chvmax} parameter. 17
- Changed min, typ and max values for V_{chv1_0} through V_{chv3_2}; changed typ R_{on} value from 10 to 8. 17
- Changed pre-driver description and updated block diagram. 18
- Removed R_{ONH_H} row, removed cross-references from R_{ONH_HP} and R_{ONH_HN}, added conditions to R_{ONH_HP} and R_{ONH_HN}, changed typ and max values for R_{ONH_HN}. 19
- Removed "side" from V_{OH_L} and V_{OL_L} description, changed high side and low side to pull up and pull down respectively for R_{ONH_L} and R_{ONL_L}. Changed values for R_{ONL_L} from 10 typ to 7 typ and from 20 max to 14 max in pre-driver electrical characteristics table. 19
- Changed Turn-off time from T_{off_h} to T_{off_l} 19
- Changed all min, typ and max values in pre-driver electrical characteristics table, changed all µs units to ns. Removed side from VOH_H and VOL_H, changed RONH_H from ON resistance high side to ON resistance pull up, changed RONL_H from ON resistance low side to ON resistance pull down. Added two new parameters for RONH_HP and RONH_HN. 19
- Updated phase comparator description. 21
- Changed min value for V_{inm} from -2 to -1. 21
- Changed min, typ, and max values for V_{iofs}, V_{ihys}, T_{res_tr}, and T_{res_tf}. Changed unit for V_{ihys} from V to mV. 21
- Changed motor current sense description and motor current sense block diagram. 22
- Added C1 = 4.7 pF to T_{set_TR1}, T_{set_TR2}, T_{set_TF1}, and T_{set_TF2} conditions in motor current sense electrical characteristics. 23
- Updated Sample and Hold Mode Block Diagram. 25
- Changed typ and max values for V_{ofs_SH} and SH Error Voltage. 27
- Changed V_{CC} Block Diagram. 29
- Changed max current limit from 500 to 550. 30
- Added 3 new parameters to VCC and VDD Electrical Characteristics table. Changed min, typ, and max values VLRVCC, CVCC, TVCC1, TVCC2, VDDOV, TVDD. Added table note. 30
- Changed VB Monitor description. 30
- Added typ and max values to VB monitor electrical characteristics table. 30
- Changed thermal shutdown description. 31
- Changed location of EN in Figure 34. 32
- Changed MCU RESET column to $\overline{RES}$ column; changed values. 33

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
DRV3202QPFPQ1	ACTIVE	HTQFP	PFP	80	96	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV3202	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between een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