Features

- A
- D
- M
- S N C , N MH
- D
  - 120µA ( )
  - S ½ PCB
- D LED
- A
- S
- 16- SOIC

General Description

T 2013H G G IC
T IC
. T 2013H

B
. C
. I
PROG$_{1-6}$
A

N
LED . T

T 2013H

Pin Descriptions

LCOM **LED c**

T LED . T CC PROG1-5 . LCOM

SEG1 **LED d a e e (d a f c-**
SEG5 **PROG1 PROG5**

E LED LCOM.

PROG1 **P a ed f c e ec**
PROG6 **(d a f c SEG1 - SEG5)**

T (PFC),

SR **Se e e**

T (SR) RS . T SR (F 1) SR > SS SR < SS , T SRO, 2013H SR + OS.

DONE **C a ec e e**

T / 2013H.

DISP **D a c**

DISP LED . T DISP

SB **Sec da ba e**

T (ED)

RBI **Re e bac**

T 2013H CC < 3 . A RBI.

HDQ **Se a I/O**

T

REF **V a e efe e ce f e a**

REF

VCC **S a e**

VSS **G d**

Functional Description

General Operation

T 2013H

. T 2013H

. T

. T

F 1

2013H LED . T 2013H

T

T

(PFC)

. A

LED .

T 2013H

(R_S F

1). A

SR .

REF

V_{CC}

$SEG_1/PROG_1$ SB

$SEG_2/PROG_2$

$SEG_3/PROG_3$ DISP

$SEG_4/PROG_4$

$SEG_5/PROG_5$

$PROG_6$ V_{SS}

FG2013H1

Register Backup

T 2013H RBI
2013H CC
3.0 CC, RBI CC, 3.0

A CC 3.0, 2013H . I ,
NAC LMD
PFC.

Voltage Thresholds

I SR /
2013H
SB (ED)
.

T ED
– .

T ED 2013H :

ED 1 ( ) = 1.00

ED F ( ) = ED 1 - 100

T (RB1 RB2 F 1)
.

I SB ED
T 1,
SB,
. ED
O LD FLGS2 .

Table 1. Delay Time in Seconds

Capacity	Temperature		
	< 10 C	10 C to 30 C	> 30 C
> 40%	7	6	5
20% 40%	4	3	2
< 20%	2	2	2

Reset

T 2013H CC
RBI 15
. T
00 PPFC (=)
00 LMD (= 05 .)

Temperature

T 2013H
10-C -35-C +85-C. T -
. T
10-C :

TMPGG (hex)	Temperature Range
0	< -30-C
1	-30-C -20-C
2	-20-C -10-C
3	-10-C 0-C
4	0-C 10-C
5	10-C 20-C
6	20-C 30-C
7	30-C 40-C
8	40-C 50-C
9	50-C 60-C
A	60-C 70-C
B	70-C 80-C
C	> 80-C

Layout Considerations

T 2013H
SR SS . OS (SR
) PC . F
PC
. S
. A :

- T SB CC SS
. A
0.1µ CC.
- T (R$_S$)
2013H.
- T R-C SR
SR . T R
100K.

Gas Gauge Operation

T F 2 -
2013H. T 2013H ,
. T 2013H

. D LCOMP (= 0). LCOMP 2013H . T 2013H -

T , N A C (NAC), . B NAC , NAC DCR (D C R). NAC OFFSET (= 0 .)

T D C R (DCR) I M D (LMD) . T , 2013H .

T ' P F C (PFC) T 2. LMD , NAC . T .

1. **La Mea ed D c a e (LMD) ea ed ba e ca ac :**

LMD . O (CC), LMD = PFC. D LMD D C R (DCR) ED . T LMD DCR 25% LMD. A DCR LMD . T LMD 100% .

2. **P a ed F C (PFC) a ba - e ca ac :**

T LMD PFC. T PFC 100% . T 2013H PFC T 2. T PFC A :

B (A) * (Ω) =

PFC ( )

S PFC .

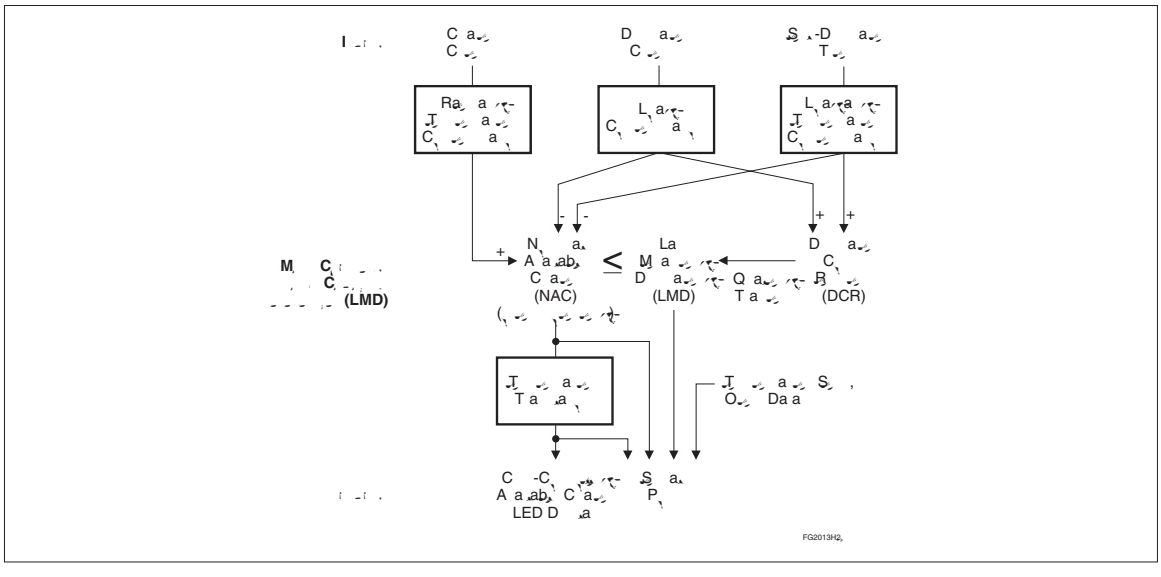


Figure 2. Operational Overview

Example: Selecting a PFC Value

G :

S = 0.0075Ω
N = 14
C = 5000 A , N C
C = 1A 30A
R 4
S = 1%
T = 0.85
T = -75µ
= 5 225

T :

5000 A ∗ 0.0075Ω = 37.5

S :

PFC = 44,800 35
$PROG_1$, $PROG_2$ = , L
$PROG_3$ =
$PROG_4$ = H
$PROG_5$ = L
$PROG_6$ =

Table 2. bq2013H Programmed Full Count mVh Selections

Programmed Full Count (PFC)	mVh	Scale	$PROG_1$	$PROG_2$
27136	84.8	1/320	H	H
24064	75.2	1/320	H	
41472	64.8	1/640	H	L
35072	54.8	1/640		H
28672	44.8	1/640		
44800	35	1/1280		L
30720	24	1/1280	L	H
38400	15	1/2560	L	
12800	5	1/2560	L	L

Table 3. Programmed Self-Discharge

$PROG_3$	Self-Discharge
H	1.6%
	0.8%
L	0.2%

$PROG_4$	Overload Threshold	Display Mode
H	V OVLD = -75 V	R [illegible] /4 [illegible] - [illegible]
	V OVLD = -75 V	R [illegible] /4 [illegible] - [illegible]
L	V OVLD = -25 V	A [illegible] /4 [illegible] - [illegible]

T 35 (4667 A) 2013H – ED 1.

3. **N a A a ab e Ca ac (NAC):**

   NAC LMD 0. NAC 0 ED 1. T , NAC NAC = LMD. DONE , NAC LMD.

4. **D c a e C Re e (DCR):**

   T DCR NAC NAC 0. P NAC = 0 ( ), DCR. A NAC = 0, DCR. T DCR 0 NAC = LMD. T DCR FFFF .

   T DCR LMD ED 1 :

   - N (2 NAC) NAC = LMD ED 1.
   - T 6% NAC.
   - T ≥ 0–C ED 1 .
   - DQ .

Charge Counting

C I $_{SR}$ 2013H NAC $_{SRO}$ ($_{SR}$ + $_{OS}$) LED $_{SRO}$ > 500µ . C NAC .

T 2013H $_{SRO}$ > 250µ . A 2 NAC . O $_{SRO}$ 250µ .

Discharge Counting

A $_{SRO}$ < -250µ NAC DCR . I $_{SRO}$ < -2 . T 10 $_{SRO}$ -2 .

Self-Discharge Estimation

T 2013H NAC DCR . T T 3. T 20 30–C. T NAC 0.

Count Compensations

T 2013H NAC ≥ 2 / . C (NA 0 7 1 1 T 7 312.48 501.8 (NA

Self-Discharge Compensation

T
. T 8
<10–C >70–C,
(10–C). S T 7.

Offset Compensation

T 2013H
. T
CC
. T
PCB -75µ . P
6
OS. O
SRO < -250µ SRO > 250µ .

Error Summary

T LMD
519 519 519 9 519 (519) 519

C 2013H . F 3 2013H NACH .

bq2013H Command Code and Registers

T 2013H T 9

Command Code

T 2013H 2013H.
T :

- /R
- C

T /R

T /R :

Command Code Bits							
7	6	5	4	3	2	1	0
/R	-	-	-	-	-	-	-

/R :

0 T 2013H

1 T

T A

Command Code Bits							
7	6	5	4	3	2	1	0
-	AD6	AD5	AD4	AD3	AD2	AD1	AD0 (LSB)

Table 9. bq2013H Command and Status Registers

Symbol	Register Name	Loc. (hex)	Read/ Write	Control Field							
				7(MSB)	6	5	4	3	2	1	0(LSB)
FLGS1	P	01	R	CHGS	BRP	RS D	RS D	DQ	RS D	ED 1	ED F
TMPGG	T	02	R	TMP3	TMP2	TMP1	TMP0	GG3	GG2	GG1	GG0
NACH	N	03	R/	NACH7	NACH6	NACH5	NACH4	NACH3	NACH2	NACH1	NACH0
NACL	N	17	R/	NACL7	NACL6	NACL5	NACL4	NACL3	NACL2	NACL1	NACL0
BATID	B	04	R/	BATID7	BATID6	BATID5	BATID4	BATID3	BATID2	BATID1	BATID0
LMD	L	05	R/	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLGS2	S	06	R	CR	RS D	RS D	RS D	RS D	RS D	RS D	O LD
PPD	P	07	R	RS D	RS D	PPD6	PPD5	PPD4	PPD3	PPD2	PPD1
PP	P	08	R	RS D	RS D	PP 6	PP 5	PP 4	PP 3	PP 2	PP 1
OCTL	O	0	R/	OC6	OC5	OC4	OC3	OC2	OC1	OCE	OCC
OFFSET	O	0	R/	OFS7	OFS6	OFS5	OFS4	OFS3	OFS2	OFS1	OFS0
SDR	S	0	R/	SDR7	SDR6	SDR5	SDR4	SDR3	SDR2	SDR1	SDR0
DMF	D	0	R/	DMF7	DMF6	DMF5	DMF4	DMF3	DMF2	DMF1	DMF0
LCOMP	L	0	R/	LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0
CCOMP	P	0	R/	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0
PPFC	P		R/	RS D	RS D	RS D	RS D	RS D	RS D	RS D	RS D
SB	B	7	R	SB7	SB6	SB5	SB4	SB3	SB2	SB1	SB0

N e : RS D =
A

Primary Status Flags Register (FLGS1)

T FLGS1 =01 2013H .

T charge status (CHGS) T 2013H NAC SRO > 250µ . A SRO 250µ CHGS.

T CHGS :

FLGS1 Bits							
7	6	5	4	3	2	1	0
CHGS	-	-	-	-	-	-	-

CHGS

0 E SRO < 250µ

1 T NAC SRO > 250µ

T battery replaced (BRP) 2013H CC . BRP NAC LMD, ED 1 . BRP = 1 .

T BRP :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	BRP	-	-	-	-	-	-

BRP

0 2013H NAC = LMD ED 1

1 2013H

T valid discharge (DQ) 2013H NAC=LMD. T LMD DQ :

- NAC 6% DQ
- A SRO > SRQ NAC
- T ED 1 0–C.

T DQ :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	DQ	-	-	-

DQ

0 S NAC 6%, ED 1 0°C,

1 O NAC = LMD

T end-of-discharge warning (ED 1) . SEG1 4H DONE . ED 1 O LD = 1. T ED .

T ED 1 :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	ED 1	-

ED 1

0 SB ≥ ED 1

1 SB < ED 1, O LD

T final end-of-discharge warning (ED F) . A T ED F T ED F 100 ED 1 .

T ED F :

FLGS1 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	ED F

ED F :

0 SB ≥ ED F

1 SB < ED F, O LD

Temperature and Gas Gauge Register (TMPGG)

TMPGG Temperature Bits							
7	6	5	4	3	2	1	0
TMP3	TMP2	TMP1	TMP0	-	-	-	

T TMPGG (=02)
T
T

T 2013H
T
T
T 10.

T 2013H
NAC LMD PFC.
T
TMPGG .
T

. T CR

T overload (O LD) PROG4 T 4. O LD

T O LD :

FLGS2 Bits							
7	6	5	4	3	2	1	0
-	-	-	-	-	-	-	O LD

O LD :

0 I SRO > O LD

1 I SRO < O LD

Program Pin Pull-Down Register (PPD)

T PPD (=07) 2013H. T PPD , PPD1 6. A . F PROG1 PROG4 , PPD 001001.

PPD/PPU Bits							
7	6	5	4	3	2	1	0
RS D	RS D	PP 6	PP 5	PP 4	PP 3	PP 2	PP 1
RS D	RS D	PPD_6	PPD_5	PPD_4	PPD_3	PPD_2	PPD_1

Program Pin Pull-Up Register (PPU)

T PPU (=08) 2013H. T PPU , PPU1 6. A . F PROG3 PROG5 PPU 010100.

Output Control Register (OCTL)

T OCTL (=0) 2013H. T OCTL 1 OCTL, OCE, . T OC5 1 OCTL (T 9) , SEG5 1, OCE=1. *W OCE , 1, MSB OCTL 1.* T OCE 2013H

. OCE 2013H.

Offset Adjustment Register

T (=0) NAC FC. T PROG6. T :

- 0 =
- 46 = -75µ
- 23 = -150µ

T :

$$O = \frac{1}{289 * \ COS}$$

COS

Self-Discharge Rate Compensation

T T PROG3. T :

- 235 = 1.6% $\left(\frac{1}{64}\right)$
- 214 = 0.8% $\left(\frac{1}{128}\right)$
- 88 = 0.2% $\left(\frac{1}{512}\right)$

T :

$$SDR = 256 - \left(\frac{0.3296}{C_{SD}}\right)$$

C_{SD} .

Digital Magnitude Filter (DMF)

T DMF (=0) . B SRD SRQ . T DMF 250µ . T :

$$DMF = \frac{45}{\ SRD,Q}$$

SRD,Q .

N : O A SRD SRQ OS 2013H.

Load Compensation

T [illegible] (V [illegible] = 0 [illegible])
2013H [illegible] E
LCOMP [illegible] 2µ [illegible]. T [illegible] LCOMP

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
٢ CC	R ▼ ١ ٢ SS	-0.3	+7.0	٢	
A ٢ ١	R ▼ ١ ٢ SS	-0.3	+7.0	٢	
REF	R ▼ ١ ٢ SS	-0.3	+8.5	٢	C ١ R1 (F ١ 1)
٢ SR CC	R ▼ ١ ٢ SS	-0.3	٢ +0.7	٢	100 Ω SR 8.3 3.65.2 1.414 ▼ SS

DC Voltage Thresholds (TA = TOPR; V = 3.0 to 6.5V)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
٢ ED	E ▼ ١ ▼ ١	0.96 *٢ ED	٢ ED	1.04 *٢ ED	٢	SB
٢ SRO	SR ▼ ١	-300	-	+500	٢	SR,٢ SR +٢ OS
٢ SRQ	٢ ▼ ١ ▼ ١	250	-	-	µ٢	٢ SR +٢ OS
٢ SRD	٢ ▼ ١ ▼ ١	-	-	-250	µ٢	٢ SR +٢ OS

N e: ٢ OS ▼ PC ▼ P ▼ ▼ ▼ S ▼ I ▼ C ▼ –

DC Electrical Characteristics ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
▼ CC	S▼ ▼	3.0	4.25	6.5	▼	▼ CC < 2.0▼ ≥ 3.0▼ ▼
▼ OS	O▼ ▼ SR	-	±50	±150	µ▼	$\overline{DISP}$ =▼ CC
▼ REF	R▼ ▼ 25–C	5.7	6.0	6.3	▼	IREF = 5µA
	R▼ ▼ -40–C +85–C	4.5	-	7.5	▼	IREF = 5µA
RREF	R▼ ▼	2.0	5.0	-	MΩ	▼ REF = 3▼
ICC	N▼ ▼	-	90	135	µA	▼ CC = 3.0▼ , HDQ = 0
		-	120	180	µA	▼ CC = 4.25▼ , HDQ = 0
		-	170	250	µA	▼ CC = 6.5▼ , HDQ = 0
▼ SB	B▼	0	-	▼ CC	▼	
RSB ▼	SB▼ ▼	10	-	-	MΩ	0 <▼ SB <▼ CC
IDISP	$\overline{DISP}$▼ ▼	-	-	5	µA	▼ DISP =▼ SS
ILCOM	LCOM▼ ▼	-0.2	-	0.2	µA	$\overline{DISP}$ =▼ CC
IRBI	RBI▼ ▼ -	-	-	100	A	▼ RBI >▼ CC < 3▼

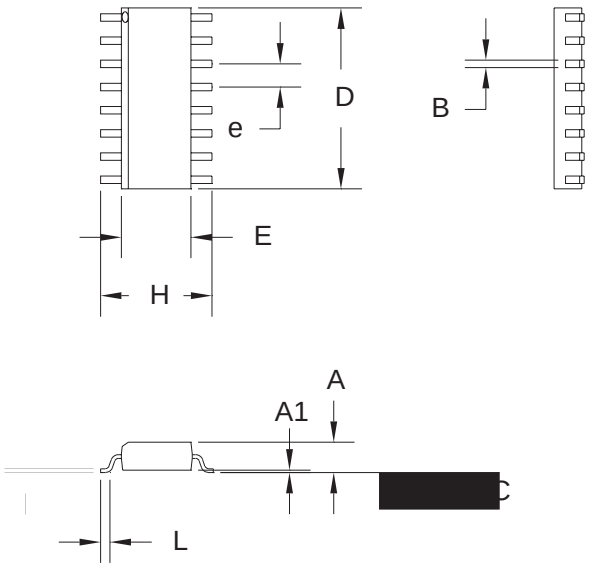
RHDQ25064.7(M) TJ/F974T (K2.2616 -0.0041 TD178)T /F1 T 2.0899 0.0041 TF97 0 R

High-Speed Serial Communication Timing Specification ($T_A = T_{OPR}$)

Symbol	Parameter	Minimum	Typical	Maximum

TD201803.eps

16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

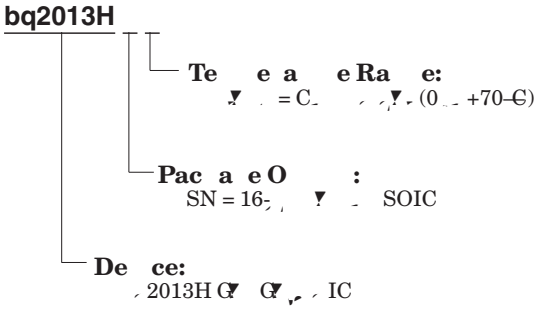
Dimension	Minimum	Maximum
A	0.060	0.070
A1	0.004	0.010
B	0.013	0.020
C	0.007	0.010
D	0.385	0.400
E	0.150	0.160
e	0.045	0.055
H	0.225	0.245
L	0.015	0.035

Data Sheet Revision History

ChangeNo.	Page No.	Description of Change
1	A	F P
2	3	
2	8	C 200µ 250µ .
2	9	C ±200µ ±250µ
2	11	D R/ R–
2	12	C 200µ 250µ
2	14	C DMF 200µ 250µ
2	16	A REF
2	16	C 200µ 250µ
2	16	A SRO
2	17	C DQ HDQ
2	17	C OL 0.5 0.3 (.)
2	17	A RPROG

N e: C 1 = D . 1998 J 1998 P .
C 2 = M 1999 B D . 1998.

Ordering Information



Notes

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
BQ2013HSN-A514	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	Samples
BQ2013HSN-A514G4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	Samples
BQ2013HSN-A514TR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	Samples
BQ2013HSN-A514TRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2013H A514	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
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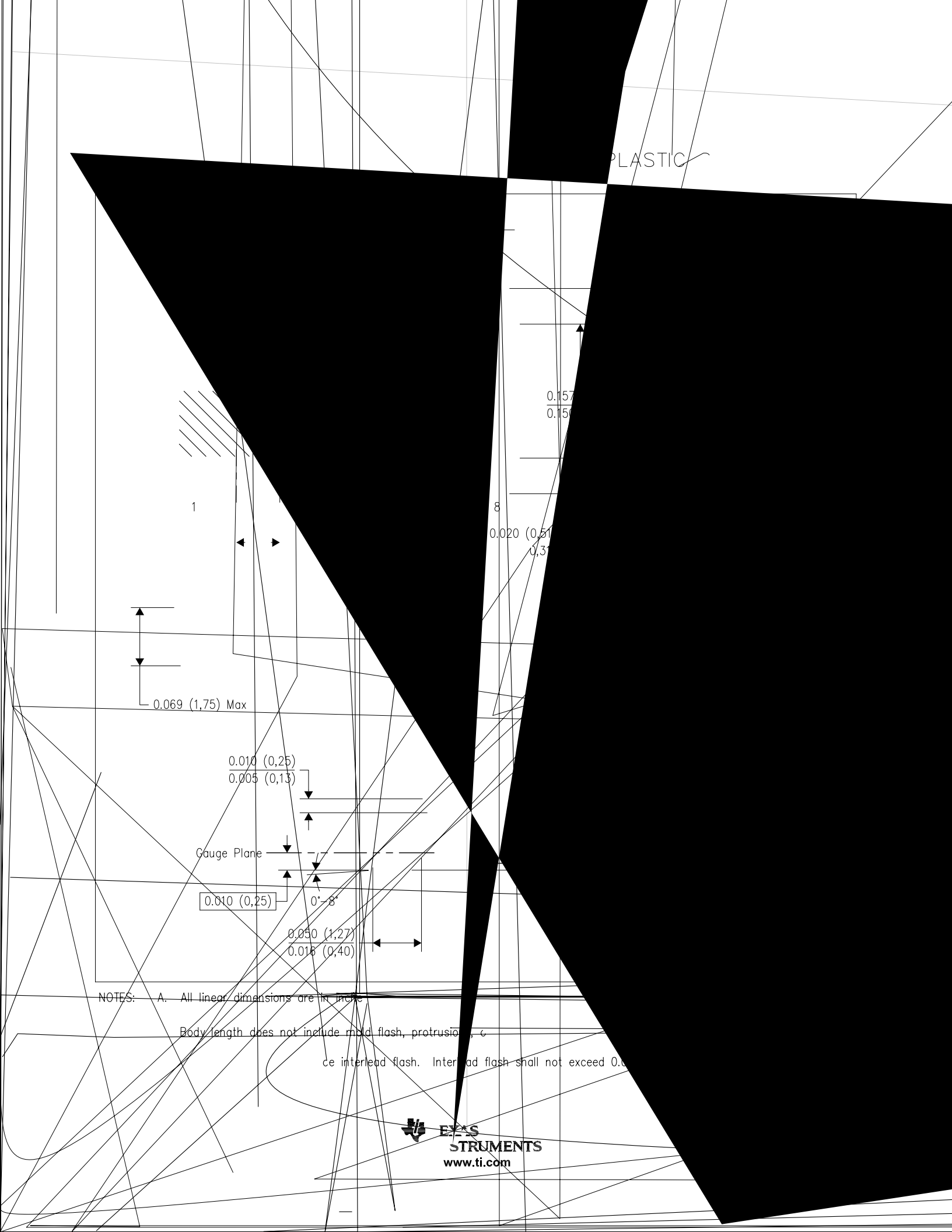
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS):



NOTES: A. All linear dimensions are in inche

Body length does not include mold flash, protrusio , c

ce interlead flash. Inter ad flash shall not exceed 0.

E S
STRUMENTS
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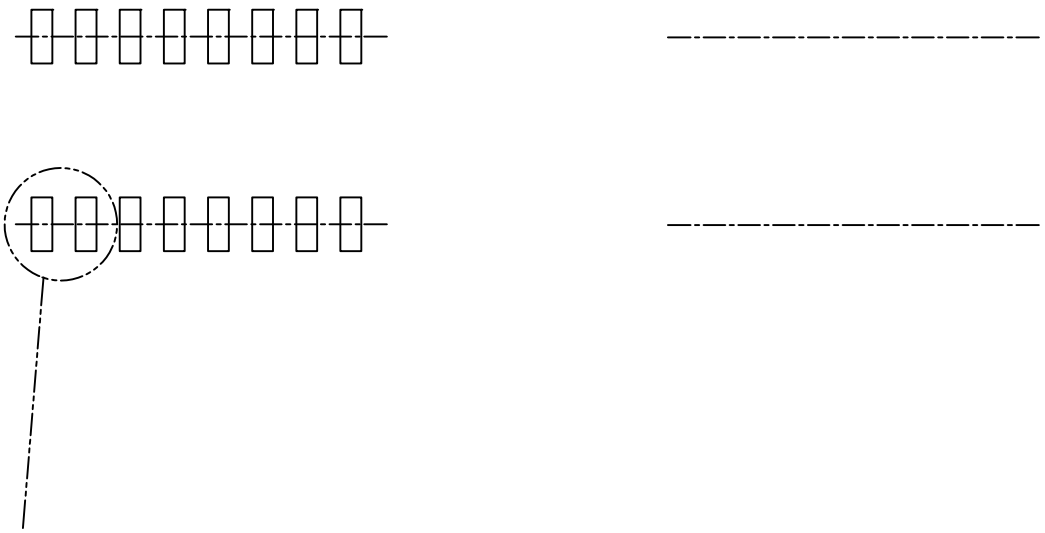
D (R–PDSO–G16) PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)



4211283–4/E 08/12

B. This drawing is s
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

Example
Pad Geometry
(See Note C)

Example

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