

## 8-Channel TFT-LCD Reference Voltage Generator

The EL5825 is designed to produce the reference voltages required in TFT-LCD applications. Each output is programmed to the required voltage with 10 bits of resolution. Reference pins determine the high and low voltages of the output range, which are capable of swinging to either supply rail. Programming of each output is performed using the serial interface. A serial out pin enables daisy chaining of multiple devices.

A number of the EL5825 can be stacked for applications requiring more than 8 outputs. The reference inputs can be tied to the rails, enabling each part to output the full voltage range, or alternatively, they can be connected to external resistors to split the output range and enable finer resolutions of the outputs.

The EL5825 has 8 outputs and is available in both the 24-pin TSSOP and the 24-pin QFN packages. It is specified for operation over the full -40°C to +85°C temperature range.

### Ordering Information

PART NUMBER	PACKAGE	TAPE & REEL	PKG. DWG. #
EL5825IL	24-Pin QFN	-	MDP0046
EL5825IL-T7	24-Pin QFN	7"	MDP0046
EL5825IL-T13	24-Pin QFN	13"	MDP0046
EL5825ILZ (See Note)	24-Pin QFN (Pb-free)	-	MDP0046
EL5825ILZ-T7 (See Note)	24-Pin QFN (Pb-free)	7"	MDP0046
EL5825ILZ-T13 (See Note)	24-Pin QFN (Pb-free)	13"	MDP0046
EL5825IR	24-Pin TSSOP	-	MDP0044
EL5825IR-T7	24-Pin TSSOP	7"	MDP0044
EL5825IR-T13	24-Pin TSSOP	13"	MDP0044
EL5825IRZ (See Note)	24-Pin TSSOP (Pb-free)	-	MDP0044
EL5825IRZ-T7 (See Note)	24-Pin TSSOP (Pb-free)	7"	MDP0044
EL5825IRZ-T13 (See Note)	24-Pin TSSOP (Pb-free)	13"	MDP0044

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

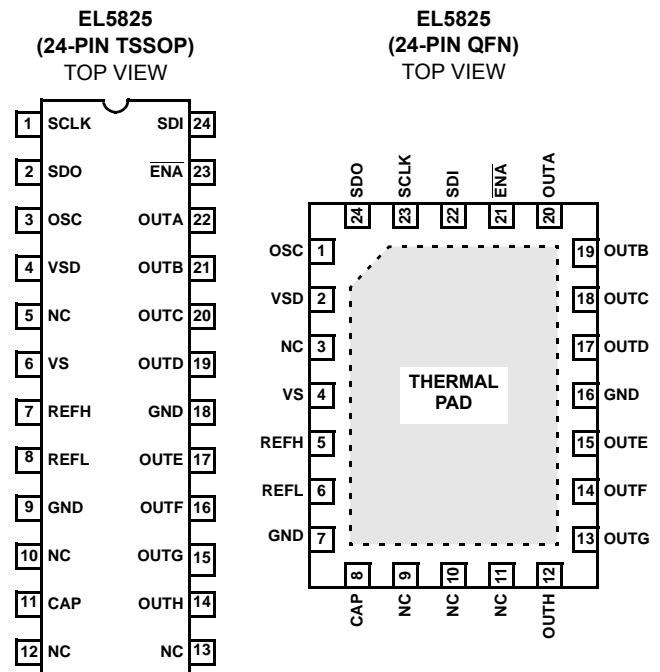
### Features

- 8-channel reference outputs
- Accuracy of  $\pm 0.1\%$
- Supply voltage of 4.5V to 16.5V
- Digital supply 3.3V to 5V
- Low supply current of 8mA
- Rail-to-rail capability
- Pb-Free plus anneal available (RoHS compliant)

### Applications

- TFT-LCD drive circuits
- Reference voltage generators

### Pinouts



**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Supply Voltage between $V_S$ and GND . . . . .	+18V	Ambient Operating Temperature . . . . .	-40°C to +85°C
Supply Voltage between $V_{SD}$ and GND . . . . .	$V_S$ and +7V (max)	Power Dissipation . . . . .	See Curves
Maximum Continuous Output Current . . . . .	30mA	Maximum Die Temperature . . . . .	125°C
		Storage Temperature . . . . .	-65°C to +150°C

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

**Electrical Specifications**  $V_S = 15\text{V}$ ,  $V_{SD} = 5\text{V}$ ,  $V_{REFH} = 13\text{V}$ ,  $V_{REFL} = 2\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  and  $C_L = 200\text{pF}$  to 0V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY</b>						
$I_S$	Supply Current	No load		7.6	9	mA
$I_{SD}$	Digital Supply Current			0.17	0.35	mA
<b>ANALOG</b>						
$V_{OL}$	Output Swing Low	Sinking 5mA ( $V_{REFH} = 15\text{V}$ , $V_{REFL} = 0$ )		50	150	mV
$V_{OH}$	Output Swing High	Sourcing 5mA ( $V_{REFH} = 15\text{V}$ , $V_{REFL} = 0$ )	14.85	14.95		V
$I_{SC}$	Short Circuit Current	$R_L = 10\Omega$	100	140		mA
PSRR	Power Supply Rejection Ratio	$V_{S+}$ is moved from 14V to 16V	45	60		dB
$t_D$	Program to Out Delay			4		ms
$V_{AC}$	Accuracy			20		mV
$V_{DROOP}$	Droop Voltage			1	2	mV/ms
$R_{INH}$	Input Resistance @ $V_{REFH}$ , $V_{REFL}$			34		$\text{k}\Omega$
REG	Load Regulation	$I_{OUT} = 5\text{mA}$ step		0.5	1.5	mV/mA
BG	Band Gap		1.1	1.3	1.6	V
<b>DIGITAL</b>						
$V_{IH}$	Logic 1 Input Voltage		$V_{SD} - 20\%$			V
$V_{IL}$	Logic 0 Input Voltage				20%* $V_{SD}$	V
$F_{CLK}$	Clock Frequency				5	MHz
$t_S$	Setup Time			20		ns
$t_H$	Hold Time			20		ns
$t_{LC}$	Load to Clock Time			20		ns
$t_{CE}$	Clock to Load Line			20		ns
$t_{DCO}$	Clock to Out Delay Time	Negative edge of SCLK		10		ns
$R_{SDIN}$	$SD_{IN}$ Input Resistance			1		$\text{G}\Omega$

**Pin Descriptions**

24-PIN QFN	24-PIN TSSOP	PIN NAME	PIN TYPE	PIN DESCRIPTION
1	3	OSC	IP/OP	Oscillator pin for synchronizing multiple chips
2	4	VSD	Power	Positive power supply for digital circuits (3.3V - 5V)
3	5	NC		Not connected
4	6	VS	Power	Positive supply voltage for analog circuits
5	7	REFH	Analog Input	High reference voltage
6	8	REFL	Analog Input	Low reference voltage
7	9	GND	Power	Ground
8	11	CAP	Analog	Decoupling capacitor for internal reference generator, 0.1 $\mu$ F
9	10	NC		Not connected
10	12	NC		Not connected
11	13	NC		Not connected
12	14	OUTH	Analog Output	Channel H programmable output voltage
13	15	OUTG	Analog Output	Channel G programmable output voltage
14	16	OUTF	Analog Output	Channel F programmable output voltage
15	17	OUTE	Analog Output	Channel E programmable output voltage
16	18	GND	Power	Ground
17	19	OUTD	Analog Output	Channel D programmable output voltage
18	20	OUTC	Analog Output	Channel C programmable output voltage
19	21	OUTB	Analog Output	Channel B programmable output voltage
20	22	OUTA	Analog Output	Channel A programmable output voltage
21	23	$\overline{\text{ENA}}$	Logic Input	Chip select, low enables data input to logic
22	24	SDI	Logic Input	Serial data input
23	1	SCLK	Logic Input	Serial data clock
24	2	SDO	Logic Output	Serial data output

Typical Performance Curves

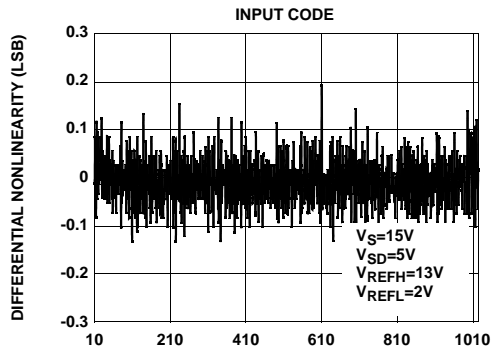


FIGURE 1. DIFFERENTIAL NONLINEARITY vs CODE

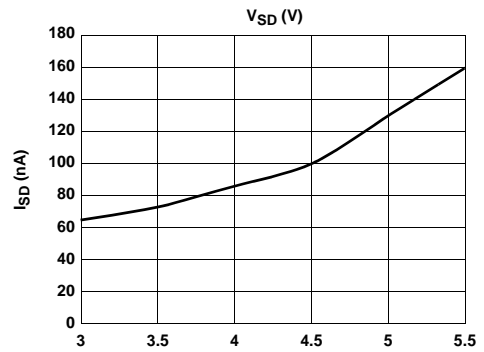


FIGURE 2. DIGITAL SUPPLY CURRENT vs DIGITAL SUPPLY VOLTAGE

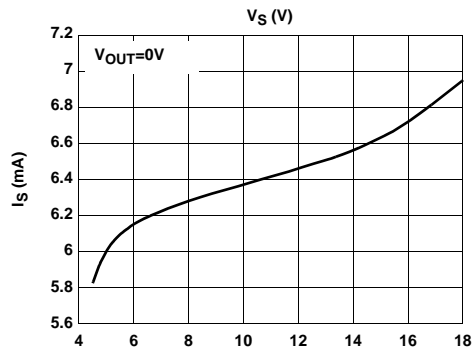


FIGURE 3. SUPPLY CURRENT vs SUPPLY VOLTAGE

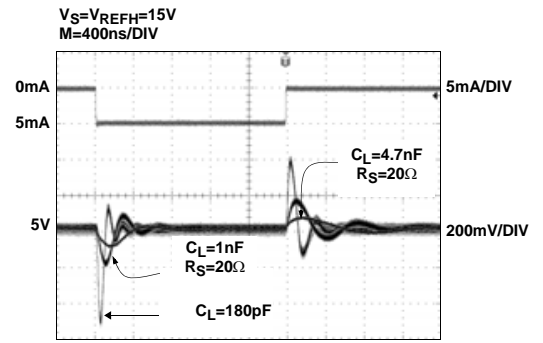


FIGURE 4. TRANSIENT LOAD REGULATION (SOURCING)

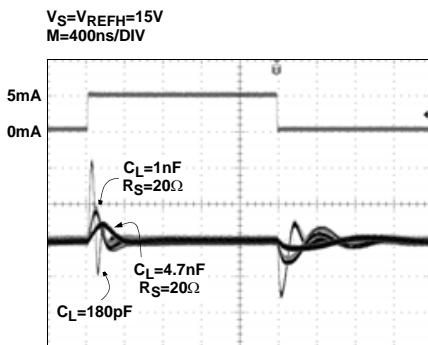


FIGURE 5. TRANSIENT LOAD REGULATION (SINKING)

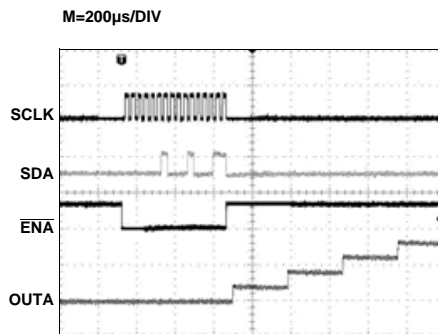


FIGURE 6. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

Typical Performance Curves (Continued)

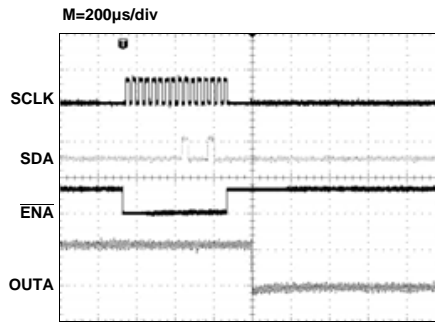


FIGURE 7. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 100mV)

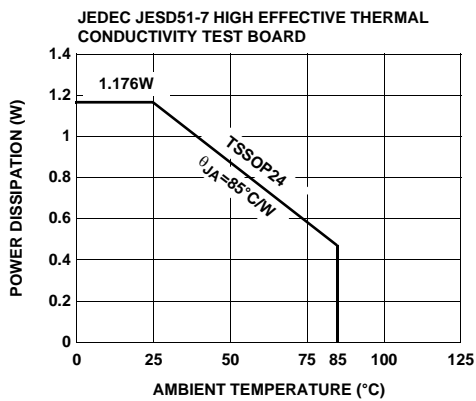


FIGURE 8. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

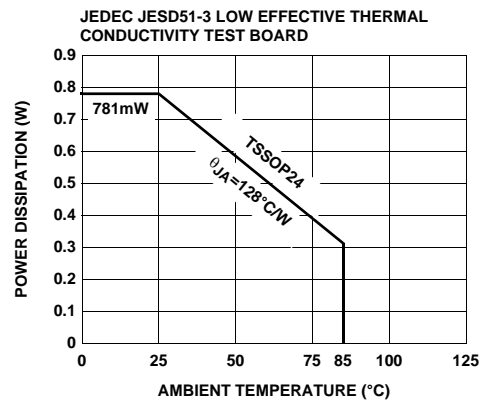


FIGURE 9. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

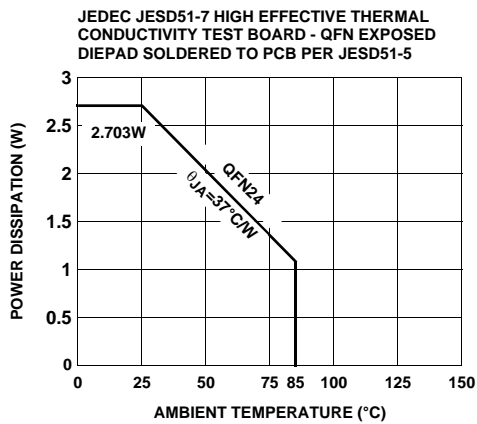


FIGURE 10. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

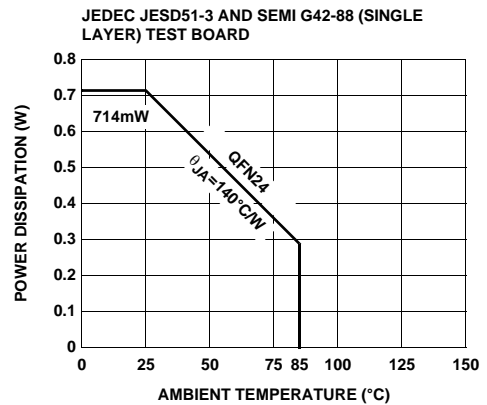


FIGURE 11. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

**Product Description**

The EL5825 provides a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels.

The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear; however, if the panel is to be used in more than one application, the final curve may differ for different applications.

By using the EL5825, this curve can be changed to optimize its characteristics according to the required application of the display product.

Each of the reference voltage outputs can be set with a 10-bit resolution. These outputs are available to within 100mV of the power rails of the EL5825.

As all of the output buffers are identical, it is also possible to use the EL5825 for applications other than LCDs where 8 voltage references are required that can be set to a 10-bit accuracy.

**Serial Interface**

The EL5825 is programmed through a three-wire serial interface. The start and stop conditions are defined by the ENA signal. While the ENA is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The MSB (bit 15) is loaded first and the LSB (bit 0) is loaded last (see Table 1). After the full 16-bit data has been loaded, the ENA is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the ENA is high. The SCLK must be low before the ENA is pulled low.

To facilitate the system designs that use multiple EL5825 chips, a buffered serial output of the shift register (SDO pin) is available. Data appears on the SDO pin at the 16th falling SCLK edge after being applied to the SDI pin.

To control the multiple EL5825 chips from a single three-wire serial port, just connect the ENA pins and the SCLK pins together, connect the SDO pin to the SDI pin on the next chip. While the ENA is held low, the 16m-bit data is loaded to the SDI input of the first chip. The first 16-bit data will go to the last chip and the last 16-bit data will go to the first chip. While the ENA is held high, all addressed outputs will be updated simultaneously.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

The serial data has a minimum length of 16 bits, the MSB (most significant bit) is the first bit in the signal. The bits are

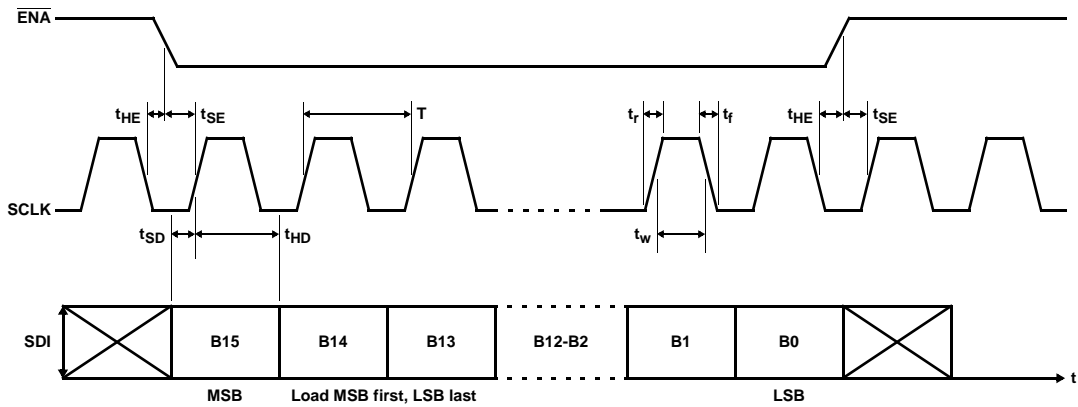
allocated to the following functions (also refer to the Control Bits Logic Table)

- Bit 15 is always set to a zero
- Bit 14 controls the source of the clock, see the next section for details
- Bits 13 through 10 select the channel to be written to, these are binary coded with channel A = 0, and channel H = 7
- The 10-bit data is on bits 9 through 0. Some examples of data words are shown in the table of Serial Programming Examples

**TABLE 1. CONTROL BITS LOGIC TABLE**

BIT	NAME	DESCRIPTION
B15	Test	Always 0
B14	Oscillator	0 = Internal, 1 = External
B13	A3	Channel Address (don't care)
B12	A2	Channel Address
B11	A1	Channel Address
B10	A0	Channel Address
B9	D9	Data
B8	D8	Data
B7	D7	Data
B6	D6	Data
B5	D5	Data
B4	D4	Data
B3	D3	Data
B2	D2	Data
B1	D1	Data
B0	D0	Data

**Serial Timing Diagram**



**TABLE 2. SERIAL TIMING PARAMETERS**

PARAMETER	EXAMPLE	DESCRIPTION
T	$\geq 200\text{ns}$	Clock Period
$t_r/t_f$	$0.05 * T$	Clock Rise/Fall Time
$t_{HE}$	$\geq 10\text{ns}$	$\overline{\text{ENA}}$ Hold Time
$t_{SE}$	$\geq 10\text{ns}$	$\overline{\text{ENA}}$ Setup Time
$t_{HD}$	$\geq 10\text{ns}$	Data Hold Time
$t_{SD}$	$\geq 10\text{ns}$	Data Setup Time
$t_w$	$0.50 * T$	Clock Pulse Width

**TABLE 3. SERIAL PROGRAMMING EXAMPLES**

CONTROL		CHANNEL ADDRESS				DATA										CONDITION
C1	C0	A3	A2	A1	A0	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	X	0	0	0	0	0	0	0	0	0	0	0	0	0	Internal Oscillator, Channel A, Value = 0
0	0	X	0	0	0	1	1	1	1	1	1	1	1	1	1	Internal Oscillator, Channel A, Value = 1023
0	0	X	0	0	0	1	0	0	0	0	0	0	0	0	0	Internal Oscillator, Channel A, Value = 512
0	0	X	0	1	1	1	0	0	0	0	0	0	0	0	1	Internal Oscillator, Channel C, Value = 513
0	0	X	1	1	1	0	0	0	0	0	1	1	1	1	1	Internal Oscillator, Channel H, Value = 31
0	1	X	1	1	1	0	0	0	0	0	1	1	1	1	1	External Oscillator, Channel H, Value = 31

**Internal Refresh Clock Oscillator**

The EL5825 requires an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labeled OSC. The internal clock is provided by an internal oscillator running at approximately 25kHz and can be output to the OSC pin. In a multiple chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. Subsequent chips may have the OSC pin connected to this clock source. In these chips, the program will set them to external OSC Mode by setting bit 14 to 1. See the control bits logic table and serial programming example for details.

For transient load application, the external clock Mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing on page 10 shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the OSC pin will be in a high impedance

condition to prevent contention. After programming the oscillator with bit 14, the pin will be set to the appropriate mode.

**Transfer Function**

The transfer function is:

$$V_{OUT(IDEAL)} = V_{REFL} + \frac{data}{1024} \times (V_{REFH} - V_{REFL})$$

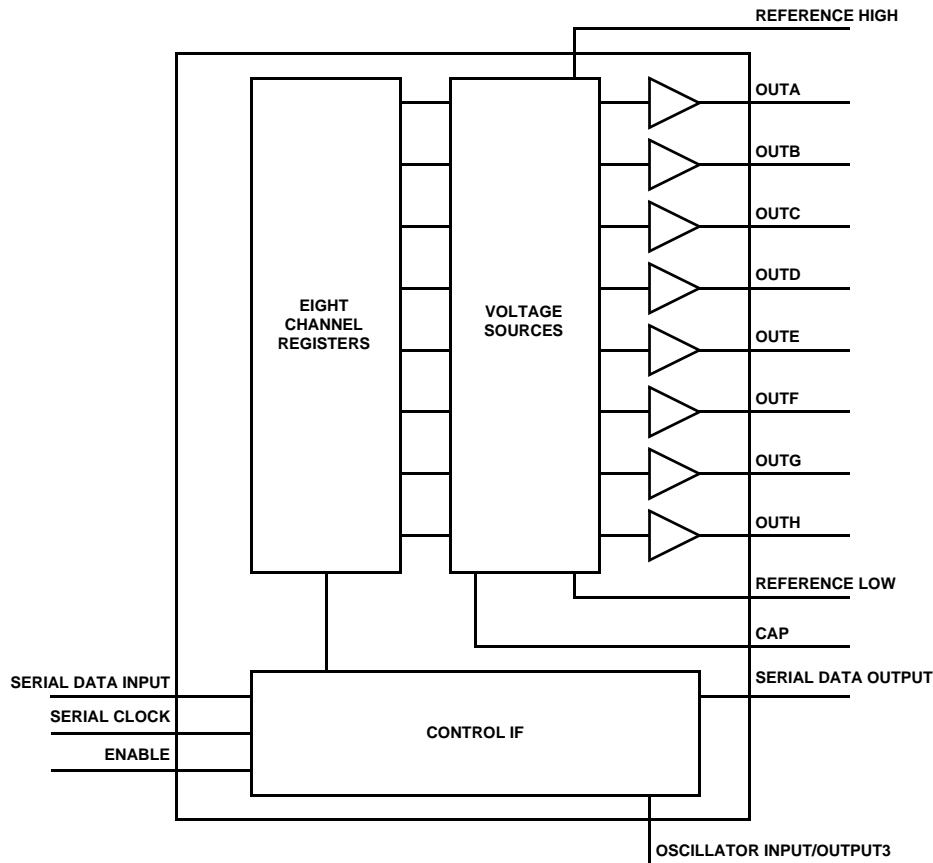
where data is the decimal value of the 10-bit data binary input code.

The output voltages from the EL5825 will be derived from the reference voltages present at the  $V_{REFL}$  and  $V_{REFH}$  pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5825.  $GND < V_{REFH} \leq V_S$  and  $GND \leq V_{REFL} \leq V_{REFH}$ .

In some LCD applications that require more than 8 channels, the system can be designed such that one EL5825 will provide the Gamma correction voltages that are more positive than the  $V_{COM}$  potential. The second EL5825 can provide the Gamma correction voltage more negative than the  $V_{COM}$  potential. The Application Drawing on page 10 shows a system connected in this way.

**Block Diagram**





**Channel Outputs**

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 100mV of the power rails, (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 40μs. In the worst-case scenario this will be 320μs, when the data has just missed the cycle.

When a large change in output voltage is required, the change will occur in 2 volt steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16 volts can take between 2.56 milliseconds and 3 milliseconds depending on the absolute timing relative to the update cycle.

**Power Dissipation**

With the 30mA maximum continues output drive capability for each channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

- $T_{JMAX}$  = Maximum junction temperature
- $T_{AMAX}$  = Maximum ambient temperature
- $\theta_{JA}$  = Thermal resistance of the package
- $P_{DMAX}$  = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{DMAX} = V_S \times I_S + \Sigma[(V_S - V_{OUT}^i) \times I_{LOAD}^i]$$

when sourcing, and:

$$P_{DMAX} = V_S \times I_S + \Sigma(V_{OUT}^i \times I_{LOAD}^i)$$

when sinking.

Where:

- $i = 1$  to total 8
- $V_S$  = Supply voltage
- $I_S$  = Quiescent current
- $V_{OUT}^i$  = Output voltage of the  $i$  channel
- $I_{LOAD}^i$  = Load current of the  $i$  channel

By setting the two  $P_{DMAX}$  equations equal to each other, We can solve for the  $R_{LOAD}$ 's to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

**Power Supply Bypassing and Printed Circuit Board Layout**

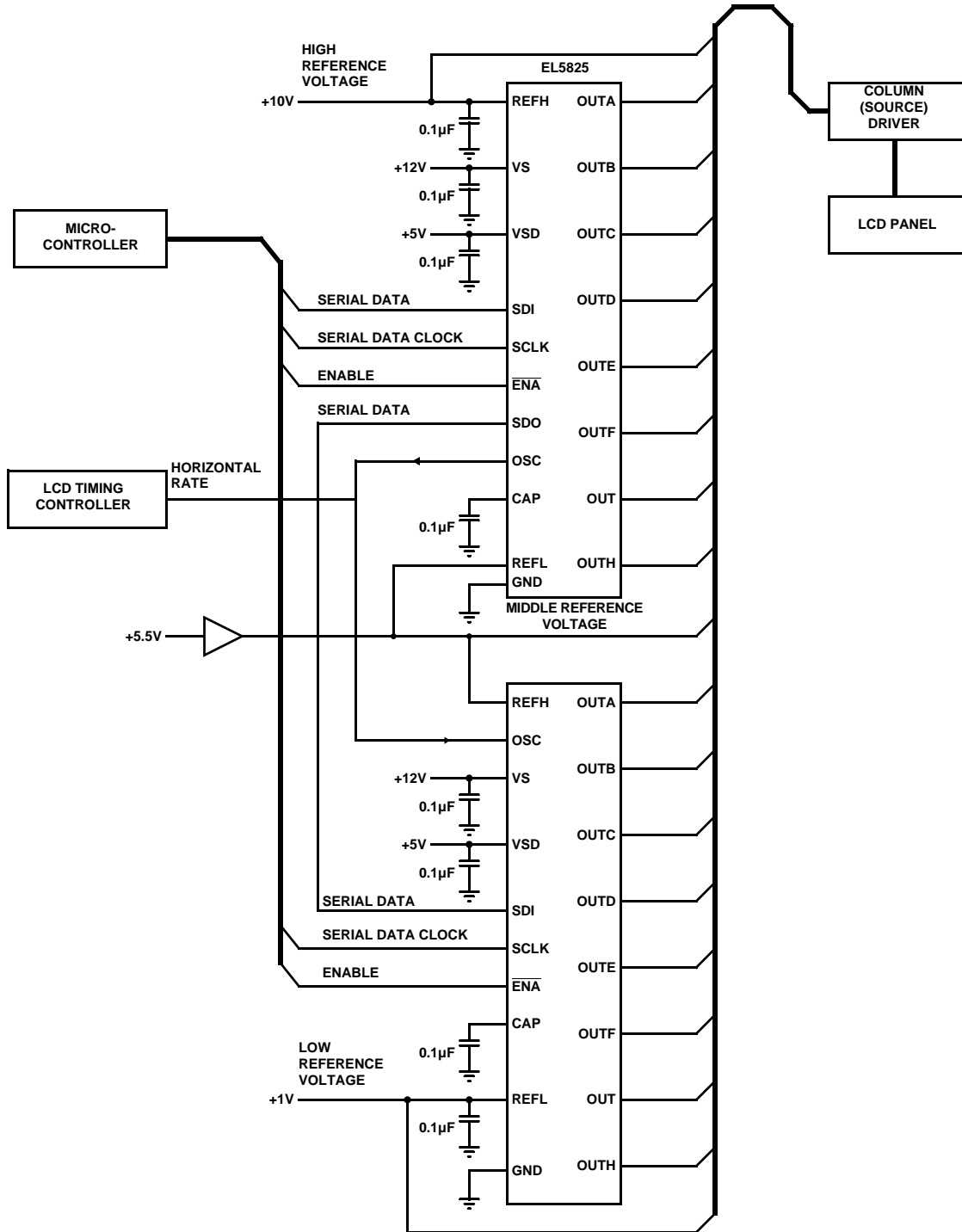
Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5825. The traces from the two ground pins to the ground plane must be very short. The thermal pad of the EL5825 should be connected to the analog ground plane. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1μF ceramic capacitor must be place very close to the  $V_S$ ,  $V_{REFH}$ ,  $V_{REFL}$ , and CAP pins. A 4.7μF local bypass tantalum capacitor should be placed to the  $V_S$ ,  $V_{REFH}$ , and  $V_{REFL}$  pins.

**Application Using the EL5825**

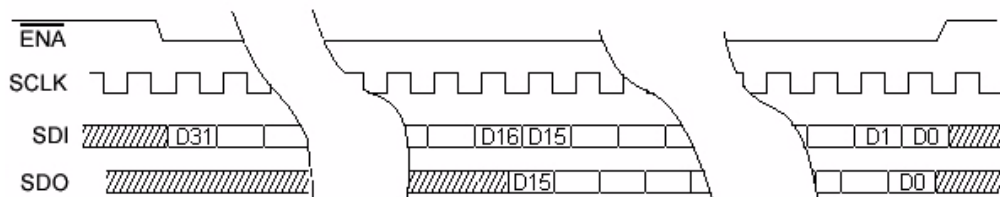
In the application drawing, the schematic shows the interconnect of a pair of EL5825 chips connected to give 8 gamma corrected voltages above the  $V_{COM}$  voltage, and 8 gamma corrected voltages below the  $V_{COM}$  voltage.

By using the serial data out pin, it is possible to daisy chain (cascade) the two chips. In this mode the micro-controller will send a 32-bit word that will update both the upper and lower references voltages in one operation. See Application Drawing 1 for details.

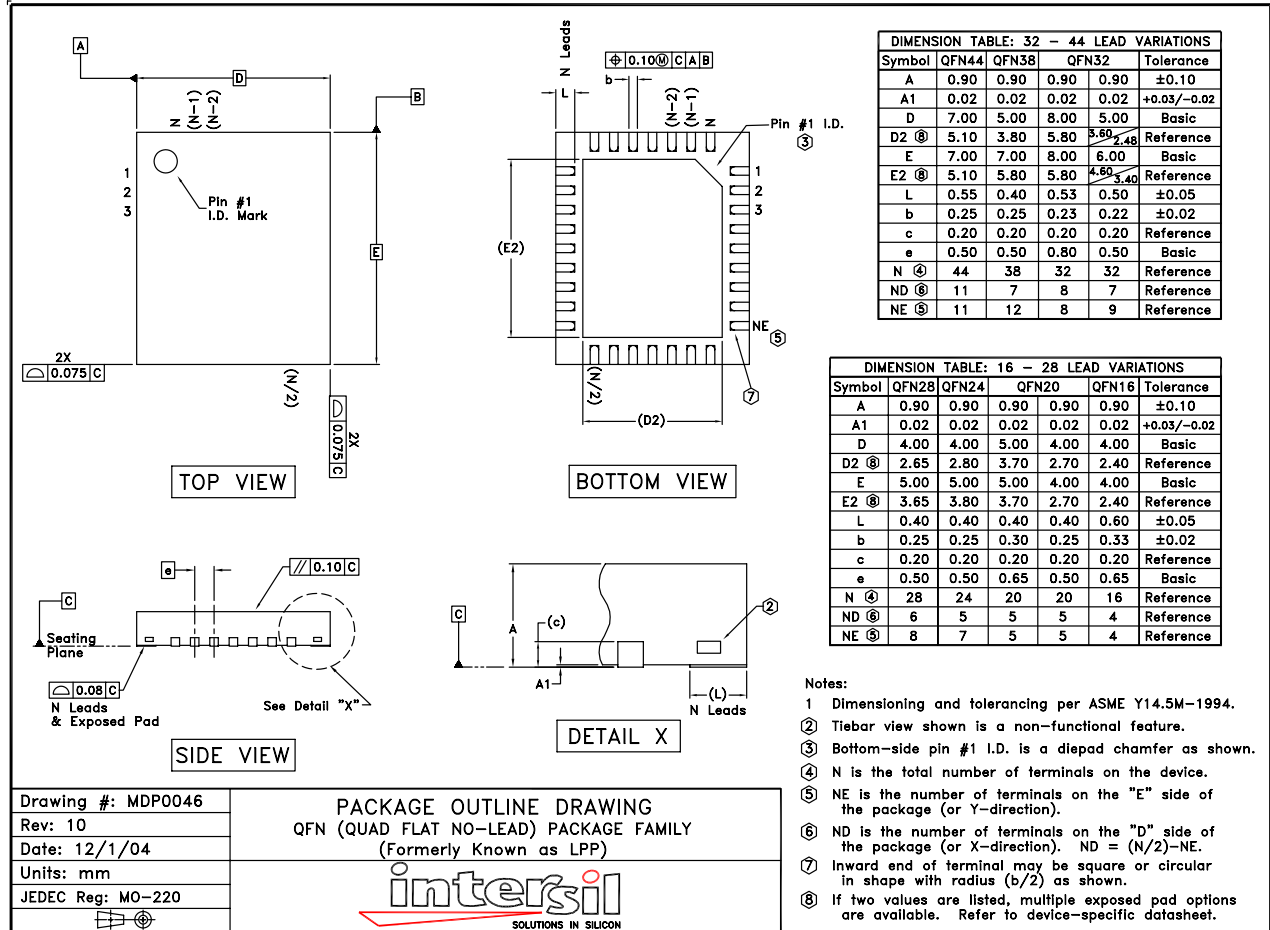
Application Drawing




Serial Timing Diagram (32 bit)

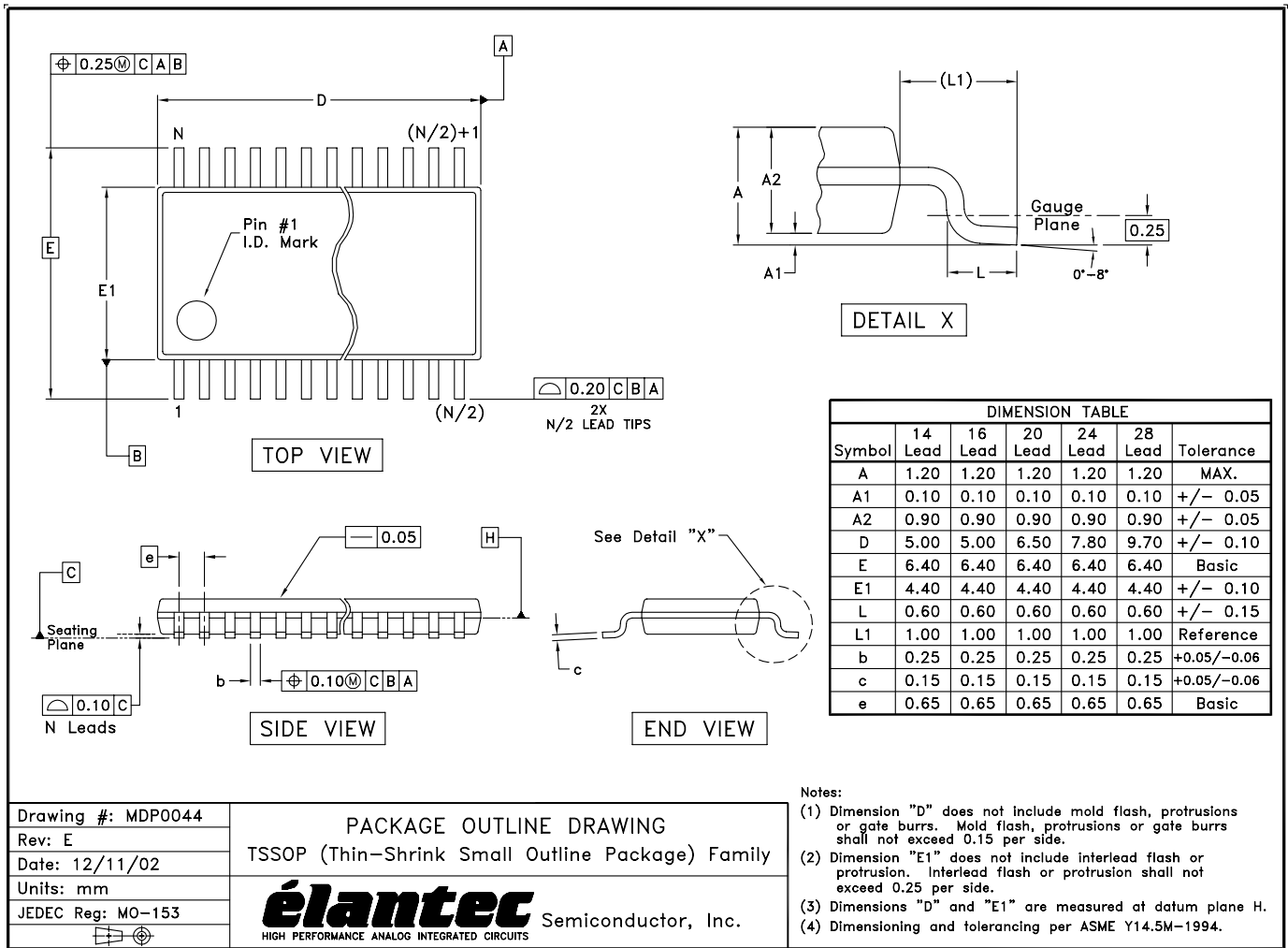


QFN Package Outline Drawing



Drawing #: MDP0046	PACKAGE OUTLINE DRAWING QFN (QUAD FLAT NO-LEAD) PACKAGE FAMILY (Formerly Known as LPP)  SOLUTIONS IN SILICON
Rev: 10	
Date: 12/1/04	
Units: mm	
JEDEC Reg: MO-220	

TSSOP Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <<http://www.intersil.com/design/packages/index.asp>>

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems. Intersil Corporation's quality certifications can be viewed at [www.intersil.com/design/quality](http://www.intersil.com/design/quality)

Intersil products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design, software and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)