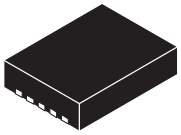


Li-Ion AND Li-Pol BATTERY GAS GAUGE IC FOR PORTABLE APPLICATIONS (bqJUNIOR)

FEATURES

- **HDQ (bq27010) or I²C (bq27210) Communication**
- **Reports Accurate *Time-to-Empty* At Both Measured and Host-Requested Load Values**
- **Reports Available Capacity Compensated for Discharge Rate, Temperature, and Age**
- **End-of-Discharge Voltage Compensated for Discharge Rate and Temperature**
- **Automatic Capacity Reduction with Age**
- **Reports Temperature, Voltage, and Current**
- **High Accuracy Charge and Discharge Current Integration with Automatic Offset Calibration**
- **Requires No User Calibration**
- **Programmable Input/Output Port**
- **Internal User EEPROM Configuration Memory**
- **Uploadable Coefficients Allows Host-Side Use with Multiple Pack Characteristics**
- **Stable Oscillator Without External Components**
- **Dynamic End-of-Discharge Detection Delay to Allow Use in a High-Dynamic Load Environment**
- **Automatic Sleep Mode When Communication Lines are Low**
- **Available in a Small 3 mm x 4 mm QFN Package**
- **Five Low-Power Operating Modes**
  - **Active: < 90 µA**
  - **Sleep: < 2.5 µA**
  - **Ship: < 2 µA (bq27010 only)**
  - **Hibernate: < 1.5 µA**
  - **Data Retention: < 20 nA**

APPLICATIONS

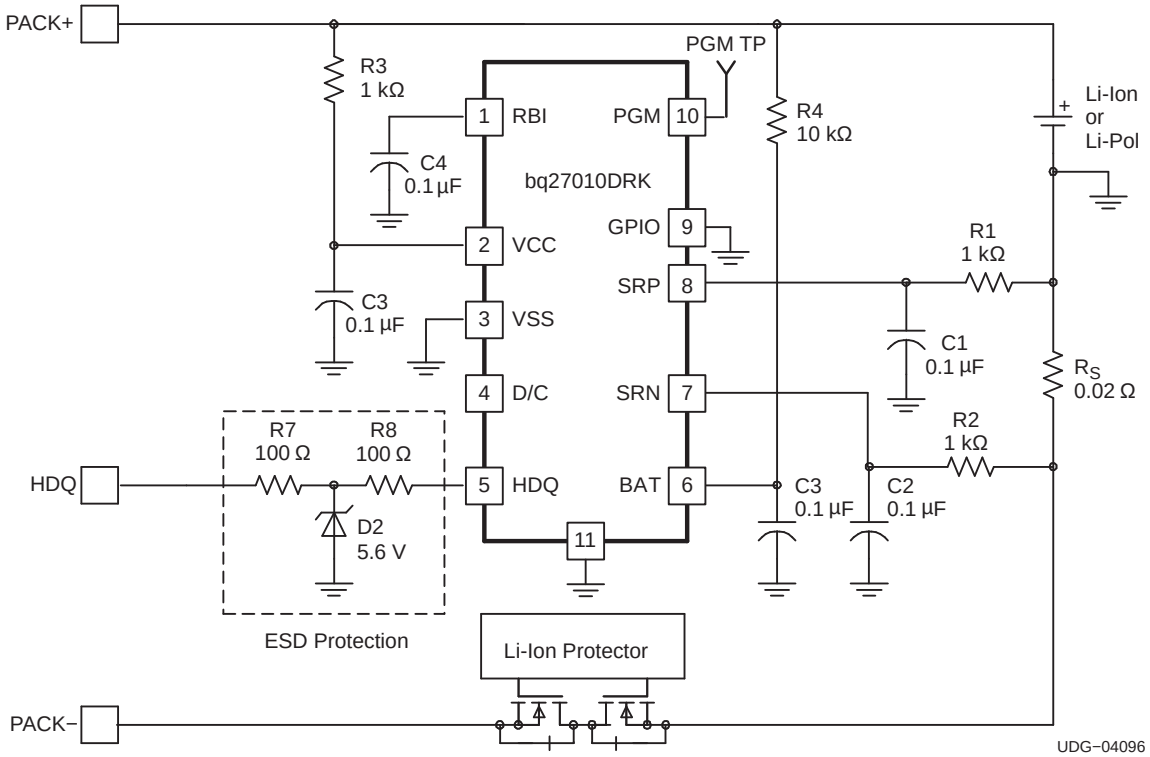
- **PDA**
- **Smart Phones**
- **MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Handheld Devices**

DESCRIPTION

The bqJUNIOR™ series are highly accurate stand-alone single-cell Li-Ion and Li-Pol battery capacity monitoring and reporting devices targeted at space-limited, portable applications. The IC monitors a voltage drop across a small current sense resistor connected in series with the battery to determine charge and discharge activity of the battery. Compensations for battery age, temperature, self-discharge, and discharge rate are applied to the capacity measurments to provide available time-to-empty information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or learned, in the course of a discharge cycle from full to empty. Internal registers include current, capacity, time-to-empty, state-of-charge, cell temperature and voltage, status, and more.

The bqJUNIOR can operate directly from single-cell Li-Ion and Li-Pol batteries and communicates to the system over a HDQ one-wire or I²C serial interface.

TYPICAL APPLICATION



ORDERING INFORMATION

TA	COMMUNICATION INTERFACE	PACKAGED DEVICES(1)	MARKINGS
-20°C to 70°C	HDQ	bq27010DRKR	27010
	I^2C	bq27210DRKR	27210

(1) The DRK package is available taped and reeled only. Quantities are 2,000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			bq27010 bq27210	UNITS
V_{CC}	Supply voltage	(with respect to V_{SS})	–0.3 to 7	V
V_{IN}	Input voltage	SRP, SRN, RBI, BAT (all with respect to V_{SS})	–0.3 to V_{CC}+0.3	
		HDQ, SCL, SDA, GPIO (all with respect to V_{SS})	–0.3 to 7	
		PGM (with respect to V_{SS}) during EEPROM programming	–0.3 to 22	
I_{SINK}	Output sink current	GPIO, SCL, SDA, HDQ	5	mA
T_A	Operating free-air temperature range		–20 to 70	°C
T_{stg}	Storage temperature range		–65 to 150	
T_J	Operating junction temperature range		–40 to 125	
	Lead temperature (soldering, 10 sec)		300	

RECOMMENDED OPERATING CONDITIONS

ELECTRICAL CHARACTERISTICS

TIMING DIAGRAMS

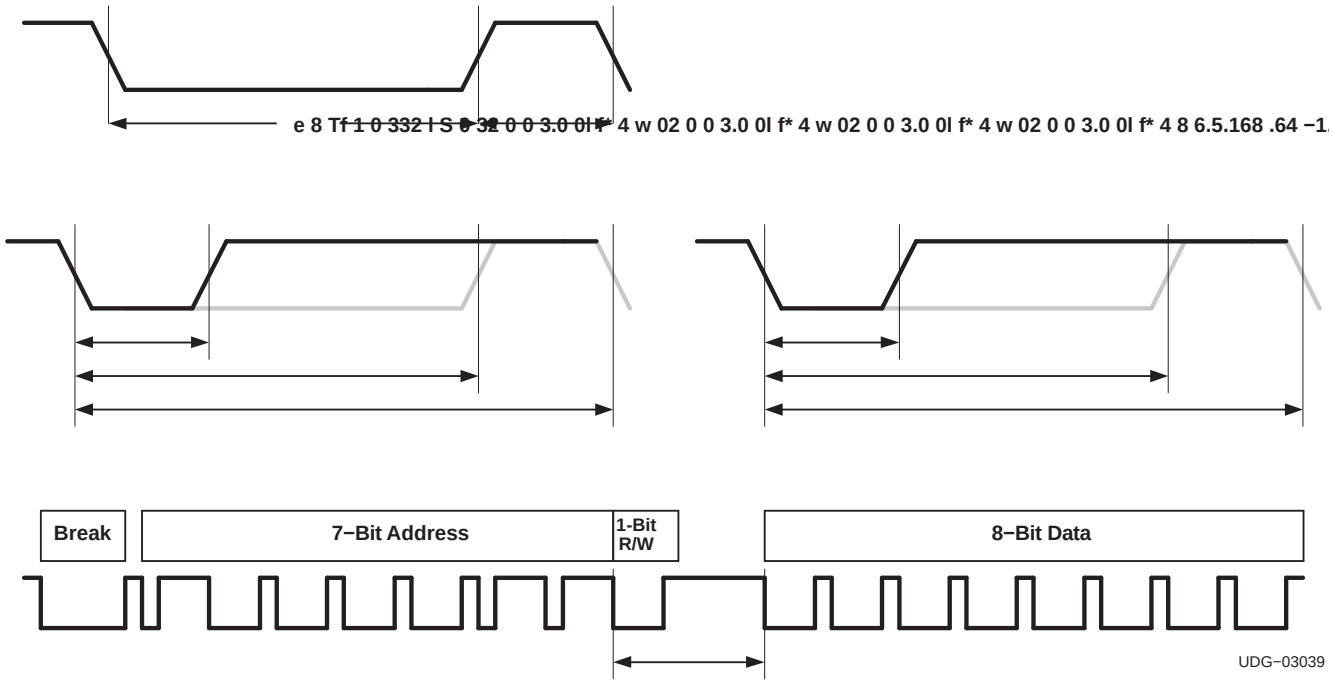


Figure 1. HDQ Bit Timing Diagram

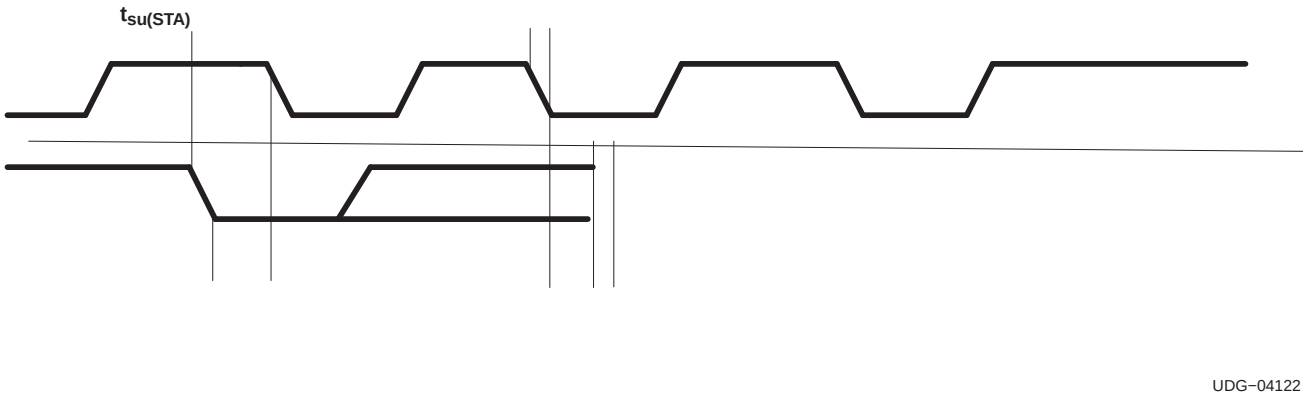
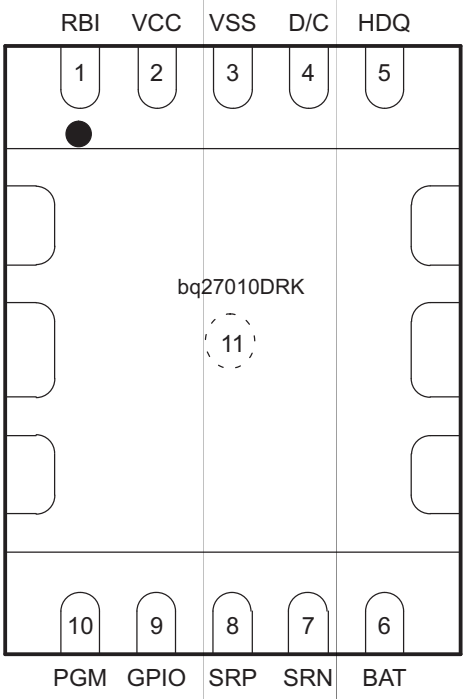
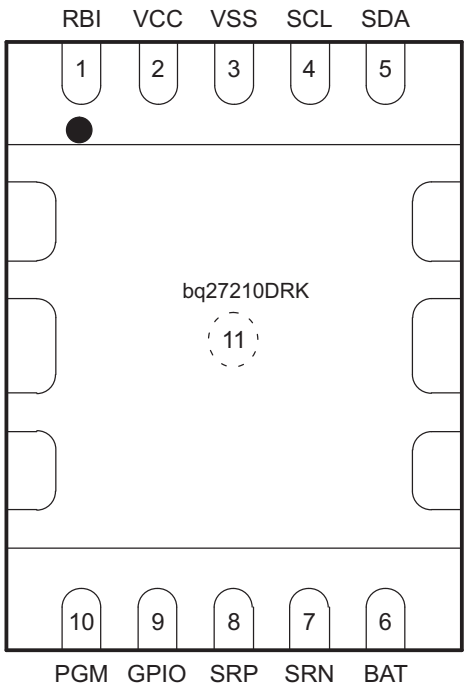


Figure 2. I²C Timing Diagram

BQ27010
DRK PACKAGE
(BOTTOM VIEW)

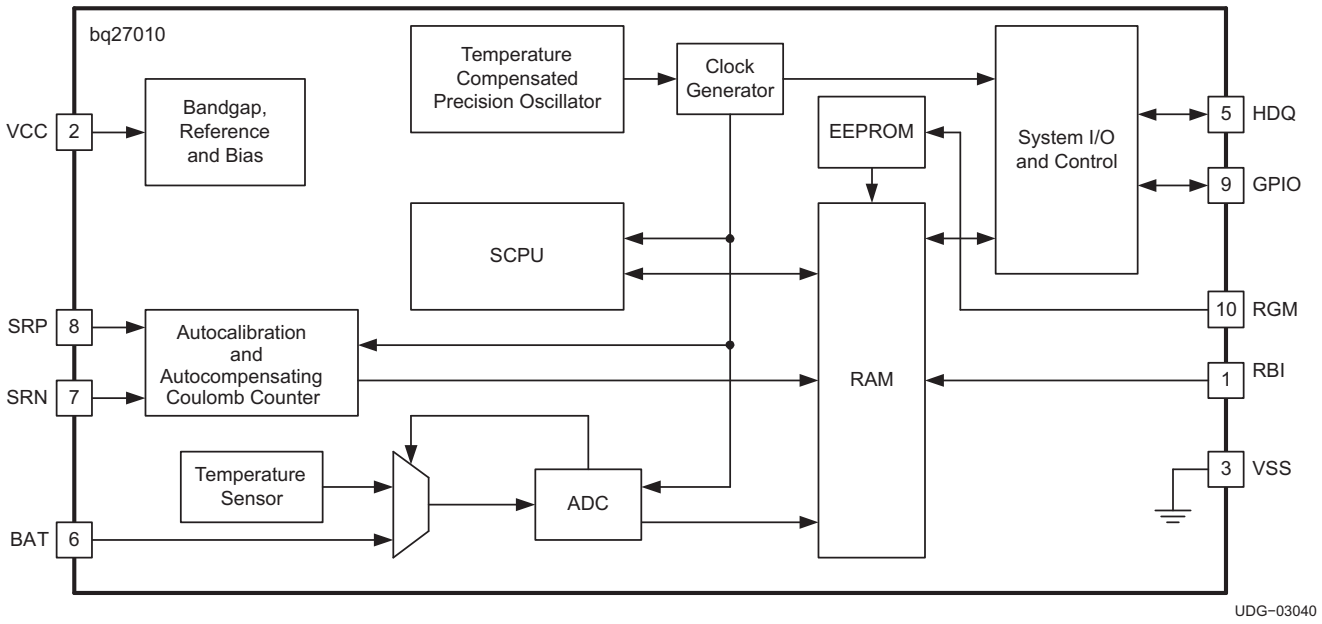


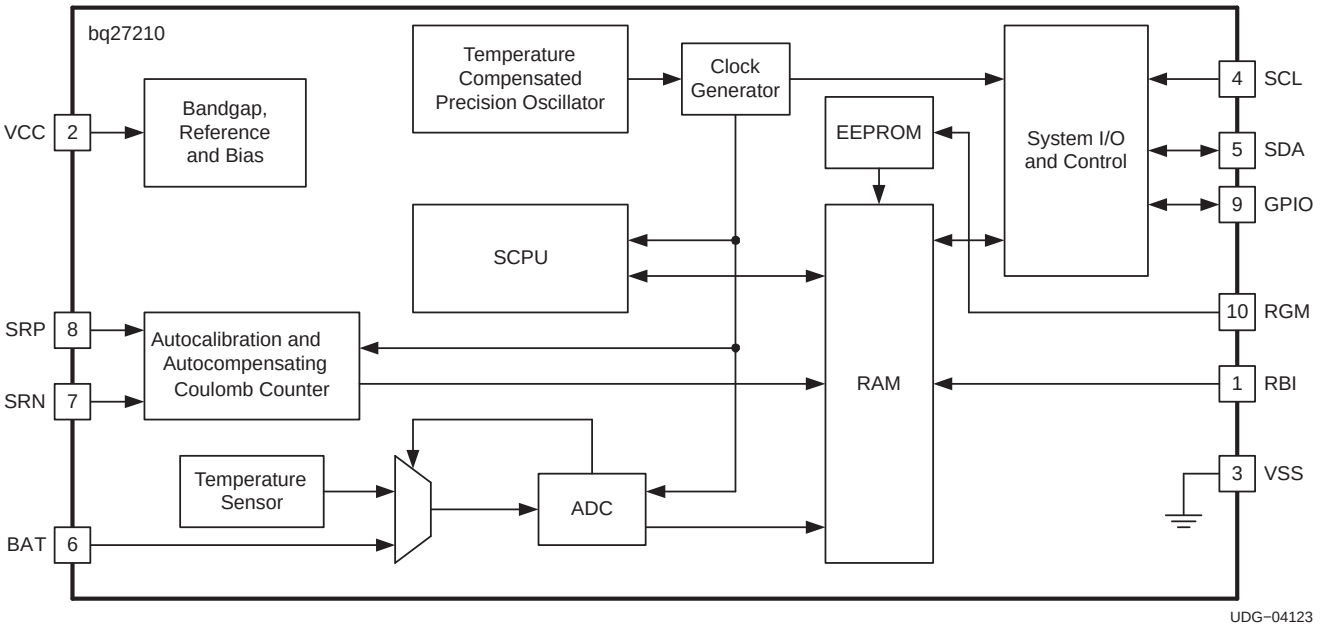
BQ27210
DRK PACKAGE
(BOTTOM VIEW)



DEVICE INFORMATION

FUNCTIONAL BLOCK DIAGRAMS





FUNCTIONAL DESCRIPTION

The bqJUNIOR determines battery capacity by monitoring the amount of charge input to or removed from a Li-Ion or Li-Pol battery. The bqJUNIOR measures discharge and charge currents, monitors the battery for low voltage thresholds, and compensates for self-discharge, aging, temperature, and discharge rate. Current is measured across a small value series resistor between the negative terminal of the battery and the pack ground (see R_S in Figure 3). Available

FUNCTIONAL DESCRIPTION (continued)

Figure 3 shows a typical application circuit. Differential sense of the voltage across the current sense resistor, R_S, improves device performance, leading to an improvement in reported time-to-empty accuracy. An internal 3-µA pull-down on the HDQ or SDA and SCL lines ensures that the device detects a logic *0* on the communication lines and allows the device to automatically enter the low-power sleep mode when the system power is switched off or the pack is removed. A 100 kΩ pullup to V_{CC} can be added to the communication lines if this feature needs to be disabled. The bqJUNIOR can operate directly from a single Li-Ion or Li-Pol cell.

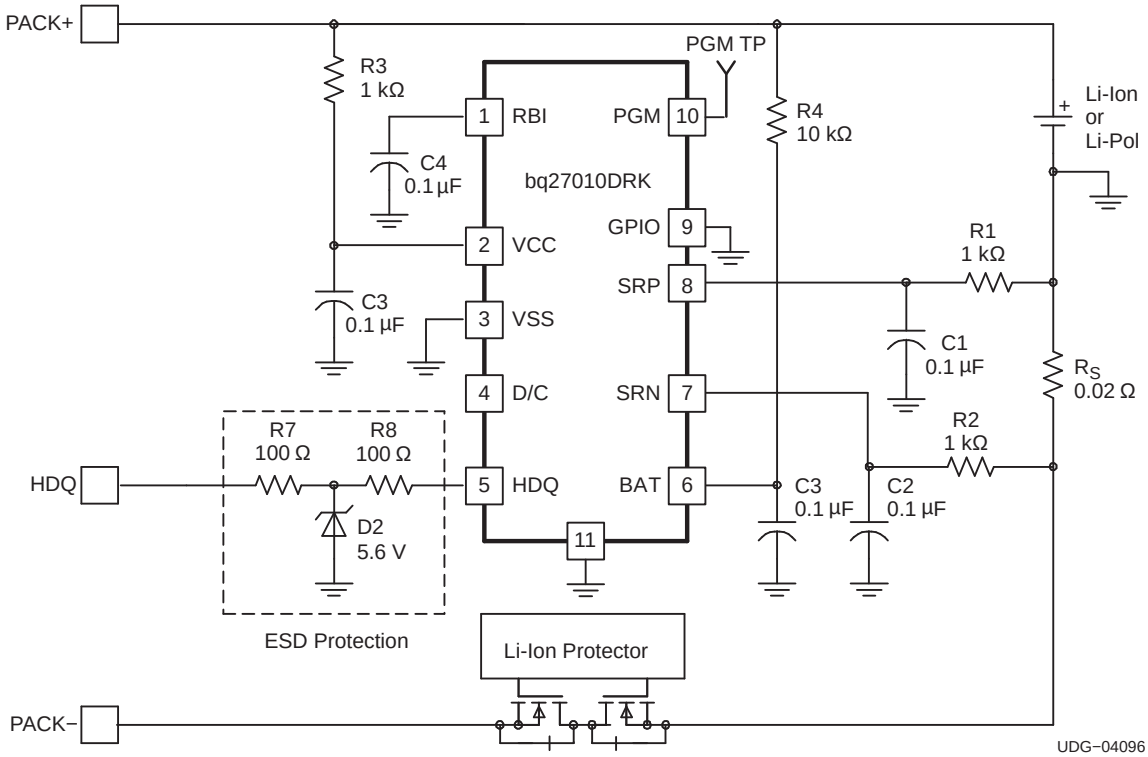


Figure 3. Typical Application Circuit (bq27010)

Measurements

As shown in the functional block diagram, the bqJUNIOR uses a dedicated fully differential Delta-Sigma Coulomb Counter (DSCC) for charge and discharge current and coulometric measurements and an analog-to-digital converter (ADC) for battery voltage and temperature measurements. Both DSCC and ADC are automatically compensated for offset. No user calibration or compensation is required. An EEPROM offset value can be programmed to compensate for contributions to the DSCC offset due to the PCB layout.

Charge and Discharge Coulometric and Current Measurements

The bqJUNIOR uses a DSCC to perform a continuous integration of the voltage waveform across a small value sense resistor in the negative lead of the battery, as shown in Figure 3. The integration of the voltage across the sense resistor is the charge added

FUNCTIONAL DESCRIPTION (continued)

Offset Calibration

The offset voltage of the DSCC measurement must be very low to be able to measure small signal levels accurately. The bqJUNIOR provides an auto-calibration feature to cancel the internal voltage offset error across SRP and SRN for maximum charge measurement accuracy. **NO CALIBRATION IS REQUIRED**. External voltage offset error caused by the PCB layout cannot be automatically calibrated out by the gauge, but the external offset can be determined using a built-in user offset measurement command and can be programmed into the EEPROM for inclusion in the offset compensation performed by the gauge. See the *Layout Considerations* section for details on minimizing PCB induced offset across the SRP and SRN pins.

The bqJUNIOR auto-calibration of the DSCC offset is performed from time-to-time as operating conditions change, to keep the measurement error small. A Calibration-In-Progress (CALIP) flag is set in FLAGS to indicate when the operation occurs. Capacity, voltage, and temperature is updated during the 5.12 second offset calibration time, but other parameters are not updated until the calibration has completed. When there is a full reset, the gauge makes an initial quick offset calibration and delays the 5.12 second full offset calibration for at least 40 seconds. This is done to prevent the full 5.12 second calibration operation from interfering with module test functions that need to be performed immediately after power application during manufacturing test. The quick offset calibration after a full reset is a 1.28 second offset measurment used as a delay, followed by a 1.28 second offset measurement that is used as the initial offset value. The 1.28 second delay allows V_{CC} to settle before the initial offset measurement. If manufacturing test does not need the additional V_{CC} settling time or can use a slightly worse initial offset measurement, the tester may write bit *0* of CTRL (address 0x00) to *1* during the first 1.28 seconds after the reset and the first offset sample will be used, cutting the initial quick offset calibration time in half.

Digital Magnitude Filter

The Digital Magnitude Filter (DMF) threshold can be set in EEPROM to indicate a threshold below which any charge or discharge accumulation is ignored. This allows setting a threshold above the maximum DSCC offset expected from the IC and PCB combination, so that when no charge or discharge current is present, the measured capacity change by the bqJUNIOR is zero. Note that even a small offset can add up to a large error over a long period. In addition to setting the threshold above the largest offset expected, the DMF should be set below the minimum signal level to be measured. The sense resistor value should be large enough to allow the minimum current level to provide a signal level substantially higher than the maximum offset voltage. Conversely, the sense resistor must be small enough to meet the system requirement for insertion loss as well as keep the maximum voltage across the sense resistor below the 100 mV maximum that the DSCC can accurately measure.

The DMF threshold is programmed in EEPROM in increments of 4.9 µV. Programming a zero in the DMF value will disable the DMF function and all non-zero DSCC measurements are counted.

Voltage

The bqJUNIOR monitors the battery voltage through the BAT pin and reports an offset corrected value through the internal registers. The bqJUNIOR also monitors the voltage for the end-of-discharge (EDV) thresholds. The EDV threshold levels are used to determine when the battery has been discharged to 6.25% or *empty* and synchronizes the reported capacity to these levels when the programmed EDV thresholds are detected.

Temperature

The bqJUNIOR uses an integrated temperature sensor to monitor the pack temperature and is reported through the internal registers. The temperature measurement is used to adjust compensated available capacity and self-discharge capacity loss.

RBI Input

The Register Backup Current (RBI) input pin is used with an external capacitor to provide backup potential to the internal registers when V_{CC} drops below $V_{(POR)}$. V_{CC} is output on RBI through an internal FET switch when V_{CC} is above $V_{(POR)}$, charging the capacitor. If V_{CC} drops below $V_{(POR)}$, the FET switch from V_{CC} is opened and the capacitor can supply the small data retention current to the internal registers to retain the data content while V_{CC} is absent. Register data will be maintained as long as the RBI voltage remains above 1.3 V.

FUNCTIONAL DESCRIPTION (continued)

Register Initialization and Data Integrity Checks

Checksums of critical internal register data are continually checked during operation of the bqJUNIOR. A failed checksum comparison will force a hardware reset. After a reset, the bqJUNIOR examines a checksum containing LMD, CYCL, CYCT, and other critical data. If the checksum is incorrect, NAC, CYCL, and CYCT are cleared, LMD and other parameters are initialized from EEPROM, the CI bit in FLAGS is set, and the INIT bit in MODE is set. This process constitutes a full reset. If the checksum is correct, NAC, LMD, CYCL, and CYCT are retained. In addition, a second checksum containing all user-updateable EEPROM coefficients is checked. If the second checksum is incorrect, the values are all initialized from the EEPROM, the CI bit in FLAGS is set, and the INIT bit in MODE is set. The INIT bit is used to inform the host that it may need to reinitialize these values if the default values are not satisfactory. If the second checksum is correct, the INIT bit in MODE will not be set, the CI bit in FLAGS will remain unchanged, and the register data that may have been updated by the host will be retained. This process constitutes a partial reset. It is the host responsibility to clear the INIT bit in MODE after any updates by the host are completed. See CTRL description for more on host updates. Other register values not specifically retained are reinitialized on all resets.

GPIO

The GPIO pin can be used as an input or an output. The initial state can be established by programming bit 7 in the PKCFG EEPROM location. The input/output state can be changed at any time by changing the value in bit 7 of MODE. If unused, the GPIO pin should be tied to V_{SS}.

Layout Considerations

The auto-calibrating DSCC approach effectively cancels the internal offset voltage within the bqJUNIOR, but any external offset caused by PCB layout must be programmed in the EEPROM to be cancelled. The magnitude and variability of the external offset makes it critical to pay special attention to the PCB layout. To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the filter capacitors from SRP and SRN to V_{SS} should be placed as closely as possible to the bqJUNIOR, with short trace runs to both signal and V_{SS} pins. All low-current V_{SS} connections should be kept separate from the high-current discharge path from the battery and should tie into the high-current trace at a point directly next to the sense resistor. This should be a trace connection to the edge or inside of the sense resistor connection, so that no part of the V_{SS} interconnections carry any load current and no portion of the high-current PCB trace is included in the effective sense resistor (i.e. Kelvin connection).

Gas Gauge Operation

Figure 4 illustrates an operational overview of the gas gauge function.

The bqJUNIOR reports uncompensated nominal available capacity (NAC), uncompensated last measured discharge (LMD), compensated available capacity (CAC), and full charge compensated available capacity (FCAC). The compensated CAC and FCAC values are reduced from their respective uncompensated NAC and LMD values by an amount that varies with discharge rate, temperature, and cycle count (age). CAC and FCAC will equal their respective uncompensated NAC and LMD values at light loads and when charging.

The bqJUNIOR learns the capacity of the battery during actual use conditions and will update LMD when a valid learning cycle occurs. The bqJUNIOR learns the capacity of the battery by measuring the capacity removed from the battery when it is discharged from full (NAC = LMD) to the first end-of-discharge (EDV1) voltage threshold

FUNCTIONAL DESCRIPTION (continued)

When the battery is charged to full (NAC = LMD), the valid discharge flag (VDQ) bit in FLAGS will be set. It will remain set during the subsequent discharge until the learning discharge cycle completes or an event occurs that disqualifies the learning cycle. When the battery is discharged to the condition where VOLT ≤ EDV1 threshold, the learning cycle will terminate and LMD will be updated if VDQ is still set. The bqJUNIOR EDV detection is designed to prevent premature detection of the EDV threshold due to dynamic load variations. EDV detection has a dynamically adjusted delay of up to 21.5 seconds with CSOC ≥ 6% and down to 3 seconds when CSOC = 0%. To prevent a severe reduction in LMD due to some abnormal situation, the new LMD value is restricted to a learn-down maximum of DC/8 during any single learning cycle. When the learning cycle completes, LMD is updated and the capacity inaccurate (CI) bit in FLAGS is cleared. The CI bit will remain cleared unless there is a full reset (reset with RAM corruption detected) or the cycle count since the last learning cycle (CYCL) reaches a count of 32.

A learning cycle can be disqualified by any of the following conditions:

1. Cold temperature: Temperature < 0°C when the EDV1 threshold voltage is reached.
2. Light load: A capacity learning cycle is disqualified if average current is less than or equal to 2 times the initial standby load when the EDV1 threshold voltage is reached.
3. Excessive charging: Cumulative Charge > 255 NAC counts (910 µVh) during a learning discharge cycle (alternating discharge/charge/discharge before EDV1 is set).
4. Reset: VDQ is cleared on all resets.
5. Excessive self-discharge: NAC reduction from self-discharge estimate (0.195%) performed 64 times.
6. Self-discharge at termination of learning cycle. If self-discharge estimate causes CAC ≤ DC/16, VDQ is cleared.

NAC is adjusted by charge and discharge coulometric measurements except when battery full or empty conditions are detected. NAC = LMD is forced when IMIN = 1 (full detection) unless Temperature ≤ TCOMP[2:0]*2 (°C). During a discharge with VDQ = 1, CAC is not allowed to drop below DC/16 until EDV1 = 1. If EDV1 = 1 occurs when CAC > DC/16, CAC = DC/16 will be forced. CAC = 0 is forced if EDVF = 1.

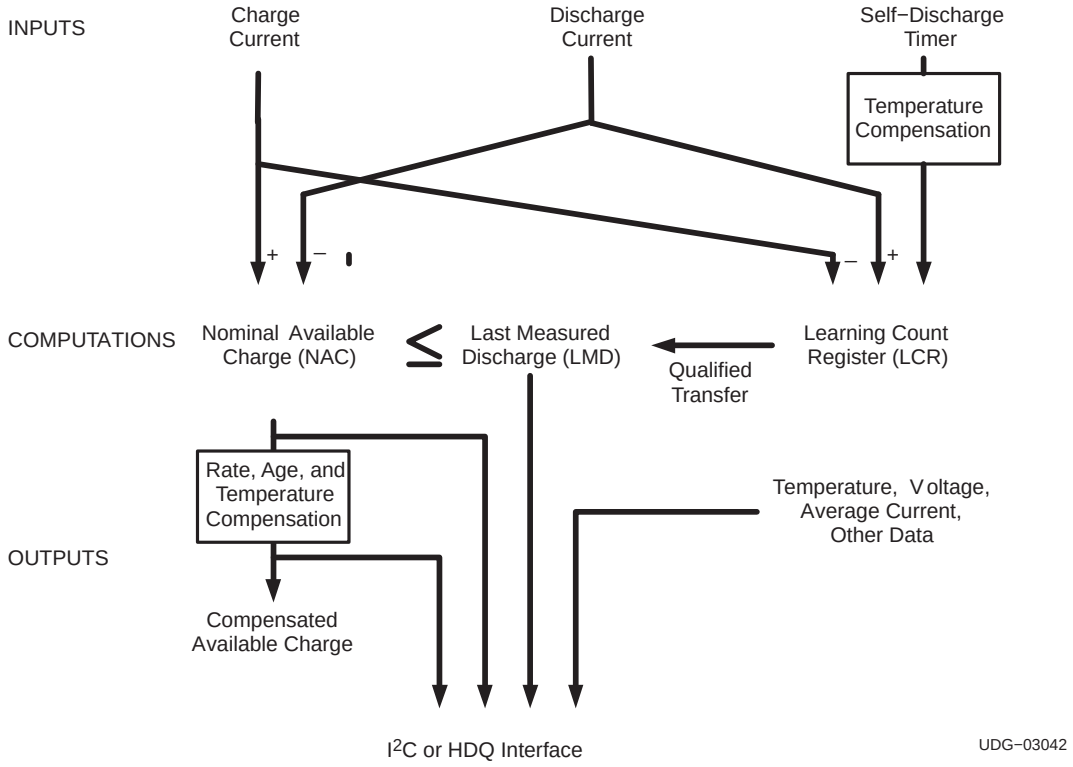
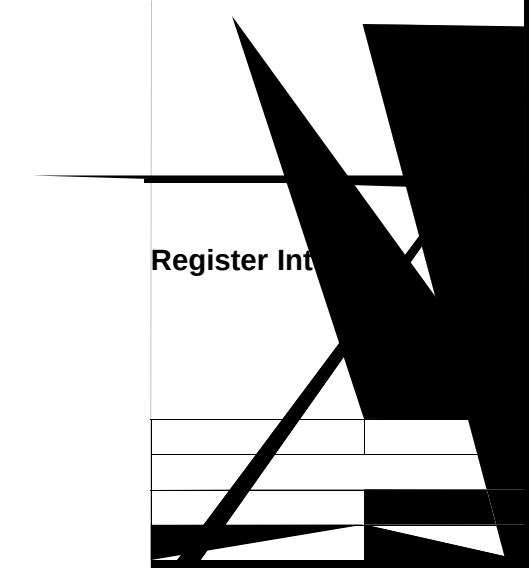


Figure 4. Operational Overview

Register Int



APPLICATION INFORMATION

Control and MODE Registers (CTRL/MODE) — Address 0x00/0x01

The device control register is used by the host system to request special operations by the bqJUNIOR. The highest priority command set in the MODE register is performed when the host writes data 0xA9, 0x56, or 0xC5 as indicated to the control register. The CTRL register and MODE bits 5, 4, 3, 1, and 0 are cleared when the command is accepted. The host must set the appropriate command bit in MODE before sending the command key to CTRL.

Mode Register (MODE) — Address 0x01

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMMAND KEY = 0xA9	GPIEN	GPSTAT	WRTNAC	DONE	PRST	INIT	FRST	SHIP(1)
COMMAND KEY = 0x56	GPIEN	GPSTAT	CEO	CIO	WNACCI	INIT	WRTCYC	WRTLMD
COMMAND KEY = 0xC5	GPIEN	GPSTAT	UPDC	UPEDVI	UPDMF	INIT	UPCFG	UPCOMP

(1) bq27010 only

GPIEN GPIEN sets the state of the GPIO pin. A *1* configures the GPIO pin as input, while a *0* configures the GPIO pin as an open-drain output. This bit is initialized to the value of bit 7 of the PKCFG register in the EEPROM. The user should keep this bit set or cleared as desired when other bits in this register are written.

GPSTAT GPSTAT sets the state of the open drain output of the GPIO pin (GPIEN = 0). A *1* turns off the open drain output, while a *0* turns the output on. This bit is set to *1* on POR. When the GPIO pin is an input (GPIEN=1), this bit returns the logic state of the GPIO pin. The user should keep this bit set or cleared as desired when other bits in this register are written.

WRTNAC WRTNAC is used to transfer data from the AR registers to NAC. Other registers are updated as appropriate. This command is useful during the pack manufacture and test to initialize the gauge to match the estimated battery capacity.

DONE DONE is used to write NAC equal to LMD. Useful if the host uses a charge termination method that does not allow the monitor to detect the taper current. The host system could use this command when the charging is complete to force update of internal registers to a full battery condition.

PRST Partial reset. This command requests a reset of all RAM registers except NAC, LMD, and the CI bit in FLAGS. This command is intended for manufacturing use.

INIT The INIT status bit is set to *1* by the bqJUNIOR if there is a full reset or if data corruption is detected in the internal memory containing EEPROM coefficients. Either of these events will cause the bqJUNIOR to update internal memory values. If NAC, LMD, CYCT, or EEPROM-initialized coefficients need to be modified from their original values, the host should first update the values and then clear the INIT bit. The INIT bit is not cleared by the bqJUNIOR.

FRST Full reset. This command bit requests a full reset. A full reset reinitializes all RAM registers, including the NAC, LMD, and FLAGS registers. This command is intended for manufacturing use.

SHIP This command bit requests that the device (bq27010 only) should be put in ship mode. See the *Power Mode* section for a description of the ship mode. This command is intended for manufacturing use.

CEO This command bit requests that the external offset value is measured. Care should be taken to insure that no charge or discharge current flows during the time this measurement is made. The external offset value is the total offset of the DSCC plus any external PCB affects. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use. The CIO offset value may be subtracted from the CEO offset value to determine the external board offset. This value can be programmed into PKCFG[4:2] in the EEPROM for automatic compensation of this external offset value.

CIO This command bit requests that the internal offset value is measured. The internal offset value is

the offset of the DSCC with an internal short applied from SRP to SRN. The result

At-Rate Registers (ARL/ARH) — Address 0x02/0x03

At Rate Time-to-Empty Registers (ARTTEL/ARTTEH) — Address 0x04/0x05

Reported Temperature Registers (TEMPL/TEMPH) — Address 0x06/0x07

Reported Battery Voltage Registers (VOLTL/VOLTH) — Address 0x08/0x09

The VOLTH and the VOLTL low-byte registers contain the reported battery voltage measured on the BAT pin. Voltage is expressed in mV with an LSB resolution of 1 mV. Reported voltage cannot exceed 5000 mV. The host system has read-only access to this register pair. Voltage is updated every 2.56 seconds.

Status Flag Register (FLAGS) — Address 0x0A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	CHGS	NOACT	IMIN	CI	CALIP	VDQ	EDV1	EDVF
POR STATUS	0	0	0	1	0	0	0	0

CHGS Charge State flag. A *1* in the CHGS indicates a charge current (V_{SRP}

Relative State-of-Charge (RSOC) — Address 0x0B

Nominal Available Capacity Registers (NACL/NACH) — Address 0x0C/0x0D

This register pair reports the light-load, or uncompensated, capacity available from the battery. NAC increments during charge (V_{SRP} > $V_{SRNf\ (or)Tj\ 1\ 0\ 06\ 114.4\ Tm\ 1\ 0\ 0\ 1\ 134\ (SR4/F2\ 1\ 0\ 0\ 1\ 65.3\ 54\ Tm\ s.\ 0\ 1\ 56.6\ 285.2\ Tm\ /(increments)Tj\ 1\ 0\ 071\ 114.4\ Tm\ 1\ 0\ 0\ 1\ 56.6\ 114.4r}$

Last Measured Discharge Registers (LMDL/LMDH) – Address 0x0E/0x0F

Compensated Available Capacity (CACL/CACH) – Address 0x10/0x11

Fully-Charged Compensated Available Capacity (FCACL/FCACH) – Address 0x12/0x13

Average Current Registers (AIL/AIH) — Address 0x14/0x15

Time-to-Empty Registers (TTEL/TTEH) — Address 0x16/0x17

Time-to-Full Registers (TTFL/TTFH) — Address 0x18/0x19

Standby Current Registers (SIL/SIH) — Address 0x1A/0x1B

Standby Time-to-Empty Registers (STTEL/STTEH) — Address 0x1C/0x1D

Compensated End-of-Discharge Registers (CEDVL/CEDVH) – Address 0x20/0x21

Time-to-Empty at Constant Power Registers (TTECPL/TTECPH) – Address 0x26/0x27

Cycle

Compensated State-of-Charge (CSOC) — Address 0x2C

CSOC reports the compensated available capacity as a percentage of the last measured discharge value (LMD). The equation is:

CSOC (%) = 100 * CAC / LMD

The host system has read-only access to this register.

Reserved Registers

Addresses 0x1E, 0x1F, 0x22-0x25, 0x2D-0x6D and 0x6F-0x75 are reserved and cannot be written by the host.

EEPROM Enable Register (EE_EN) — Address 0x6E

This register is used to enable host writes to EEPROM data locations (addresses 0x76 — 0x7F). The host must write data 0xDD to this register to enable EEPROM programming. See the *Programming the EEPROM* section for further information on programming the EEPROM bytes. Care should be taken to insure that no value except 0xDD is written to this location. All bqJUNIOR measurements and computations will be inhibited until 0x00 is written back to address 0x6E.

EEPROM Data Registers (EE_DATA) — Address 0x76 — 0x7F

The EEPROM data registers contain information vital to the performance of the device. These registers are to be programmed during pack manufacturing to allow flexibility in the design values of the battery to be monitored. The EEPROM data registers are listed in Table 2. Detailed descriptions of what should be programmed follow. See the *Programming the EEPROM* section for detailed information on writing the values to EEPROM.

Table 2. bq27010/bq27210 EEPROM Memory Map

Address	Name	Function
0x7F	TCOMP	Temperature compensation constants, OR, ID#1
0x7E	DCOMP	Discharge rate compensation constants, OR, ID#2
0x7D	GAF/DEDV	Gain Age Factor / EDVI rate compensation
0x7C	PKCFG	Pack configuration values
0x7B	TAPER	Aging estimate enable [7], charge termination taper current [6:0]
0x7A	DMFSD	Digital magnitude filter and self-discharge rate constants
0x79	ISLC/EDVT	Initial standby load current / EDVI temperature compensation
0x78	SEDV1	Scaled EDV1 threshold
0x77	SEDVF	Scaled EDVF threshold
0x76	ILMD	Initial last measured discharge high byte

Initial Last Measured Discharge High Byte (ILMD) — Address 0x76

This register contains the scaled design capacity of the battery to be monitored. ILMD is programmed in

Scaled EDVF Threshold (SEDVF) — Address 0x77

Scaled EDV1 Threshold (SEDV1) — Address 0x78

This register contains the scaled value of the voltage when the battery has 6.25% remaining capacity at a very light load. DEDV and EDVT coefficients can be programmed to reduce the EDVI threshold at heavier loads and at cold temperatures. When the battery reaches this threshold during a valid discharge, the device learns the full battery capacity, including the remaining unmeasured 6.25%. See the *bqJUNIOR Capacity Learning* section for more information on the learning cycles of the device. To calculate the value to program, use the following equation:

SEDV1 = Design EDV1 (mV) / 8 – 256

Initial Standby Load Current and EDV1 Temperature Compensation (ISLC/EDVT) – Address 0x79

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
Name	0	ISLC[2]	ISLC[1]	ISLC[0]	EDVT[3]	EDVT[2]	EDVT[1]	EDVT[0]

The most significant nibble in this register contains the initial standby load current (ISLC) that is transferred to SI on all resets. The gauge will use this initial value, but will learn the actual system standby current by averaging in measured discharge currents above the DMF threshold and less than or equal to 2 times the ISLC value. ISLC is programmed in units of 57.1 μV per bit.

A capacity learning cycle is disqualified if average current is less than or equal to 2 times the ISLC programmed value.

The equation for programming ISLC is:

ISLC = Design Standby Current (mA) * R_S (mΩ) / 57.1 μV, where R_S is the sense resistor value.

The least significant nibble in this register contains the EDV1 temperature compensation (EDVT) coefficient. The temperature compensation is impedance-based, so the resulting compensation is proportional to load current. EDVT is programmed to increase the EDV1 rate compensation (programmed in the DEDV coefficient) by 0.78% per count for each degree than temperature is below the T_{off} threshold programmed in TCOMP. See the GAF/DEDV section for the complete EDV1 compensation equation.

Digital Magnitude Filter and Self-Discharge Values (DMFSD) — Address 0x7A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	DMF[3]	DMF[2]	DMF[1]	DMF[0]	SD[3]	SD[2]	SD[1]	SD[0]

DMF[3:0] Sets the digital magnitude filter threshold. See the *bqJUNIOR Digital Magnitude Filter* section for more information on the function of the DMF. The value to be programmed is: DMF[3:0] = Design Threshold / 4.9

si2)the

SD[3:0] Sets the self-discharge rate % per day value at 25°C. The value to be programmed is: SD[3:0] = 1.61 / Design SD

NAC is reduced with an estimated self-discharge correction to adjust for the expected self-discharge of the battery. This estimation is performed only when the battery is not being charged. The rate programmed in EEPROM for DMFSD determines the self-discharge when 20°C ≤ TEMP < 30°C. The self-discharge estimation is doubled for each 10°C decade hotter than the 20-30°C decade, up to a maximum of 16 times the programmed rate for TEMP ≥ 60°C and is halved for each 10°C decade colder than the 20-30°C decade, down to a minimum of 1/4th the programmed rate for TEMP < 0°C. The self-discharge estimation is performed by reducing NAC by NAC / 512 at a time interval that achieves the desired estimation. If DMFSD is programmed with 8 decimal, the self-discharge rate is 0.195% per day in the 20-30°C decade. This is accomplished by reducing NAC by NAC / 512 (100 / 512 = 0.195%) a single time every 23.3 23 0 0 1 405.099 637 (Digital)Tj 1 0 0 1 /F2 Tı

and

Taper Current (TAPER) — Address 0x7B

This register contains the enable bit for the capacity aging estimate and the charge taper current value. The taper current value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming the taper current is:

TAPER[6-0] = Design Taper Current (mA) * R_S(mΩ) / 228 µV

where R_S is

Pack Configuration (PKCFG) — Address 0x7C

			rent					

DCFIX Fixed discharge compensation. Normal discharge rate compensation (DCOMP register) is used if this bit is set to 0. If this bit is set to 1, the device assumes a fixed value of 0x6C for DCOMP, giving a discharge rate compensation gain (DCGN) of 5.08% with a compensation offset threshold of C/2. Setting the bit to *1* frees the EEPROM location of 0x7E for use as a programmable identification byte.

TCFIX Fixed temperature compensation. Normal temperature compensation (TCOMP register) is used if this bit is set to 0. If this bit is set to 1, the device assumes a fixed value of 0x46 for TCOMP, which will increase DCGN by 25% per °C below 12°C. Setting this bit to *1* frees the EEPROM location of 0x7F for use as a programmable identification byte.

Gain Age Factor and EDV1 Discharge Rate Compensation (GAF/DEDV) – Address 0x7D

	BIT 7	BIT 6	BIT 5	BIT				

Discharge Rate Compensation Coefficients (DCOMP) – Address 0x7E

Discharge Rate Compensation Threshold

DCOFF[2:0]	DCOFF Threshold (1)
0	0
1	(DCGN / 256) * 1C / 8
2	(DCGN / 256) * 2C / 8
3	(DCGN / 256) * 3C / 8
4	(DCGN / 256) * 4C / 8
5	(DCGN / 256) * 5C / 8
6	(DCGN / 256) * 6C / 8
7	(DCGN / 256) * 7C / 8

(1) C = ILMD * 256

The discharge compensation capacity reduction (DCMP) is a function of discharge rate, temperature, and age (cycle count). There is no compensation if the DCGN factor increased for age and temperature times AI is less than the DCOFF threshold (DCMP ≥ 0). The following is the combined equationfollowing

Temperature Compensation Coefficients (TCOMP) – Address 0x7F

Power Modes

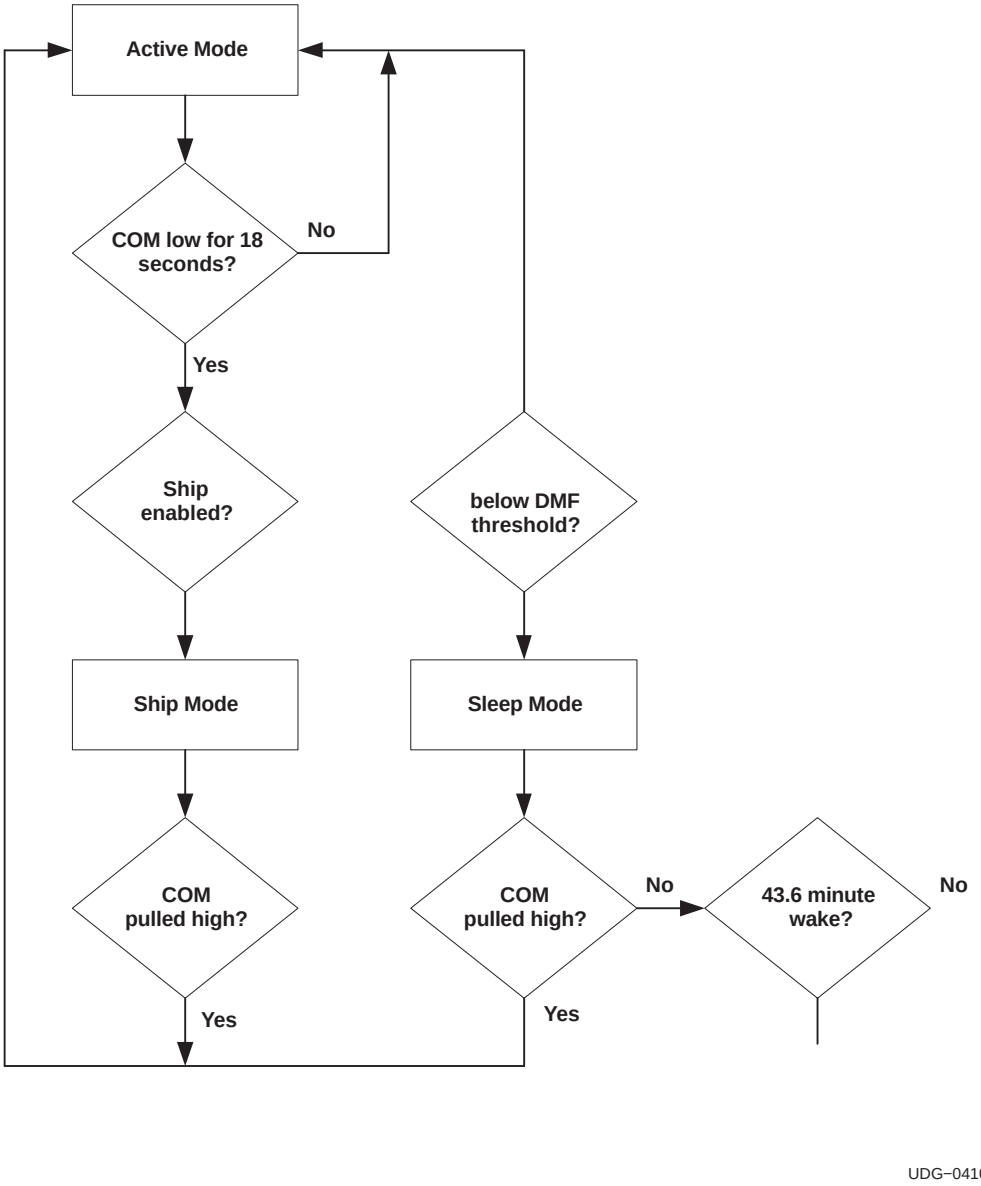


Figure 5. Power Mode Flow Chart

Active Mode

During normal operation, the device is in active mode, which corresponds to the highest power consumption. Normal gas gauging is performed in this mode. If system requirements mandate that bqJUNIOR should not enter Sleep or Ship modes, then an external pullup resistor from V_{CC} to keep HDQ or CLK and DTA at a logic *1* is required on the bqJUNIOR side of the system. The resistor value chosen should be small enough to force a logic *1* even with the internal pulldown current and any external ESD protection circuitry loading.

Sleep Mode

This low power mode is entered when the HDQ or CLK and/or DTA line is

Ship Mode (bq27010 only)

Hibernate Mode

Programming the EEPROM

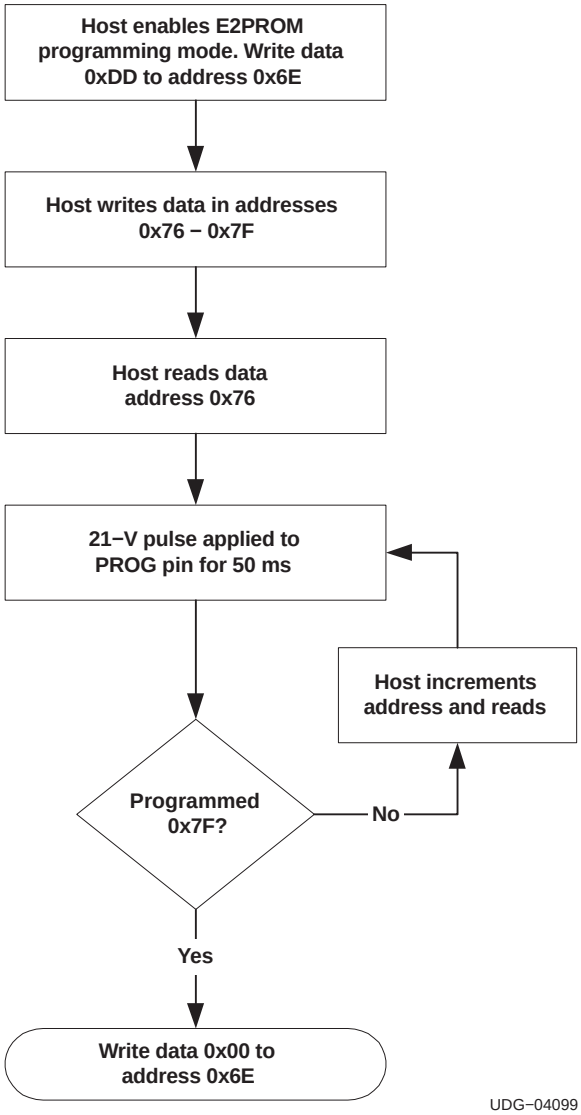


Figure 6. EEPROM Programming Flow

It is not required that addresses 0x76 — 0x7F be programmed at the same time or in any particular order. The programming method illustrated in Figure 6 can be used to program any of the bytes as long as the sequence of Enable, Write, Read, Apply Programming Pulse, and Disable is followed.

The bqJUNIOR must have a full reset to force the updated EEPROM values into RAM. A full reset will occur after a POR if RAM data is corrupted (failed checksum), or a full-reset command may be sent using the CTRL and MODE registers.

Communicating With the bq27010 (HDQ interface)

The bq27010 includes a single-wire HDQ serial data interface. Host processors, configured for either polled or interrupt processing, can use the interface to access various bq27010 registers. The HDQ pin is an open-drain device, which requires an external pullup resistor. The interface uses a command-based protocol, where the host processor sends a command byte to the bq27010. The command directs the bq27010 either to store the next eight bits of data received to a register specified by the command byte or to output the eight bits of data from a register specified by the command byte.

Command byte

Communicating with the bq27210 (I²C interface - Product Preview)

The bq27210 supports the standard I²C read, incremental read, quick read, and one byte write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively. (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop)

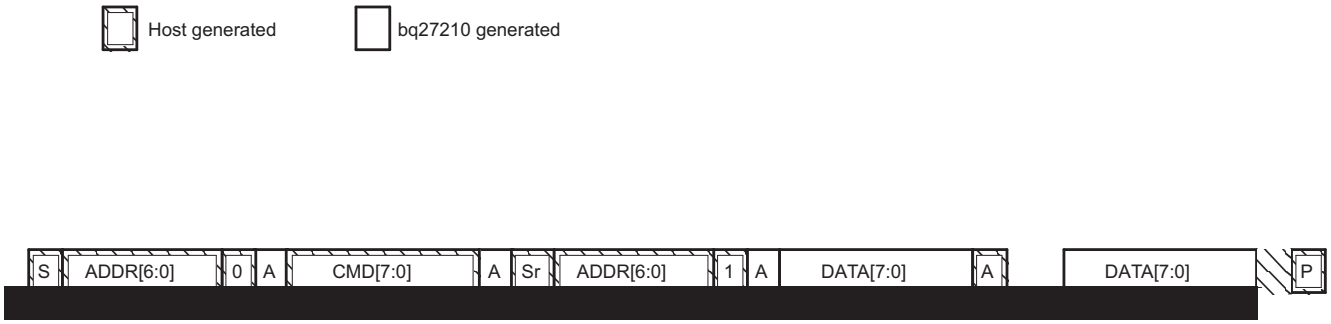
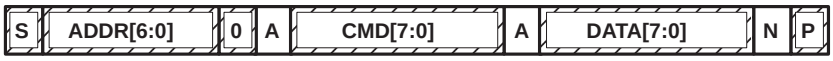


Figure 7. Supported I2C formats :
(a) 1-byte write; (b) quick read; (c) 1-byte read; (d) incremental read

The incremental read protocol is recommended for reading all 16-bit values, as this ensures that the 16-bit value is not updated during the time interval between reading the two bytes of data (see previous section on reading 16-bit values). The quick read returns data at the address indicated by the internal address pointer. The address pointer is incremented after each data byte is read or written. Reading an even address causes the communication engine to simultaneously capture the data byte from the requested even address and the data byte from the next odd address, and the address pointer is incremented twice. The data byte captured from the next odd address is output if the communication continues, without a stop, after the host acknowledges the even address byte.

Due to the memory map setup of the device, several boundary conditions must be enforced by the communication engine.

Attempt to write a read-only address (NACK after data sent by master):



Attempt to read an address above 0x7F (NACK command):

Attempt at incremental writes (NACK all extra data bytes sent):

Incremental read at the maximum allowed read address:

The I²C engine releases both SDA and SCL if the I²C bus is held low for $T_{(BUSERR)}$. If the bq27210 is holding the lines, releasing them frees the master to drive the lines. If an external condition is holding either of the lines low, the I²C engine enters the low-power sleep mode if the measured charge/discharge activity level is less than the DMF threshold.

PACKAGING INFORMATION

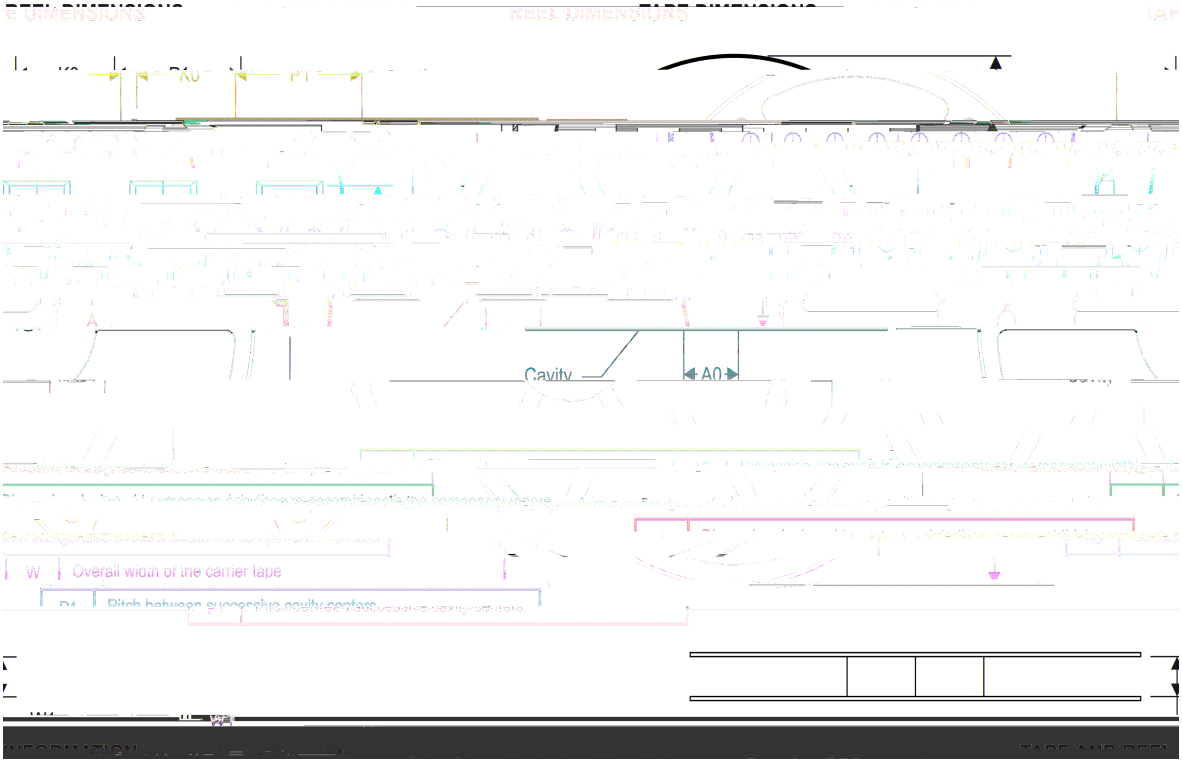
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
BQ27010DRKR	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ27010DRKRG4	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ27210DRKR	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples
BQ27210DRKRG4	ACTIVE	VSON	DRK	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	Request Free Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

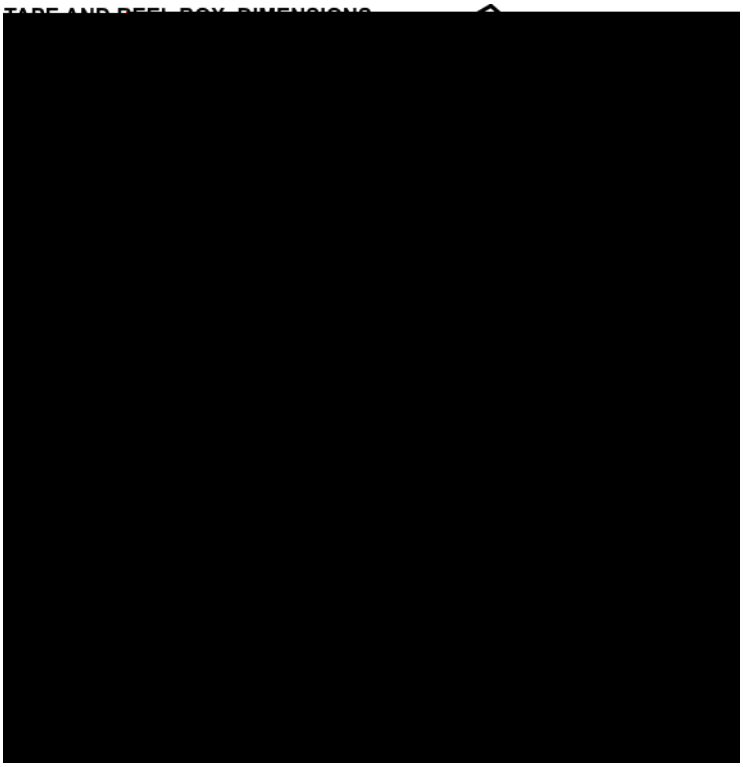
TAPE AND REEL INFORMATION



*All dimensions are nominal

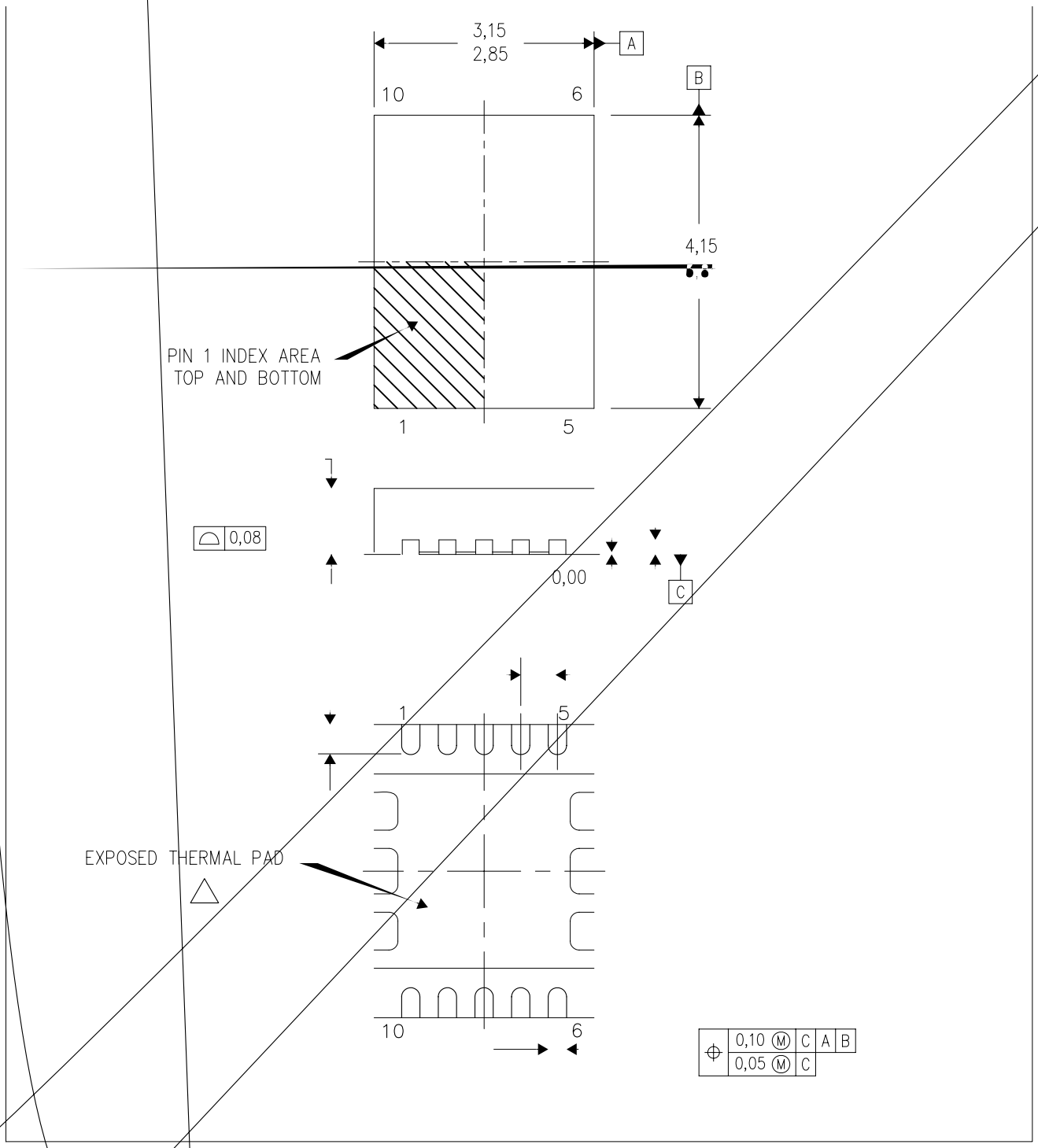
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27010DRKR	VSON											

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27010DRKR	VSON	DRK	10	3000	338.1	338.1	20.6
BQ27210DRKR	VSON	DRK	10	3000	338.1	338.1	20.6



B. This dr[illegible] cing pe
C. Small Outline No–Lead (SON) package configuration.
[illegible]ckage thermal pad must be soldered to the board for thermal and mechanical performance.
See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

DRK PLASTIC SMALL OUTLINE NO–LEAD

THERMAL INFORMATION

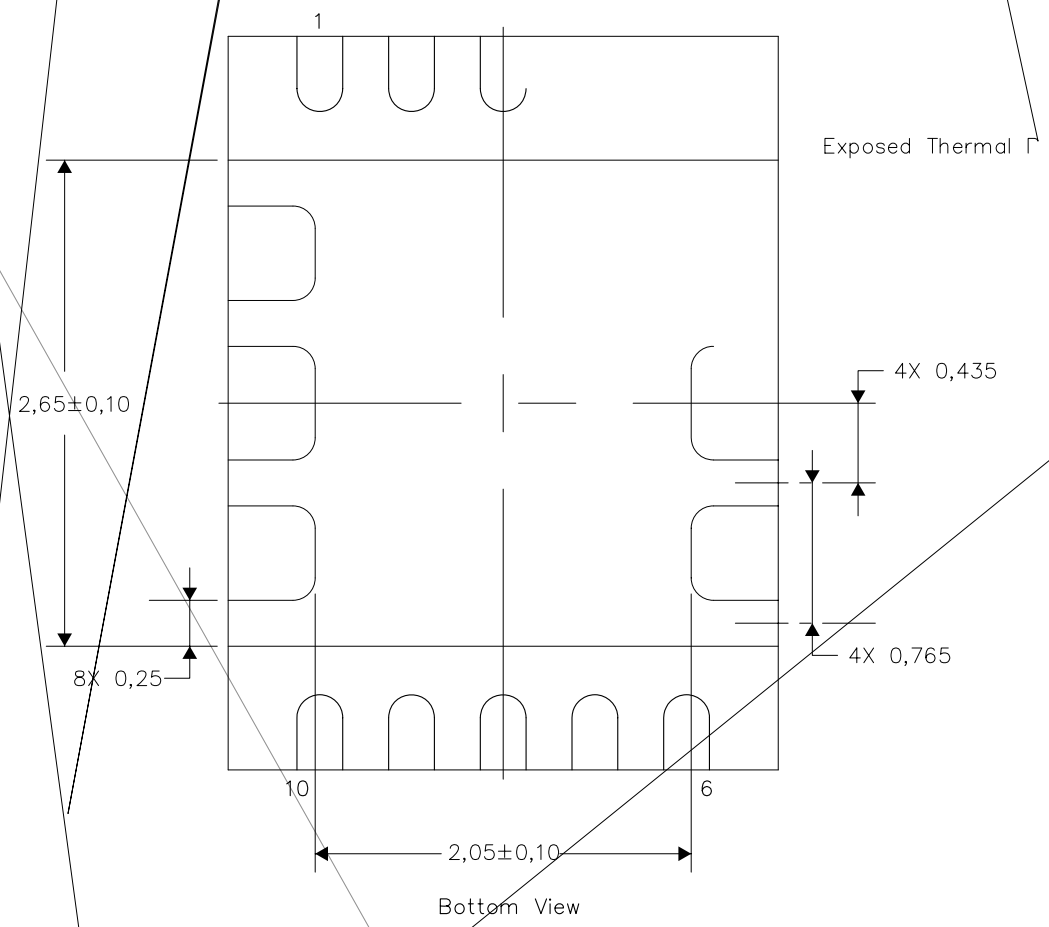
This package inco
heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached

ansfer from the

integrated circuit (IC).

QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

ons for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206317/F 08/10

NOTE: A. All linear dimensions are in millimeters

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