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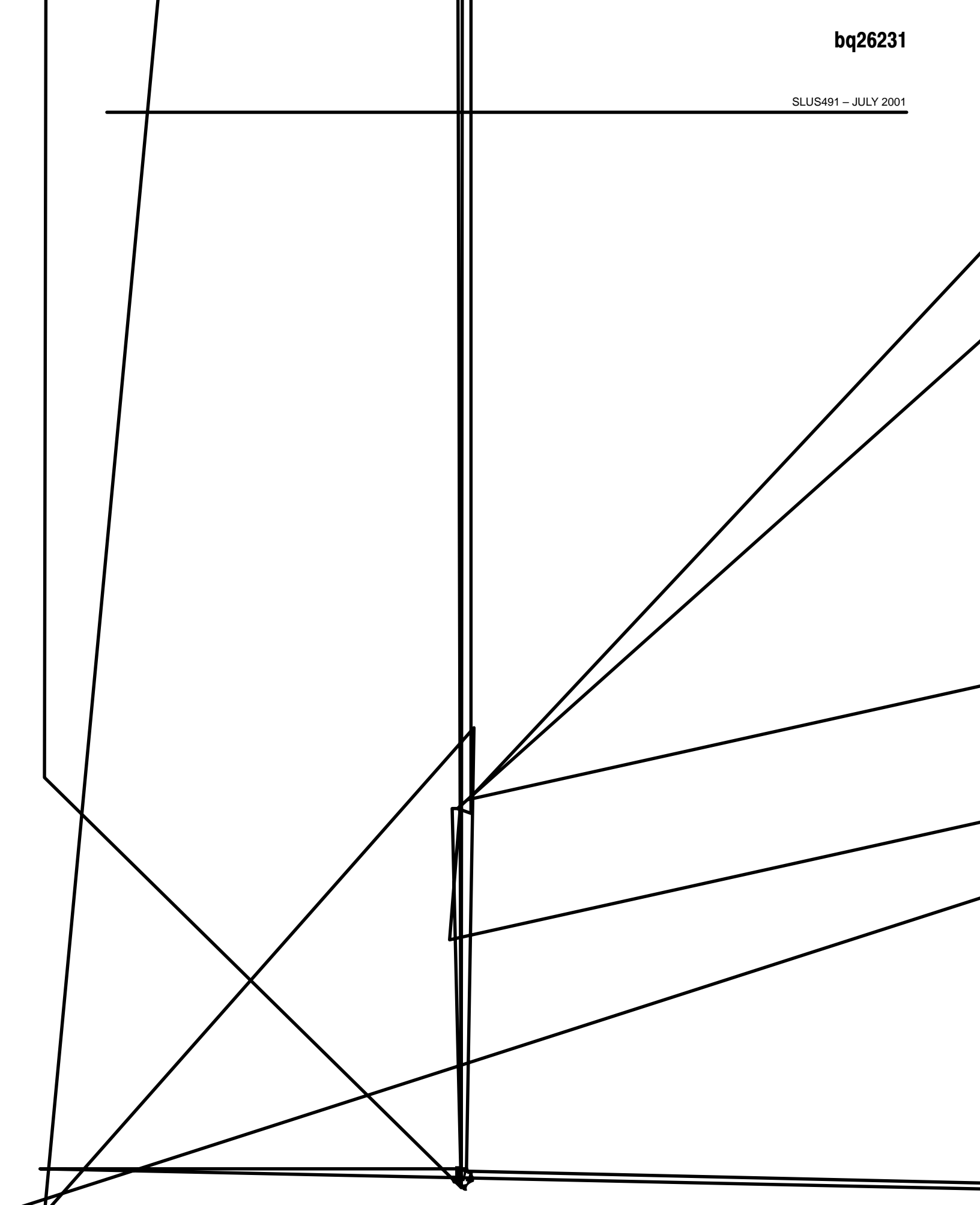
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bq26231

APPLICATION INFORMATION

charge and discharge count operation (continued)

Figure 3 shows the bq26231 register address map. The bq26231 uses the upper 13 locations. The remaining memory can store user-specific information such as chemistry, serial number, and manufacturing date.
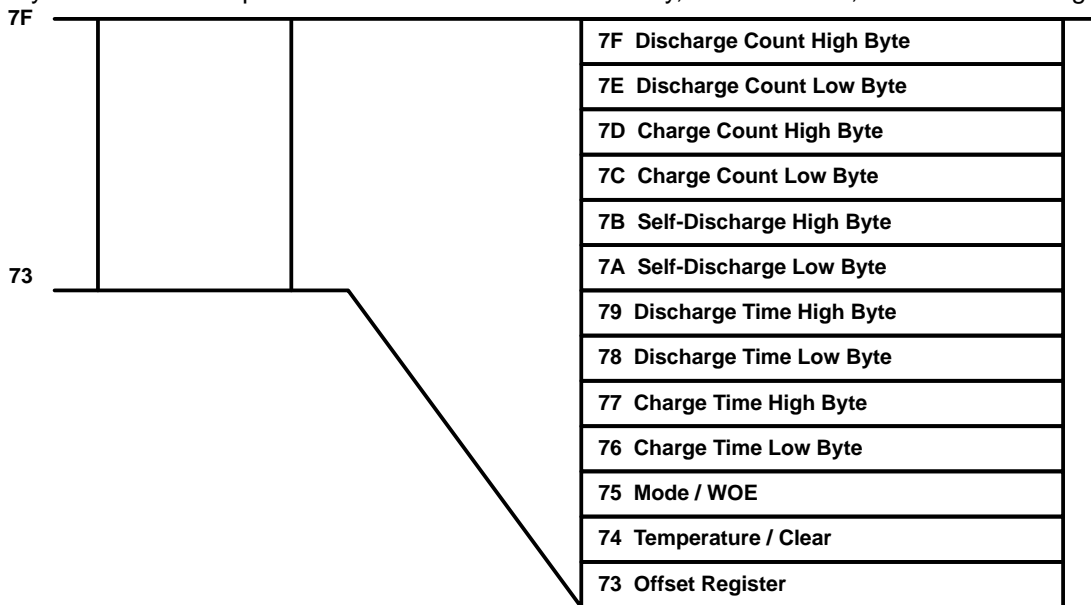
7F	Discharge Count High Byte
7E	Discharge Count Low Byte
7D	Charge Count High Byte
7C	Charge Count Low Byte
7B	Self-Discharge High Byte
7A	Self-Discharge Low Byte
79	Discharge Time High Byte
78	Discharge Time Low Byte
77	Charge Time High Byte
76	Charge Time Low Byte
75	Mode / WOE
74	Temperature / Clear
73	Offset Register

Figure 3. bq26231 Register Map

temperature

The bq26231 has an internal temperature sensor to set the value in the temperature register (TMP/CLR) and to set the self-discharge count rate value. The register reports the temperature in 8 steps of 10°C from < 0°C to > 60°C as Table 3 specifies. The bq26231 temperature sensor has typical accuracy of ±2°C at 25°C. See the TMP/CLR register description for more details.

Table 3. Temperature Steps

TEMPERATURE	VALUE (hex)	SDR COUNT RATE
< 0°C	0h	× 1/8
0–10°C	1h	× 1/4
10–20°C	2h	× 1/2
20–30°C	3h	1 count/hr
30–40°C	4h	× 2
40–50°C	5h	×c4
50–60°C	6h	× 8
>60°C	7h	× 16

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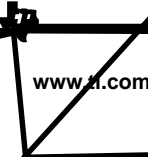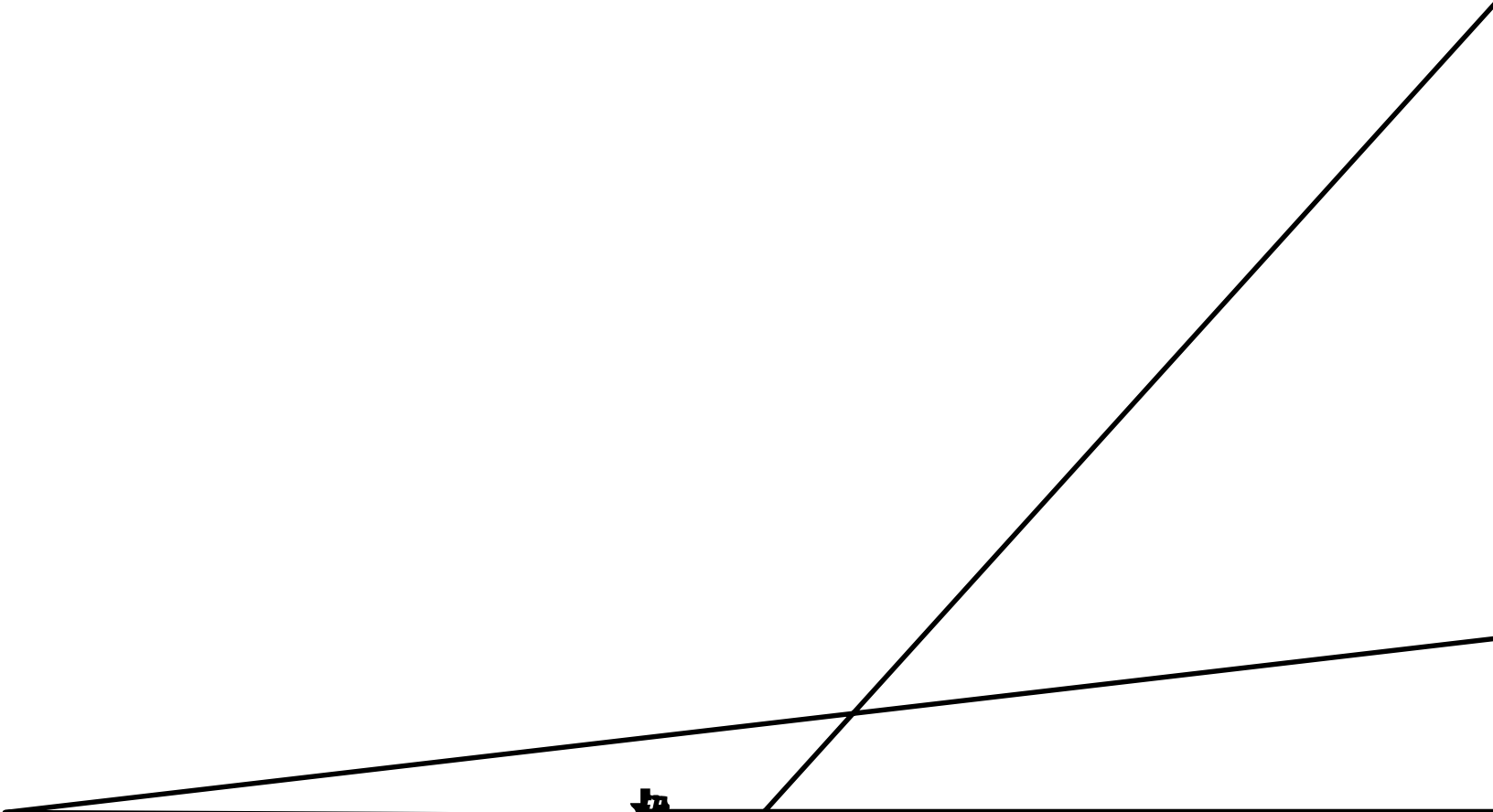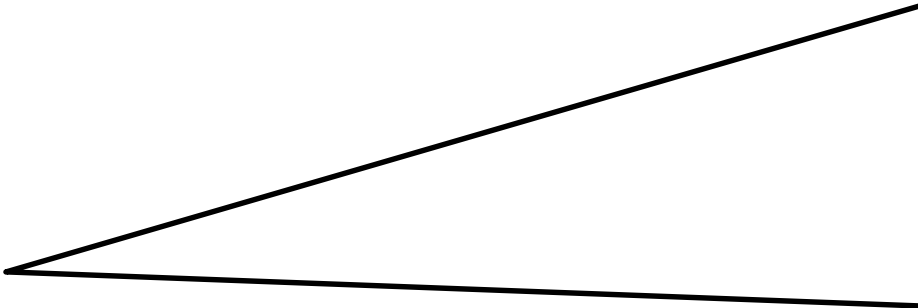
APPLICATION INFORMATION

temperature and clear register (continued)

The clear bit locations are

TMP/CLR BITS							
7	6	5	4	3	2	1	0
–	–	–	CTC	DTC	SCR	CCR	DCR

Where:

The CTC bit (bit 4) resets both the CTCH and CTCL registers and the STC bit to 0.

The DTC bit (bit 3) resets both the DTCH and DTCL registers and the STD bit to 0.

The SCR bit (bit 2) resets both the SCRH and SCRL registers to 0.

The CCR bit (bit 1) resets both the CCRH and CCRL registers to 0.

The DCR bit (bit 0) resets both the DCRH and DCRL registers to 0.

offset register (OFR)

The OFR register (address = 73 hex) is used to store the calculated $V_{(OS)}$ of the bq26231. The OFR value can be used to cancel the voltage offset between $V_{(SR1)}$ and $V_{(SR2)}$. The up/down offset counter is centered at zero. The actual offset is an 8-bit 2s complement value located in OFR.

The OFR locations are

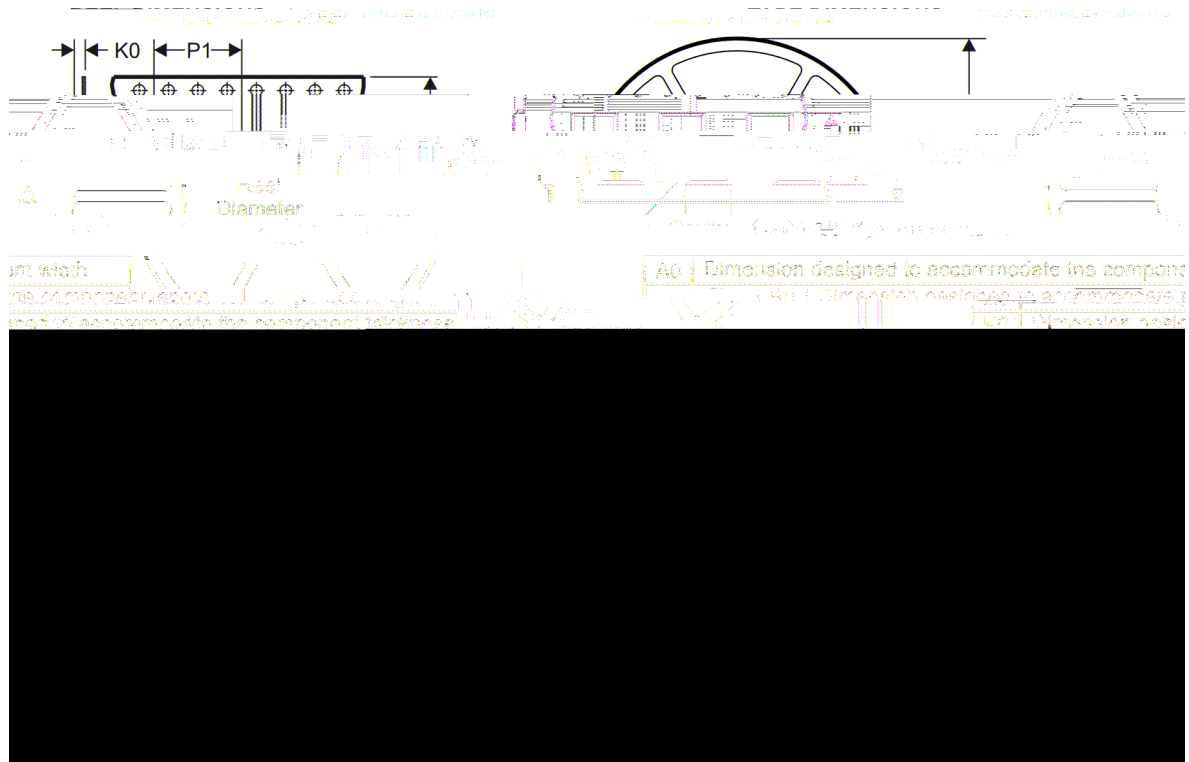| TMP/CLR BITS							
7	6	5	4	3	2	1	0
OFR7	OFR6	OFR5	OFR4	OFR3	OFR2	OFR1	OFR0

where OFR7 is

0   Discharge

1   Charge

bq26231

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PACKAGING INFORMATION

| Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]

PACKAGE MATERIALS INFORMATION

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ26231PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS
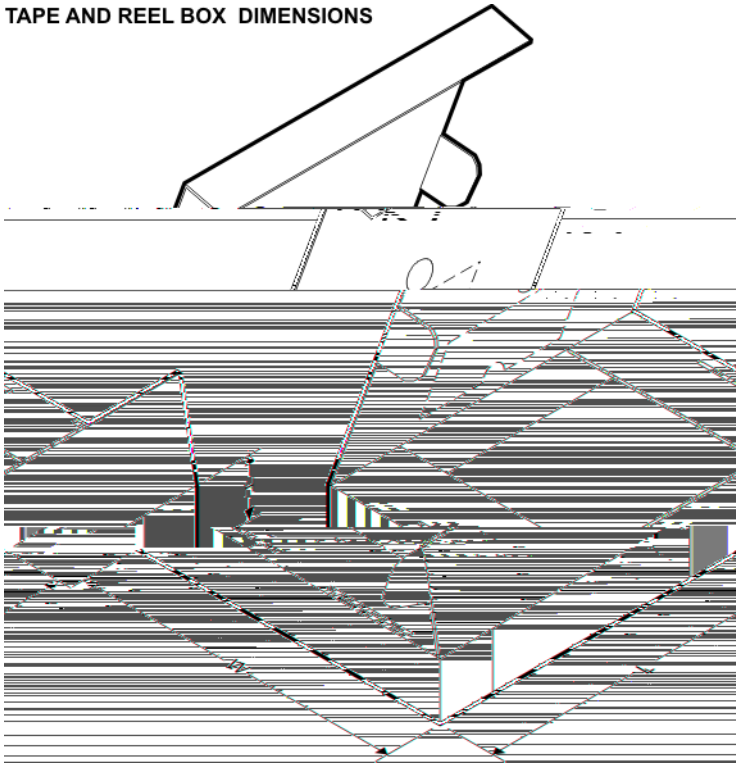
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ26231PWR	TSSOP	PW	8	2000	346.0	346.0	29.0

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