Benchmarq Product
om Te ments

bq2 /F

cd/NiMH Fast-Charge Man nt ICs

Fea

- el cadmium dride batter-
- tput displays
- mination by -ΔV, tage, maximum and maximum
- -gap voltag
- ectable pulse rge rates
- Low-power mode
- 8-pin 300-mil DIP or 150-mil SOIC

General Description

The bq2002 and bq2002/F Fast ICs are low-cost CMOS batt controllers providing termination for both battery applicat a current-limit rrent supply all be the basis f nd-alone or sy harger. The s fast charge with nd pulsed-trickle con- gle IC for charging one or d or NiMH battery cells.

ast charge is initiated on application of the charging supply or battery replacement. For safety, fast charge is inhibited if the battery temperature and voltage are outside configured limits.

is terminated by any of ing:

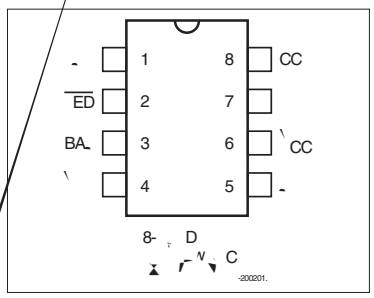
eak voltage detection (PVD)

- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

After fast charge, the bq2002/F optionally tops-off and pulse-trickles the battery per the pre-configured limits. Fast charge may be inhibited using the INH pin. The bq2002/F may also be placed in low-standby-power mode to reduce system power consumption.

The bq2002F differs from the bq2002 only in that a slightly different set of fast-charge and top-off time limits is available. All differences between the two ICs are illustrated in Table 1.

Pin Connections



Pin Names

TM	Timer mode select input	TS	Temperature sense input
$\overline{LED}$	Charging status output	V_{CC}	Supply voltage input
BAT	Battery voltage input	INH	Charge inhibit input
V_{SS}	System ground	CC	Charge control output

bq2002/F Selection Guide

Part No.	TCO	HTF	LTF	-ΔV	PVD	Fast Charge	t_{MTO}	Top-Off	Maintenance
bq2002	0.5 * V_{CC}	None	None		✔	C/2	160	C/32	C/64
					✔	1C	80	C/16	C/64
				✔		2C	40	None	C/32
bq2002F	0.5 * V_{CC}	None	None		✔	C/2	160	C/32	C/64
					✔	1C	100	C/16	C/64
				✔		2C	55	None	C/32

Pin Descriptions

TM **T e . de**

A three-level input that controls the settings for the fast charge safety timer, voltage termination mode, top-off, pulse-trickle, and voltage hold-off time.

$\overline{\text{LED}}$ **C . a . a**

Open-drain output that indicates the charging status.

BAT **Ba e . a e**

The battery voltage sense input. The input to this pin is created by a high-impedance resistor divider network connected between the positive and negative terminals of the battery.

V_{SS} **S e . d**

TS **Te e . a . e e e**

Input for an external battery temperature monitoring thermistor.

V_{CC} **S a e**

5.0V ±20% power input.

INH **C . a . e . b**

When high, INH suspends the fast charge in progress. When returned low, the IC resumes operation at the point where initially suspended.

CC **C . a . e c .**

An open-drain output used to control the charging current to the battery. CC switching to high impedance (Z) enables charging current to flow, and low to inhibit charging current. CC is modulated to provide top-off, if enabled, and pulse trickle.

Functional Description

Figure 2 shows a state diagram and Figure 3 shows a block diagram of the bq2002/F.

Battery Voltage and Temperature Measurements

Battery voltage and temperature are monitored for maximum allowable values. The voltage presented on the battery sense input, BAT, should represent a single-cell potential for the battery under charge. A resistor-divider ratio of

$$\frac{RB1}{RB2} = N - 1$$

is recommended to maintain the battery voltage within the valid range, where N is the number of cells, RB1 is the resistor connected to the positive battery terminal, and RB2 is the resistor connected to the negative battery terminal. See Figure 1.

N e: This resistor-divider network input impedance to end-to-end should be at least 200kΩ and less than 1 MΩ.

A ground-referenced negative temperature coefficient thermistor placed near the battery may be used as a low-cost temperature-to-voltage transducer. The temperature sense voltage input at TS is developed using a resistor-thermistor network between V_{CC} and V_{SS}. See Figure 1.

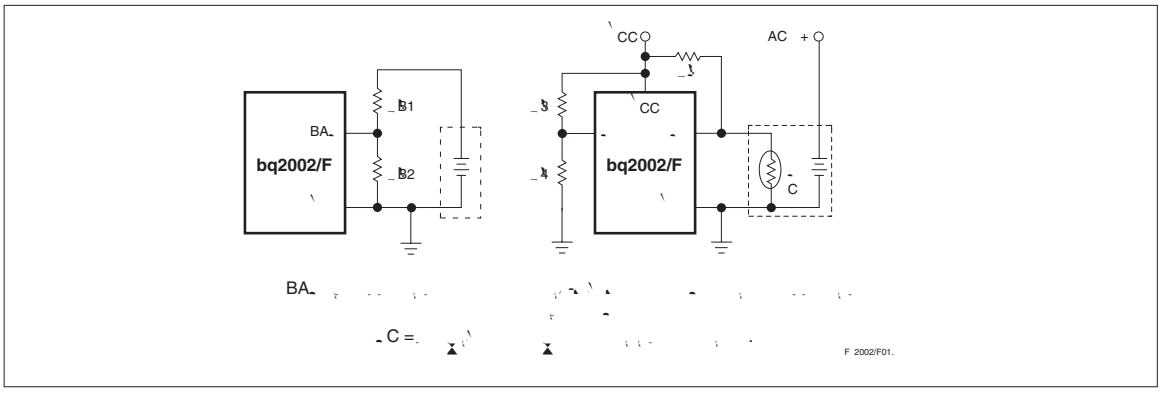
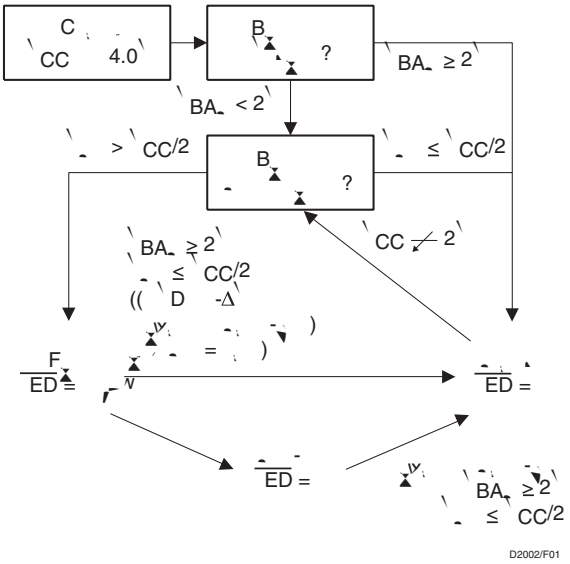


Figure 1. Voltage and Temperature Monitoring and TM Pin Configuration


C
CC 4.0
B
?
BA ≥ 2
BA < 2
> CC/2
B
?
≤ CC/2
CC 2
BA ≥ 2
≤ CC/2
D -Δ
F
ED =
ED =
ED =
BA ≥ 2
≤ CC/2
D2002/F01

Starting A Charge Cycle

Either of two events starts a charge cycle (see Figure 4):

1. Application of power to V_{CC} or

2. Voltage at the BAT pin falling through the maximum cell voltage V_{MCV} where

$$V_{MCV} = 2V \pm 5\%.$$

If the battery is within the configured temperature and voltage limits, the IC begins fast charge. The valid battery voltage range is $V_{BAT} < V_{MCV}$. The valid temperature range is $V_{TS} > V_{TCO}$ where

$$V_{TCO} = 0.5 * V_{CC} \pm 5\%.$$

If the battery voltage or temperature is outside of these limits, the IC pulse-trickle charges until the next new charge cycle begins.

Fast charge continues until termination by one or more of the five possible termination conditions:

- Peak voltage detection (PVD)
- Negative delta voltage (-ΔV)
- Maximum voltage
- Maximum temperature
- Maximum time

Corresponding Fast-Charge Rate	TM	Termination	Typical Fast-Charge and Top-Off Time Limits (minutes)		Typical PVD and -ΔV Hold-Off Time (seconds)	Top-Off Rate	Pulse-Trickle Rate	Pulse-Trickle Period (ms)
			bq2002	bq2002F				
C/2	Mid	PVD	160	160	600	C/32	C/64	9.15
1C	Low	PVD	80	100	300	C/16	C/64	18.3
2C	High	-ΔV	40	40	150	Disabled	C/32	18.3

N e : Typical conditions = 25°C, [illegible] Fast Charge [illegible]3.16.849f5-2924m52366 2

PVD and -ΔV Termination

There are two modes for voltage termination depending on the state of TM. For -ΔV (TM = high), if V_{BAT} is lower than any previously measured value by 12mV ±3mV, fast charge is terminated. For PVD (TM = low or mid), a decrease of 2.5mV ±2.5mV terminates fast charge. The PVD and -ΔV tests are valid in the range $1V < V_{BAT} < 2V$.

Voltage Sampling

Voltage is sampled at the BAT pin for PVD and -ΔV termination once every 17s. The sample is an average of voltage measurements taken 570µs apart.The IC takes 32 measurements in PVD mode and 16 measurements in -ΔV mode. The resulting sample periods (9.17 and 18.18ms, respectively) filter out harmonics centered around 55 and 109Hz. This technique minimizes the effect of any AC line ripple that may feed through the power supply from either 50 or 60Hz AC sources. Tolerance on all timing is ±20%.

Voltage Termination Hold-off

A hold-off period occurs at the start of fast charging. During the hold-off time, the PVD and -ΔV terminations are disabled. This avoids premature termination on the voltage spikes sometimes produced by older batteries when fast-charge current is first applied. Maximum voltage and temperature terminations are not affected by the hold-off period.

Maximum Voltage, Temperature, and Time

Any time the voltage on the BAT pin exceeds the maximum cell voltage,V_{MCV}, fast charge or optional top-off charge is terminated.

Maximum temperature termination occurs anytime the voltage on the TS pin falls below the temperature cut-off threshold V_{TCO}.

Maximum charge time is configured using the TM pin. Time settings are available for corresponding charge rates of C/2, 1C, and 2C. Maximum time-out termination is enforced on the fast-charge phase, then reset, and enforced again on the top-off phase, if selected. There is no time limit on the trickle-charge phase.

Top-off Charge

An optional top-off charge phase may be selected to follow fast charge termination for 1C and C/2 rates. This phase may be necessary on NiMH or other battery chemistries that have a tendency to terminate charge prior to reaching full capacity. With top-off enabled, charging continues at a reduced rate after fast-charge termination for a period of time selected by the TM pin. (See Table 1.) During top-off, the CC pin is modulated at a duty cycle of 286µs active for every 4290µs inactive. This modulation results in an average rate 1/16th that of the fast charge rate. Maximum voltage, time, and temperature are the only termination methods enabled during top-off.

Pulse-Trickle Charge

Pulse-trickle is used to compensate for self-discharge while the battery is idle in the charger. The battery is pulse-trickle charged by driving the CC pin active for a period of 286µs for every 18.0ms of inactivity for 1C and 2C selections, and 286µs for every 8.86ms of inactivity for C/2 selection. This results in a trickle rate of C/64 for the top-off enabled mode and C/32 otherwise.

TM Pin

The TM pin is a three-level pin used to select the charge timer, top-off, voltage termination mode, trickle rate, and voltage hold-off period options. Table 1 describes the states selected by the TM pin. The mid-level selection input is developed by a resistor divider between V_{CC} and ground that fixes the voltage on TM at $V_{CC}/2 \pm 0.5V$. See Figure 4.

Charge Status Indication

A fast charge in progress is uniquely indicated when the $\overline{LED}$ pin goes low. The $\overline{LED}$ pin is driven to the high-Z state for all conditions other than fast charge. Figure 2 outlines the state of the $\overline{LED}$ pin during charge.

Charge Inhibit

Fast charge and top-off may be inhibited by using the INH pin. When high, INH suspends all fast charge and top-off activity and the internal charge timer. INH freezes the current state of $\overline{LED}$ until inhibit is removed. Temperature monitoring is not affected by the INH pin. During charge inhibit, the bq2002/F continues to pulse-trickle charge the battery per the TM selection. When INH returns low, charge control and the charge timer resume from the point where INH became active.

Low-Power Mode

The IC enters a low-power state when V_{BAT} is driven above the power-down threshold (V_{PD}) where

$$V_{PD} = V_{CC} - (1V \pm 0.5V)$$

Both the CC pin and the $\overline{LED}$ pin are driven to the 16 4 -1ry

Absolute Maximum Ratings

Recommended DC Operating Conditions (T_A = 0 to 70°C)

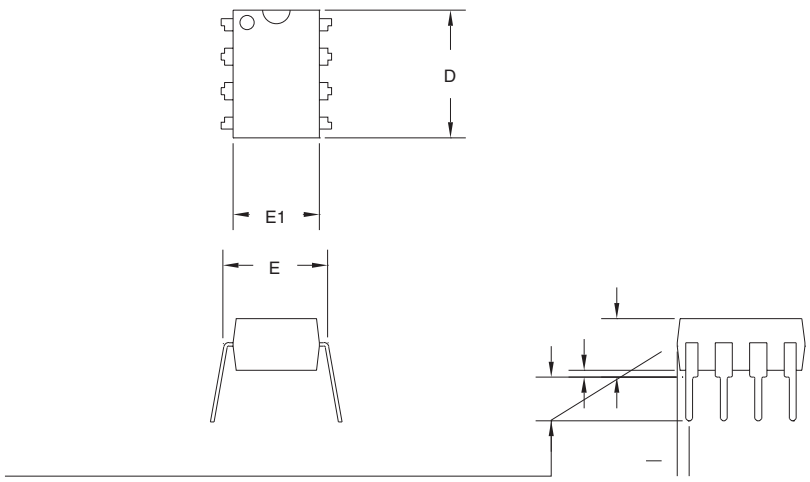
Symbol	Condition	Minimum	Typical	Maximum	Unit	Notes
V_{CC}	Supply voltage	4.0	5.0	6.0	V	
V_{DET}	-ΔV, PVD detect voltage	1	-	2	V	

Impedance

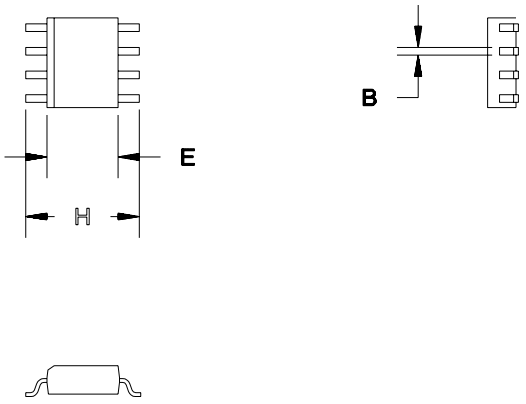
Symbol	Parameter	Minimum	Typical	Maximum	Unit
R_{BAT}	Battery input impedance	50	-	-	MΩ
R_{TS}	TS input impedance	50	-	-	MΩ

Timing (T_A = 0 to +70°C; V_{CC} ±10%)

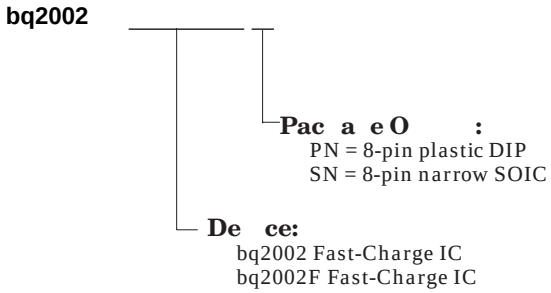
Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
d_{FCV}	Base time variation	-20	-	20	%	


D
E1
E

8-Pin SOIC Narrow (SN)



Ordering Information



Data Sheet Revision History

Change No.[1]	Page No.	Description	Nature of Change
1	3	Was: Table 1 gave the bq2002/F Operational Summary. Is: Figure 2 gives the bq2002/F Operational Summary.	Changed table to figure.
1	5	Summy Addre Is: include 4[illegible]	[illegible]

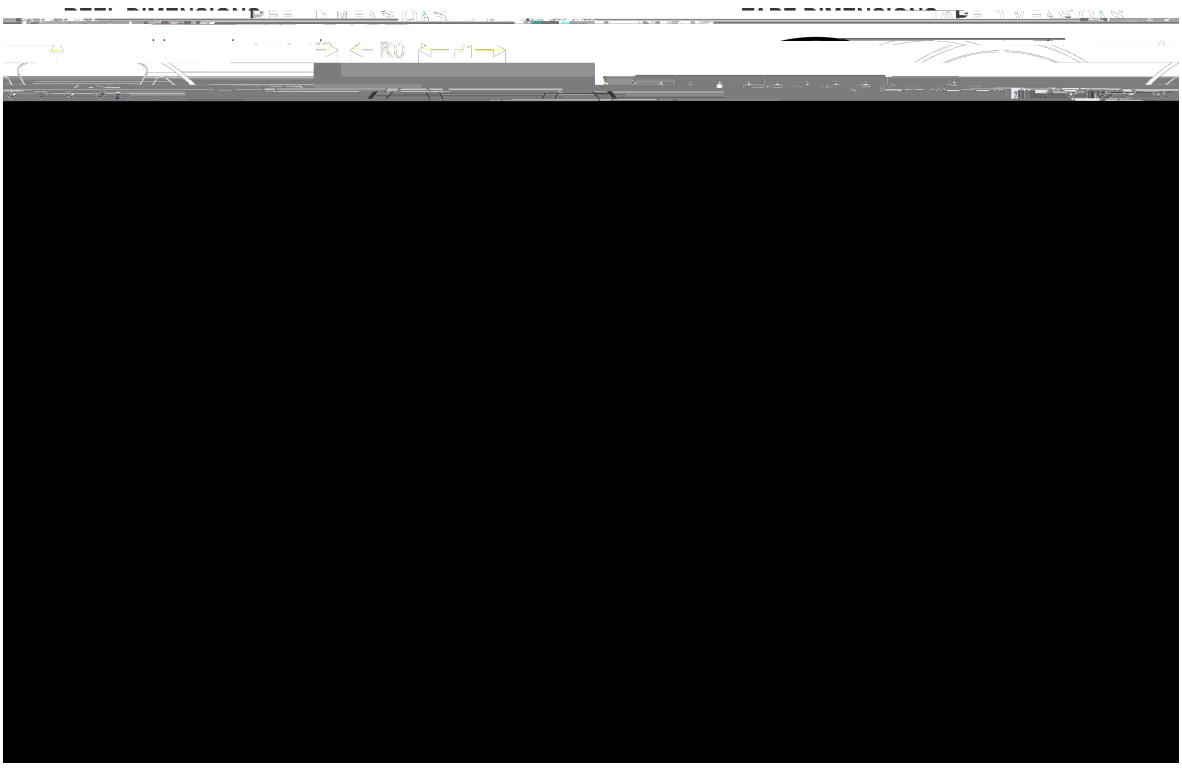
PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

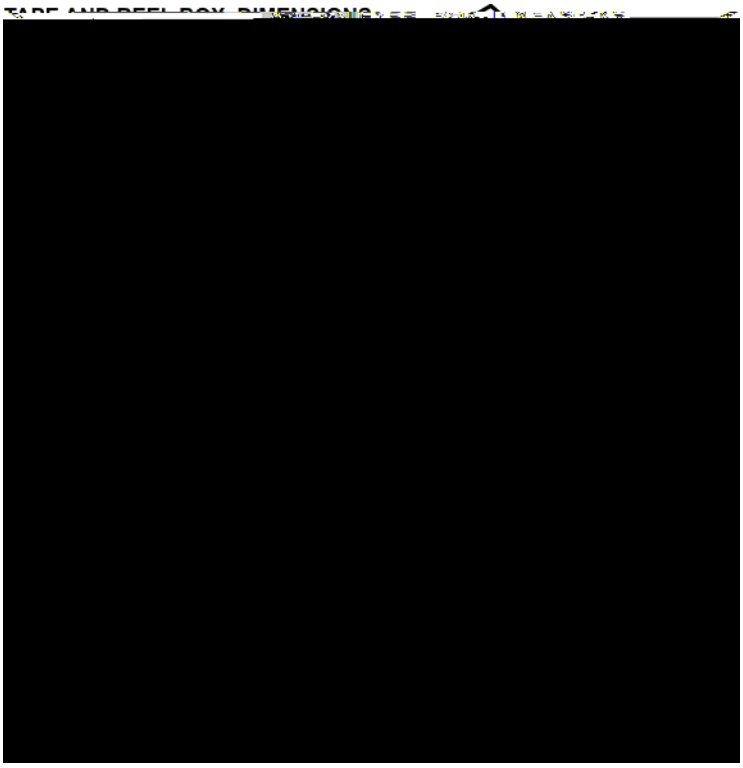
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2002FSNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
BQ2002SN-SANTR	SOIC	D	8	0	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
BQ2002SNTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ2002FSNTR	SOIC	D	8	2500	340.5	338.1	20.6
BQ2002SN-SANTR	SOIC	D	8	0	340.5	338.1	20.6
BQ2002SNTR	SOIC	D	8	2500	340.5	338.1	20.6

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