

## **Features**

- Conservative and repeatable measurement of available charge in rechargeable batteries
- Designed for portable equipment such as power tools with high discharge rates
-

## Pin Descriptions

### MODE Display mode output

When left floating, this output selects relative mode for capacity display. If connected to the anode of the LEDs to source current, absolute mode is selected for capacity display. See Table 1.

### SEG<sub>1</sub>– SEG<sub>5</sub> LED display segment outputs

Each output may activate an LED to sink the current sourced from MODE, the battery, or V<sub>CC</sub>.

### PFC Programmed full count selection input

This three-level input pin defines the programmed full count (PFC) thresholds and scale selections described in Table 1. The state of the PFC pin is only read immediately after a reset condition.

### SR Sense resistor input

The voltage drop (V<sub>SR</sub>) across the sense resistor R<sub>S</sub> is monitored and integrated over time to interpret charge and discharge activity. The SR input is tied to the low side of the sense resistor. V<sub>SR</sub> > V<sub>SS</sub> indicates discharge, and V<sub>SR</sub> < V<sub>SS</sub> indicates charge. The effective voltage drop, V<sub>SRO</sub>, as seen by the bq2011 is V<sub>SR</sub> + V<sub>OS</sub> (see Table 3).

### NC No connect

### $\overline{\text{DISP}}$

### Display control input

$\overline{\text{DISP}}$  floating allows the LED display to be active during charge and discharge if V<sub>SRO</sub> < -1mV (charge) or V<sub>SRO</sub> > 2mV (discharge). Transitioning  $\overline{\text{DISP}}$  low activates the display for 4  $\mu$ s.

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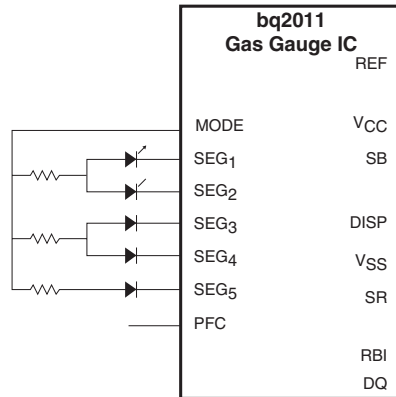
## Functional Description

### General Operation

The bq2011 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2011 measures discharge and charge currents, estimates self-discharge, monitors the battery for low-battery voltage thresholds, and compensates for temperature and charge/discharge rates. The charge measurement is made by monitoring the voltage across a small-value series sense resistor between the negative battery terminal and ground. The available battery charge is determined by monitoring this voltage over time and correcting the measurement for the environmental and operating conditions.

Figure 1 shows a typical battery pack application of the bq2011 using the LED display with absolute mode as a charge-state indicator. The bq2011 can be configured to display capacity in either a relative or an absolute display mode. The relative display mode uses the last measured discharge capacity of the battery as the battery "full" reference. The absolute display mode uses the programmed full count (PFC) as the full reference, forcing each segment of the display to represent a fixed amount of charge. A push-button display feature is available for momentarily enabling the LED display.

The bq2011 monitors the charge and discharge currents as a voltage across a sense resistor (see  $R_s$  in Figure 1). A filter between the negative battery terminal and the SR pin may be required if the rate of change of the battery current is too great.



## Register Backup

The bq2011 RBI input pin is intended to be used with a storage capacitor to provide backup potential to the internal bq2011 registers when  $V_{CC}$  momentarily drops below 3.0V.  $V_{CC}$  is output on RBI when  $V_{CC}$  is above 3.0V.

After  $V_{CC}$  rises above 3.0V, the bq2011 checks the internal registers for data loss or corruption. If data has changed, then the NAC and FULCNT registers are cleared, and the LMD register is loaded with the initial PFC.

## Voltage Thresholds

In conjunction with monitoring  $V_{SR}$  for charge/discharge currents, the bq2011 monitors the single-cell battery potential through the SB pin. The single-cell voltage potential is determined through a resistor-divider network per the following equation:

$$\frac{RB_1}{RB_2} = N - 1$$

where N is the number of cells,  $RB_1$  is connected to the positive battery terminal, and  $RB_2$  is connected to the negative battery terminal. The single-cell battery voltage is monitored for the end-of-discharge voltage (EDV) and for maximum cell voltage (MCV). The EDV threshold level is used to determine when the battery has reached an “empty” state, and the MCV threshold is used for fault detection during charging. The EDV and MCV thresholds for the bq2011 are fixed at:

$$\begin{aligned} V_{EDV} &= 0.90V \\ V_{MCV} &= 2.00V \end{aligned}$$

During discharge and charge, the bq2011 monitors  $V_{SR}$  for various thresholds,  $V_{SR1}$ – $V_{SR4}$ . These thresholds are used to compensate the charge and discharge rates. Refer to the discharge compensation section for details. EDV monitoring is disabled if  $V_{SR} \geq V_{SR1}$  (50mV typical) and resumes 1 second after  $V_{SR}$  drops back below  $V_{SR1}$ .

## Reset

The bq2011 recognizes a valid battery whenever  $V_{SB}$  is greater than 0.1V typical.  $V_{SB}$  rising from below 0.25V resets the device. Reset can also be accomplished with a command over the serial port as described in the Reset Register section.

## Temperature

The bq2011 internally determines the temperature in 10°C steps centered from -35°C to +85°C. The temperature steps are used to adapt charge and discharge rate compensations, self-discharge counting, and available

charge display translation. The temperature range is available over the serial port in 10°C increments as shown below:

| TMPGG (hex) | Temperature Range |
|-------------|-------------------|
| 0x          | < -30°C           |
| 1x          | -30°C to -20°C    |
| 2x          | -20°C to -10°C    |
| 3x          | -10°C to 0°C      |
| 4x          | 0°C to 10°C       |
| 5x          | 10°C to 20°C      |
| 6x          | 20°C to 30°C      |
| 7x          | 30°C to 40°C      |
| 8x          | 40°C to 50°C      |
| 9x          | 50°C to 60°C      |
| Ax          | 60°C to 70°C      |
| Bx          | 70°C to 80°C      |
| Cx          | > 80°C            |

## Layout Considerations

The bq2011 measures the voltage differential between the SR and  $V_{SS}$  pins.  $V_{OS}$  (the offset voltage at the SR pin) is greatly affected by PC board layout. For optimal results, the PC board layout should follow the strict rule of a single-point ground return. Sharing high-current ground with small signal ground causes undesirable noise on the small signal nodes. Additionally:

- The capacitors (SB and  $V_{CC}$ ) should be placed as close as possible to the SB and  $V_{CC}$  pins, respectively, and their paths to  $V_{SS}$  should be as short as possible. A high-quality ceramic capacitor of 0.1µf is recommended for  $V_{CC}$ .
- The sense resistor ( $R_S$ ) should be as close as possible to the bq2011.
- The R-C on the SR pin should be located as close as possible to the SR pin. The maximum R should not exceed 20K.

## Gas Gauge Operation

The operational overview diagram in Figure 2 illustrates the operation of the bq2011. The bq2011 accumulates a measure of charge and discharge currents, as well as an estimation of self-discharge. Charge and discharge currents are temperature and rate compensated, whereas self-discharge is only temperature compensated.

The main counter, Nominal Available Charge (NAC), represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register and increment the DCR (Discharge Count Register).

The Discharge Count Register (DCR) is used to update the Last Measured Discharge (LMD) register only if a complete battery discharge from full to empty occurs without any partial battery charges. Therefore, the bq2011 adapts its capacity determination based on the actual conditions of discharge.

The battery's initial capacity is equal to the Pro-

**E** **FC**

Select:

Given:

- Sense resistor = 0.005Ω
- Number of cells = 6
- Capacity = 1300mAh, NiCd cells
- Current range = 1A to 80A
- Relative display mode
- Self-discharge = %<sub>64</sub>
- Voltage drop over sense resistor = 5mV to 400mV

- PFC = 34304 counts or 6.5mVh
- PFC = Z (float)
- MODE = not connected

The initial full battery capacity is 6.5mVh (1300mAh) until the bq2011 “learns” a new capacity with a qualified discharge from full to EDV.

Therefore:

$$1300\text{mAh} * 0.005\Omega = 6.5\text{mVh}$$

| PFC | Programmed Full Count (PFC) | mVh  | Scale                                   | MODE Pin | Display Mode |
|-----|-----------------------------|------|---|----------|--------------|
| H   | 27648                       | 10.5 | bq2011TE91.261011TE91283.8231.20011T055 | TD105    |              |

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### 3. Nominal Available Charge (NAC):

NAC counts up during charge to a maximum value of LMD and down during discharge and self discharge to 0. NAC is reset to 0 on initialization and on the first valid charge following discharge to EDV. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

**Note:** NAC is set to the value in LMD when SEG<sub>5</sub> is pulled low during a reset.

### 4. Discharge Count Register (DCR):

The DCR counts up during discharge independent of NAC and could continue increasing after NAC has decremented to 0. Prior to NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when NAC = LMD. The DCR does not roll over but stops counting when it reaches FFFFh.

The DCR value becomes the new LMD value on the first charge after a valid discharge to V<sub>EDV</sub> if:

- No valid charge initiations (charges greater than 256 NAC counts; or 0.006 – 0.01C) occurred during the period between NAC = LMD and EDV detected.
- The self-discharge count is not more than 4096 counts (8% to 18% of PFC, specific percentage threshold determined by PFC).
- The temperature is  $\geq 0^{\circ}\text{C}$  when the EDV level is reached during discharge.

The valid discharge flag (VDQ) indicates whether the present discharge is valid for LMD update.

### Charge Counting

Charge activity is detected based on a negative voltage on the V<sub>SR</sub> input. If charge activity is detected, the bq2011 increments NAC at a rate proportional to V<sub>SRO</sub> (V<sub>SR</sub> + V<sub>OS</sub>) and, if enabled, activates an LED display if V<sub>SRO</sub> < -1mV. Charge actions increment the NAC after compensation for charge rate and temperature.

The bq2011 determines a valid charge activity sustained at a continuous rate equivalent to V<sub>SRO</sub> < -400 $\mu\text{V}$ . A valid charge equates to a sustained charge activity greater than 256 NAC counts. Once a valid charge is detected, charge counting continues until V<sub>SRO</sub> rises above -400 $\mu\text{V}$ .

### Discharge Counting

All discharge counts where V<sub>SRO</sub> > 500 $\mu\text{V}$  cause the NAC register to decrement and the DCR to increment. Exceeding the fast discharge threshold (FDQ) if the rate is equivalent to V<sub>SRO</sub> > 2mV activates the display, if enabled. The display becomes inactive after V<sub>SRO</sub> falls below 2mV.

### Self-Discharge Estimation

The bq2011 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal  $\frac{1}{80} * \text{NAC}$  rate per day. This is the rate for a battery whose temperature is between 20°–30°C. The NAC register cannot be decremented below 0.

### Count Compensations

The bq2011 determines fast charge when the NAC updates at a rate of  $\geq 2$  counts/sec. Charge and discharge activity is compensated for temperature and charge/discharge rate before updating the NAC and/or DCR. Self-discharge estimation is compensated for temperature before updating the NAC or DCR.

### Charge Compensation

Two charge efficiency factors are used for trickle charge and fast charge. Fast charge is defined as a rate of charge resulting in  $\geq 2$  NAC counts/sec ( $\geq 0.15\text{C}$  to  $0.32\text{C}$  depending on PFC selections; see Table 2). The compensation defaults to the fast charge factor until the actual charge rate is determined.

Temperature adapts the charge rate compensation factors over three ranges between nominal, warm, and hot temperatures. The compensation factors are shown below.

| Charge Temperature        | Trickle Charge Compensation | Fast Charge Compensation |
|---------------------------|-----------------------------|--------------------------|
| <40°C                     | 0.80                        | 0.95                     |
| $\geq 40^{\circ}\text{C}$ | 0.75                        | 0.90                     |

## Discharge Compensation

Corrections for the rate of discharge are made by adjusting an internal discharge compensation factor. The discharge factor is based on the dynamically measured  $V_{SR}$ . The compensation factors during discharge are:

Temperature compensation during discharge also takes place. At lower temperatures, the compensation factor increases by 0.05 for each 10°C temperature step below 10°C.

$$\text{Comp. factor} = 1.00 + (0.05 * N)$$

Where N = number of 10°C steps below 10°C and  $V_{SR} < 50\text{mV}$ .

For example:

T > 10°C: Nominal compensation, N = 0

0°C < T < 10°C: N = 1 (i.e., 1.00 becomes 1.05)

-10°C < T < 0°C: N = 2 (i.e., 1.00 becomes 1.10)

-20°C < T < -10°C: N = 3 (i.e., 1.00 becomes 1.15)

-30°C < T < -20°C: N = 4 (i.e., 1.00 becomes 1.20)

## Self-Discharge Compensation

The self-discharge compensation is programmed for a nominal rate of  $\frac{1}{60} * \text{NAC}$  per day. This is the rate for a battery within the 20–30°C temperature range (TMPGG = 6x). This rate varies across 8 ranges from <10°C to >70°C, doubling with each higher temperature step (10°C). See Table 2

## Error Summary

### Capacity Inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual



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## Communicating with the bq2011

The bq2011 includes a simple single-pin (DQ plus return) serial data interface. A host processor uses the interface to access various bq2011 registers. Battery characteristics may be easily monitored by adding a single contact to the battery pack. The open-drain DQ pin on the bq2011 should be pulled up by the host system, or may be left floating if the serial interface is not used.

The interface uses a command-based protocol, where the host processor sends a command byte to the bq2011. The command directs the bq2011 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte.

The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 333 bits/sec. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2011 may be sampled using the pulse-width capture timers available on some microcontrollers.

Communication is normally initiated by the host processor sending a BREAK command to the bq2011. A BREAK is detected when the DQ pin is driven to a logic-low state for a time,  $t_B$  or greater. The DQ pin should then be returned to its normal ready-high logic state for a time,  $t_{BR}$ . The bq2011 is now ready to receive a command from the host processor.

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2011 taking the DQ pin to a

logic-low state for a period,  $t_{STRH,B}$ . The next section is the actual data transmission, where the data should be valid by a period,  $t_{DSU}$ , after the negative edge used to start communication. The data should be held for a period,  $t_{DV}$ , to allow the host or bq2011 to sample the data bit.

The final section is used to stop the transmission by returning the DQ pin to a logic-high state by at least a period,  $t_{SSU}$ , after the negative edge used to start communication. The final logic-high state should be held until a period,  $t_{SV}$ , to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

Communication with the bq2011 is always performed with the least-significant bit being transmitted first. Figure 3 shows an example of a communication sequence to read the bq2011 NAC register.

## bq2011 Registers

The bq2011 command and status registers are listed in Table 4 and described below.

### Command Register (CMDR)

The write-only CMDR register is accessed when eight valid command bits have been received by the bq2011. The CMDR register contains two fields:

- $W/\bar{R}$  bit
- Command address

The  $W/\bar{R}$  bit of the command register is used to select whether the received command is for a read or a write function.

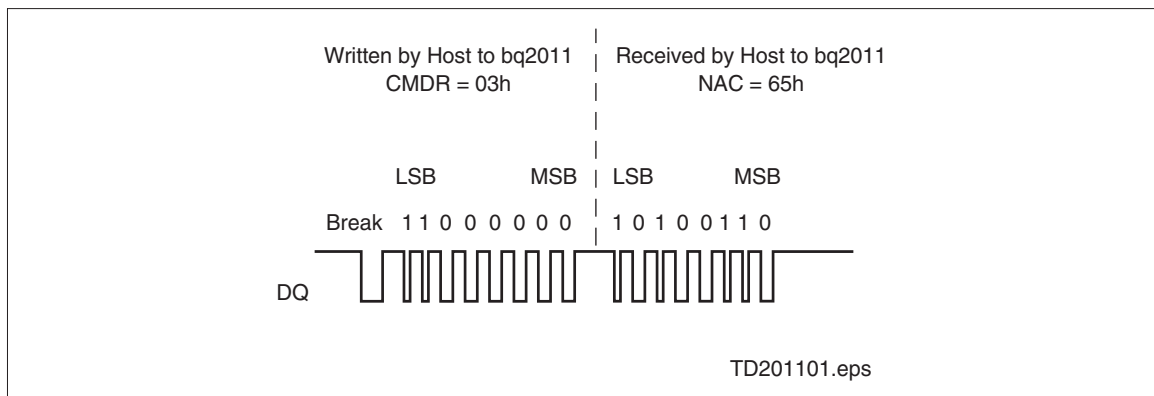


Figure 3. Typical Communication with the bq2011

Table 4. bq2011 Command and Status Registers

| Symbol | Register Name                               | Loc. (hex) | Read/Write | Control Field |        |        |        |        |        |        |        |
|--------|---|------------|------------|---------------|--------|--------|--------|--------|--------|--------|--------|
|        |   |            |            | 7(MSB)        | 6      | 5      | 4      | 3      | 2      | 1      | 0(LSB) |
| CMDR   | Command register                            | 00h        | Write      | W/R           | AD6    | AD5    | AD4    | AD3    | AD2    | AD1    | AD0    |
| FLGS1  | Primary status flags register               | 01h        | Read       | CHGS          | BRP    | MCV    | CI     | VDQ    | n/u    | EDV    | n/u    |
| TMPGG  | Temperature and gas gauge register          | 02h        | Read       | TMP3          | TMP2   | TMP1   | TMP0   | GG3    | GG2    | GG1    | GG0    |
| NACH   | Nominal available charge high byte register | 03h        | R/W        | NACH7         | NACH6  | NACH5  | NACH4  | NACH3  | NACH2  | NACH1  | NACH0  |
| NACL   | Nominal available charge low byte register  | 17h        | Read       | NACL7         | NACL6  | NACL5  | NACL4  | NACL3  | NACL2  | NACL1  | NACL0  |
| BATID  | Battery identification register             | 04h        | R/W        | BATID7        | BATID6 | BATID5 | BATID4 | BATID3 | BATID2 | BATID1 | BATID0 |
| LMD    | Last measured discharge register            | 05h        | R/W        | LMD7          | LMD6   | LMD5   | LMD4   | LMD3   | LMD2   | LMD1   | LMD0   |
| FLGS2  | Secondary status flags register             | 06h        | Read       | CR            | DR2    | DR1    | DR0    | n/u    | n/u    | n/u    | OVLD   |
| CPI    | Capacity inaccurate count register          | 09h        | Read       | CPI7          | CPI6   | CPI5   | CPI4   | CPI3   | CPI2   | CPI1   | CPI0   |
| OCTL   | Output control register                     | 0ah        | Write      | 1             | OC5    | OC4    | OC3    | OC2    | OC1    | n/u    | OCE    |
| FULCNT | Full count register                         | 0bh        | Read       | FUL7          | FUL6   | FUL5   | FUL4   | FUL3   | FUL2   | FUL1   | FUL0   |
| RST    | Reset register                              | 39h        | Write      | RST           | 0      | 0      | 0      | 0      | 0      | 0      | 0      |

**Note:** n/u = not used

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The W/R values are:

| CMDR Bits |   |   |   |   |   |   |   |
|-----------|---|---|---|---|---|---|---|
| 7         | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| W/R       | - | - | - | - | - | - | - |

Where W/R is:

- 0 The bq2011 outputs the requested register contents specified by the address portion of CMDR.
- 1 The following eight bits should be written to the register specified by the address portion of CMDR.

The lower seven-bit field of CMDR contains the address portion of the register to be accessed. Attempts to write to invalid addresses are ignored.

| CMDR Bits |     |     |     |     |     |     |           |
|-----------|-----|-----|-----|-----|-----|-----|-----------|
| 7         | 6   | 5   | 4   | 3   | 2   | 1   | 0         |
| -         | AD6 | AD5 | AD4 | AD3 | AD2 | AD1 | AD0 (LSB) |

## Primary Status Flags Register (FLGS1)

The read-only FLGS1 register (address=01h) contains the primary bq2011 flags.

The CHGS flag (CHGS) is asserted when a valid charge rate is detected. Charge rate is deemed valid when  $V_{SRO} < -400\mu V$ . A  $V_{SRO}$  of greater than  $-400\mu V$  or discharge activity clears CHGS.

The CHGS values are:

| FLGS1 Bits |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CHGS       | - | - | - | - | - | - | - |

Where CHGS is:

- 0 Either discharge activity detected or  $V_{SRO} > -400\mu V$
- 1  $V_{SRO} < -400\mu V$

The BRP flag (BRP) is asserted whenever the potential on the SB pin (relative to  $V_{SS}$ ),  $V_{SB}$ , rises above 0.1V and determines the internal registers have been corrupted. The BRP flag is also set when the bq2011 is reset (see the RST register description). BRP is latched until either the bq2011 is charged until NAC = LMD or discharged until EDV is reached. BRP = 1 signifies that the device has been reset.

The BRP values are:

| FLGS1 Bits |     |   |   |   |   |   |   |
|------------|-----|---|---|---|---|---|---|
| 7          | 6   | 5 | 4 | 3 | 2 | 1 | 0 |
| -          | BRP | - | - | - | - | - | - |

Where BRP is:

- 0 bq2011 is charged until NAC = LMD or discharged until the EDV flag is asserted
- 1 SB rising from below 0.1V, or a serial port initiated reset has occurred

The MCV flag (MCV) is asserted whenever the potential on the SB pin (relative to  $V_{SS}$ ) is above 2.0V. The MCV flag is asserted until the condition causing MCV is removed.

The MCV values are:

| FLGS1 Bits |   |     |   |   |   |   |   |
|------------|---|-----|---|---|---|---|---|
| 7          | 6 | 5   | 4 | 3 | 2 | 1 | 0 |
| -          | - | MCV | - | - | - | - | - |

Where MCV is:

- 0  $V_{SB} < 2.0V$
- 1  $V_{SB} > 2.0V$

The CI flag (CI) is used to warn the user that the battery has been charged a substantial number of times since LMD has been updated. The CI flag is asserted on the 64th charge after the last LMD update or when the bq2011 is reset. The flag is cleared after an LMD update.

The CI values are:

| FLGS1 Bits |   |   |    |   |   |   |   |
|------------|---|---|----|---|---|---|---|
| 7          | 6 | 5 | 4  | 3 | 2 | 1 | 0 |
| -          | - | - | CI | - | - | - | - |

Where CI is:

- 0 When LMD is updated with a valid full discharge or the bq2011 is reset
- 1 After the 64th valid charge action with no LMD updates



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The gas gauge display and the gas gauge portion of the TMPGG register are adjusted for cold temperature dependencies. A piece-wise correction is performed as follows:

| Temperature     | Available Capacity Calculation |
|-----------------|--------------------------------|
| > 0°C           | NAC / "Full Reference"         |
| -20°C < T < 0°C | 0.75 * NAC / "Full Reference"  |
| < -20°C         | 0.5 * NAC / "Full Reference"   |

The adjustment between > 0°C and -20°C < T < 0°C has a 4°C hysteresis.

## Nominal Available Charge Register (NAC)

The read/write NACH register (address=03h) and the read-only NACL register (address=17h) are the main gas gauging registers for the bq2011. The NAC registers are incremented during charge actions and decremented during discharge and self-discharge actions. The correction factors for charge/discharge efficiency are applied automatically to NAC.

On reset, the NACH and NACL registers are cleared to zero. NACL stops counting when NACH reaches zero. When the bq2011 detects a valid charge, NACL resets to zero; *writing to the NAC register affects the available charge counts and, therefore, affects the bq2011 gas gauge operation.*

## Battery Identification Register (BATID)

The read/write BATID register (address=04h) is available for use by the system to determine the type of battery pack. The BATID contents are retained as long as V<sub>CC</sub> is greater than 2V. The contents of BATID have no effect on the operation of the bq2011. There is no default setting for this register.

## Last Measured Discharge Register (LMD)

LMD is a read/write register (address=05h) that the bq2011 uses as a measured full reference. The bq2011 adjusts LMD based on the measured discharge capacity of the battery from full to empty. In this way the bq2011 updates the capacity of the battery. LMD is set to PFC during a bq2011 reset.

## Secondary Status Flags Register (FLGS2)

The read-only FLGS2 register (address=06h) contains the secondary bq2011 flags.

The CR flag (CR) is used to denote the fast charge regime. Fast charge is assumed whenever a charge action is initiated. The CR flag remains asserted if the charge rate does not fall below 2 counts/sec.

The CR values are:

| FLGS2 Bits |   |   |   |   |   |   |   |
|------------|---|---|---|---|---|---|---|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| CR         | - | - | - | - | - | - | - |

Where CR is:

- 0 When charge rate falls below 2 counts/sec
- 1 When charge rate is above 2 counts/sec

The fast charge regime efficiency factors are used when CR = 1. When CR = 0, the trickle charge efficiency factors are used. The time to change CR varies due to the user-selectable count rates.

The DR2, DR1, DR0 flags, DR2-0, are bits 6-4.

| FLGS2 Bits |     |     |     |   |   |   |   |
|------------|-----|-----|-----|---|---|---|---|
| 7          | 6   | 5   | 4   | 3 | 2 | 1 | 0 |
| -          | DR2 | DR1 | DR0 | - | - | - | - |

They are used to determine the present discharge regime as follows:

| DR2 | DR1 | DR0 | V <sub>SR</sub> (V)                               |
|-----|-----|-----|---|
| 0   | 0   | 0   | V <sub>SR</sub> < 50mV                            |
| 0   | 0   | 1   | 50mV < V <sub>SR</sub> < 100mV (overload, OVLD=1) |
| 0   | 1   | 0   | 100mV < V <sub>SR</sub> < 150mV                   |
| 0   | 1   | 1   | 150mV < V <sub>SR</sub> < 253mV                   |
| 1   | 0   | 0   | V <sub>SRD</sub> > 253mV                          |

The OVLD flag (OVLD) is asserted when a discharge overload is detected, V<sub>SRD</sub> > 50mV. OVLD remains asserted as long as the condition persists and is cleared when V<sub>SRD</sub> < 50mV.

| FLGS2 Bits |   |   |   |   |   |   |      |
|------------|---|---|---|---|---|---|------|
| 7          | 6 | 5 | 4 | 3 | 2 | 1 | 0    |
| -          | - | - | - | - | - | - | OVLD |

DR2-0 and OVLD are set based on the measurement of the voltage at the SR pin relative to V<sub>SS</sub>. The rate at which this measurement is made varies with device activity.

### Full Count Register (FULCNT)

The read-only FULCNT register (address=0bh) provides the system with a diagnostic of the number of times the battery has been fully charged (NAC = LMD). The number of full occurrences can be determined by multiplying the value in the FULCNT register by 16. Any discharge action other than self-discharge allows detection of another full occurrence during the next valid charge action.

### Capacity Inaccurate Count Register (CPI)

The read-only CPI register (address=09h) is used to indicate the number of times a battery has been charged without an LMD update. Because the capacity of a rechargeable battery varies with age and operating conditions, the bq2011 adapts to the changing capacity over time. A complete discharge from full (NAC=LMD) to empty (EDV=1) is required to perform an LMD update assuming there have been no intervening valid charges, the temperature is greater than or equal to 0°C, and the self-discharge counter is less than 4096 counts.

The CPI register is incremented every time a valid charge is detected. The register increments to 255 without rolling over. When the contents of CPI are incremented to 64, the capacity inaccurate flag, CI, is asserted in the FLGS1 register. CPI is reset whenever an update of the LMD register is performed, and the CI flag is also cleared.

### Output Control Register (OCTL)

The write-only OCTL register (address=0ah) provides the system with a means to check the display connections for the bq2011. The segment drivers may be overwritten by data from OCTL when the least-significant bit of OCTL, OCE, is set. The data in bits OC<sub>5-1</sub> of the OCTL register (see Table 4 on page 10 for details) is output onto the segment pins, SEG<sub>5-1</sub>, respectively if OCE=1. *Whenever OCE is written to 1, the MSB of OCTL should be set to a 1.* The OCE register location must be cleared to return the bq2011 to normal operation. OCE may be cleared by either writing the bit to a logic zero via the serial port or by resetting the bq2011 as explained below. **Note:** Whenever the OCTL register is

# bq2011

## Absolute Maximum Ratings

| Symbol           | Parameter                   | Minimum | Maximum | Unit | Notes   |
|------------------|-----------------------------|---------|---------|------|---|
| V <sub>CC</sub>  | Relative to V <sub>SS</sub> | -0.3    | +7.0    | V    |   |
| All other pins   | Relative to V <sub>SS</sub> | -0.3    | +7.0    | V    |   |
| V <sub>SR</sub>  | Relative to V <sub>SS</sub> | -0.3    | +7.0    | V    | Minimum 100Ω series resistor should be used to protect SR in case of a shorted battery (see the bq2011 application note for details). |
| T <sub>OPR</sub> | Operating temperature       | 0       | +70     | °C   | Commercial  |

**Note:** Permanent device damage may occur if **Absolute Maximum Ratings** are exceeded. Functional operation should be limited to the Recommended DC Operating Conditions detailed in this data sheet. Exposure to conditions beyond the operational limits for extended periods of time may affect device reliability.

## DC Voltage Thresholds (T<sub>A</sub> = T<sub>OPR</sub>; V = 3.0 to 6.5V)

| Symbol           | Parameter                        | Minimum | Typical | Maximum | Unit | Notes                             |
|------------------|----------------------------------|---------|---------|---------|------|-----------------------------------|
| V <sub>EDV</sub> | End-of-discharge warning         | 0.87    | 0.90    | 0.93    | V    | SB                                |
| V <sub>SR1</sub> | Discharge compensation threshold | 20      | 50      | 75      | mV   | SR (see note)                     |
| V <sub>SR2</sub> | Discharge compensation threshold | 70      | 100     | 125     | mV   | SR (see note)                     |
| V <sub>SR3</sub> | Discharge compensation threshold | 120     | 150     | 175     | mV   | SR (see note)                     |
| V <sub>SR4</sub> | Discharge compensation threshold | 220     | 253     | 275     | mV   | SR (see note)                     |
| V <sub>SRQ</sub> | Valid charge                     | -       | -       | -400    | μV   | V <sub>SR</sub> + V <sub>OS</sub> |
| V <sub>SRD</sub> | Valid discharge                  | 500     | -       | -       | μV   | V <sub>SR</sub> + V <sub>OS</sub> |
| V <sub>MCV</sub> | Maximum single-cell voltage      | 1.95    | 2.0     | 2.05    | V    | SB                                |
| V <sub>BR</sub>  | Battery removed/replaced         | -       | 0.1     | 0.25    | V    | SB                                |

**Note:** For proper operation of the threshold detection circuit, V<sub>CC</sub> must be at least 1.5V greater than the voltage being measured.

**DC Electrical Characteristics** ( $T_A = T_{OPR}$ )

| Symbol   | Parameter                   | Minimum | Typical  | Maximum | Unit | Notes   |
|----------|-----------------------------|---------|----------|---------|------|---|
| $V_{CC}$ | Supply voltage              | 3.0     | 4.25     | 6.5     | V    | $V_{CC}$ excursion from $< 2.0V$ to $\geq 3.0V$ initializes the unit. |
| $V_{OS}$ | Offset referred to $V_{SR}$ | -       | $\pm 50$ |         |      |   |



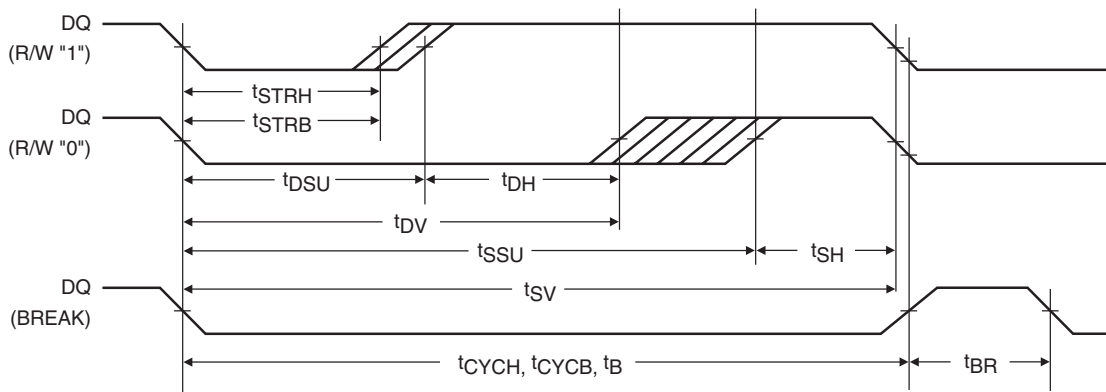
# bq2011

## Serial Communication Timing Specification ( $T_A = T_{OPR}$ )

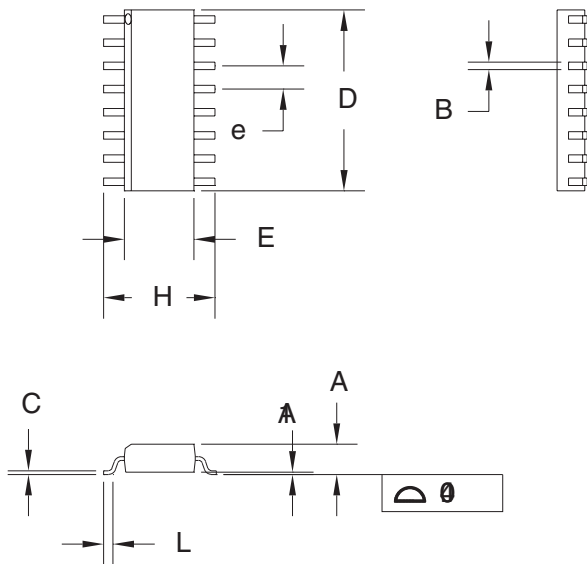
| Symbol            | Parameter                  | Minimum | Typical | Maximum | Unit | Notes    |
|-------------------|----------------------------|---------|---------|---------|------|----------|
| t <sub>CYCH</sub> | Cycle time, host to bq2011 | 3       | -       | -       | ms   | See note |
| t <sub>CYCB</sub> | Cycle time, bq2011 to host | 3       | -       | 6       | ms   |          |
| t <sub>STRH</sub> | Start hold, host to bq2011 | 5       | -       | -       | ns   |          |
| t <sub>STRB</sub> | Start hold, bq2011 to host | 500     | -       | -       | μs   |          |
| t <sub>DSU</sub>  | Data setup                 | -       | -       | 750     | μs   |          |
| t <sub>DH</sub>   | Data hold                  | 750     | -       | -       | μs   |          |
| t <sub>DV</sub>   | Data valid                 | 1.50    | -       | -       | ms   |          |
| t <sub>SSU</sub>  | Stop setup                 | -       | -       | 2.25    | ms   |          |
| t <sub>SH</sub>   | Stop hold                  | 700     | -       | -       | μs   |          |
| t <sub>SV</sub>   | Stop valid                 | 2.95    | -       | -       | ms   |          |
| t <sub>B</sub>    | Break                      | 3       | -       | -       | ms   |          |
| t <sub>BR</sub>   | Break recovery             | 1       | -       | -       | ms   |          |

**Note:** The open-drain DQ pin should be pulled to at least  $V_{CC}$  by the host system for proper DQ operation. DQ may be left floating if the serial interface is not used.

## Serial Communication Timing Illustration



16-Pin SOIC Narrow (SN)



16-Pin SN (SOIC Narrow)

| Dimension | Minimum | Maximum |
|-----------|---------|---------|
| A         | 0       | 0       |
| A         | 0       | 0       |
| B         | 0       | 0       |
| C         | 0       | 0       |
| D         | 0       | 0       |
| E         | 0       | 0       |
| e         | 0       | 0       |
| H         | 0       | 0       |
| L         | 0       | 0       |

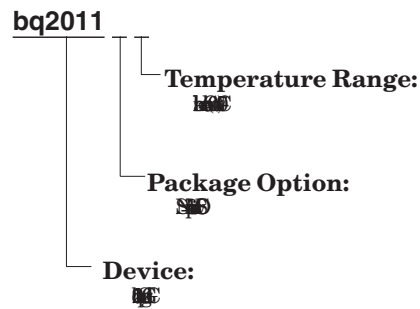
1616

### Data Sheet Revision History

| Change No. | Page No. | Description | Nature of Change              |
|------------|----------|-------------|-------------------------------|
| 3          | 7        | AV          | $\frac{1}{6}$ * $\frac{1}{8}$ |
| 3          | 7        | AV 0        | 0                             |
| 3          | 7        | AV 0        | 0                             |
| 4          | 7        |             |                               |
| 4          | 8        |             |                               |

Notes: ~~1995~~ 1995 Data Book.  
~~0-100C~~  
~~0-100D~~

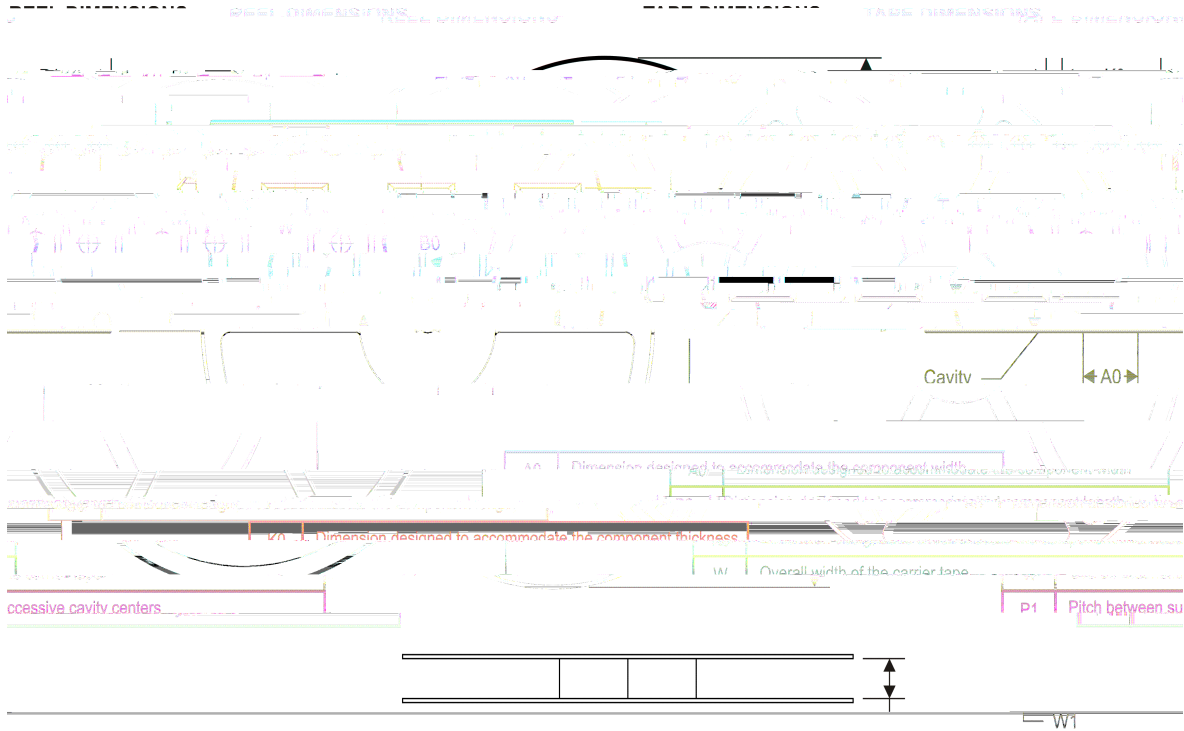
### Ordering Information



## PACKAGING INFORMATION

| Orderable Device | Status <sup>(1)</sup> | Package |
|------------------|-----------------------|---------|
|------------------|-----------------------|---------|

**TAPE AND REEL INFORMATION**

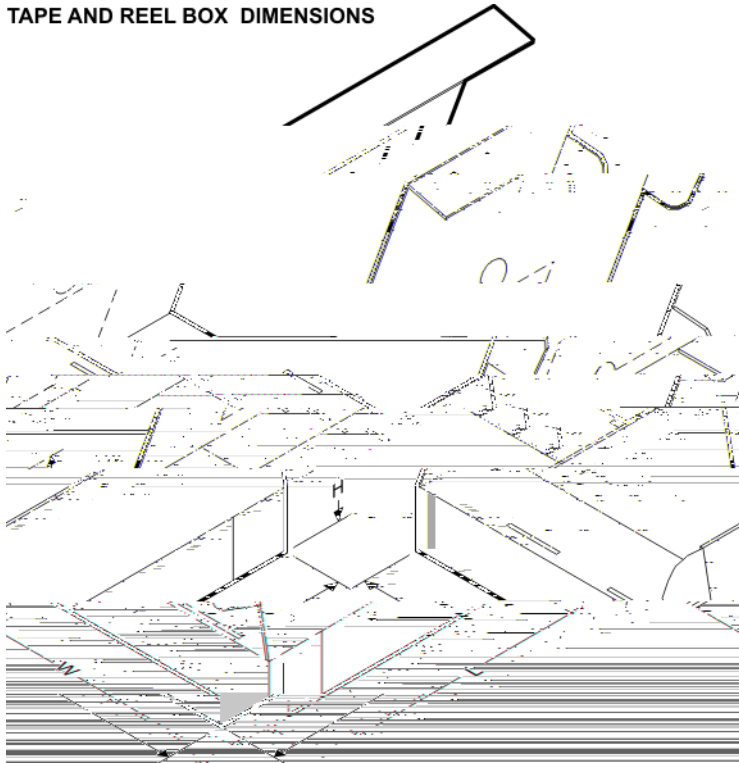


**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| BQ2011SN-D118TR | SOIC         | D               | 16   | 2500 | 330.0              | 16.4               | 6.5     | 10.3    | 2.1     | 8.0     | 16.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



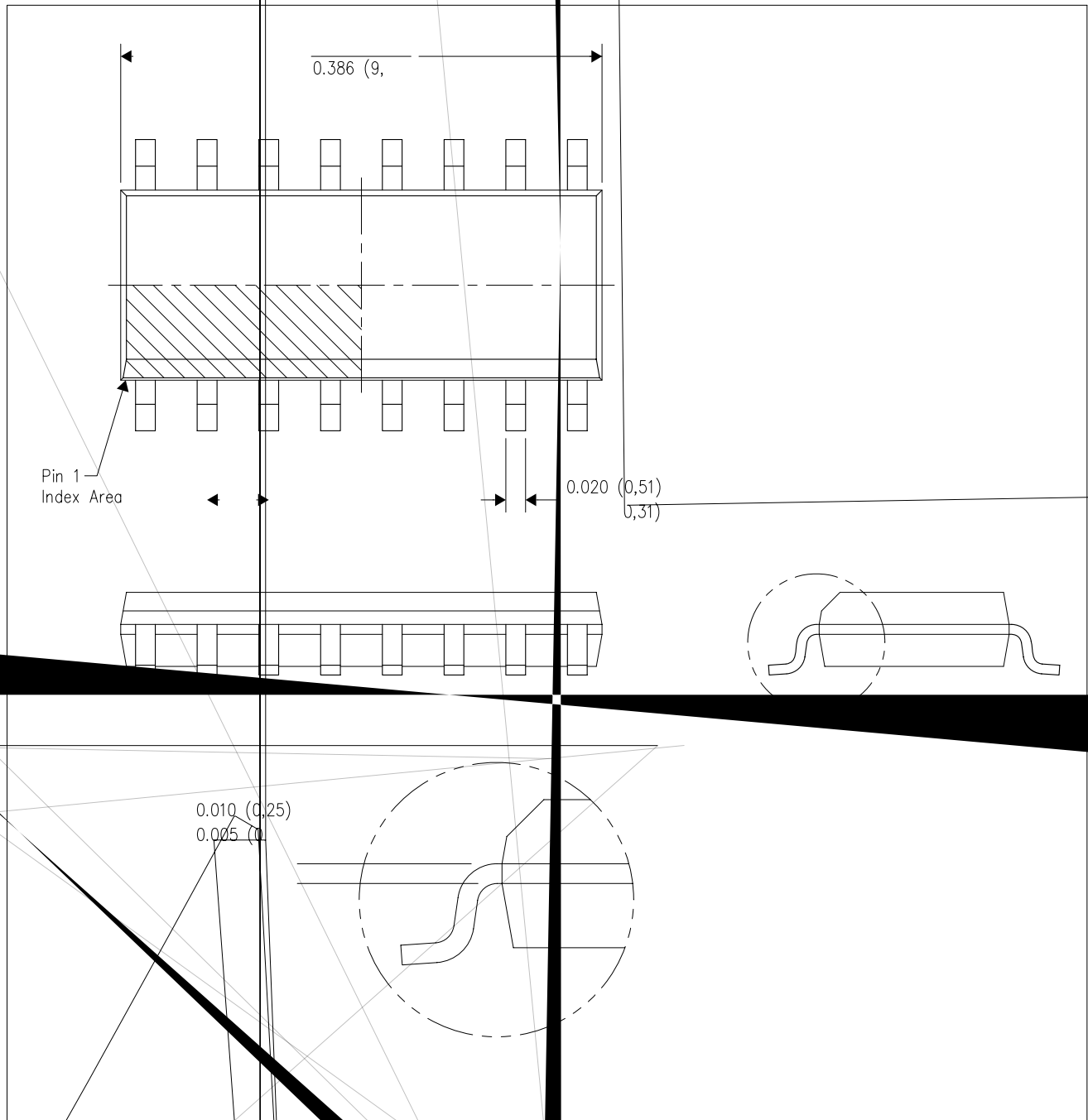
\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| BQ2011SN-D118TR | SOIC         | D               | 16   | 2500 | 367.0       | 367.0      | 38.0        |

# MECHANICAL DATA

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).  
B. This drawing is subject to change without notice.

not inclu

ce interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

- D. Laser cutting apertures with trapezoidal walls and also round l  
contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
- . Customers sh



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