AN-400A

Low-Power Green-Mode PWM Flyback Power Controller without Secondary Feedback

Abstract

This highly integrated PWM controller, FAN400A, offers several features to enhance the performance of a flyback converter for low-power applications. Using the controller reduces the costs of battery chargers and AC adapters. The no-load power consumption can be less than 200mW for universal AC input voltage range to meet the power conservation requirements.

Features

- Linearly Decreasing PWM Frequency
- Green Mode Under Light-load and Zero-load Conditions
- Constant Voltage (CV) and Constant Current (CC)
- No Secondary Feedback
- Low Startup Current: 8µA
- Low Operating Current: 3.6mA
- Leading-edge Blanking
- Constant Power Limit
- Universal AC Input Range
- Synchronized Slope Compensation
- 140°C OTP Sensor with Hysteresis
- V_{DD} Over-Voltage Clamping
- Cycle-by-cycle Current Limiting
- Under voltage lockout (UVLO)
- Fixed PWM Frequency with Hopping
- Gate Output Maximum Voltage Clamped at 17V
- Small SOT-26 Package

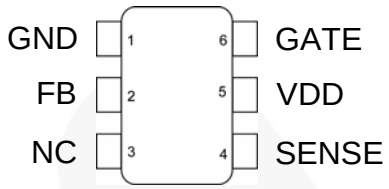

Figure 1. SOT-26 Pin Configuration

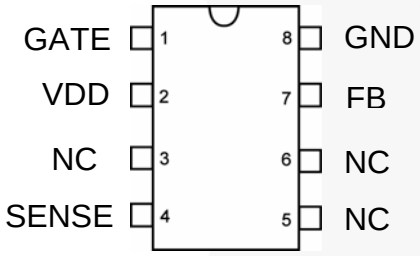

Figure 2. DIP-8 Pin Configuration

Application Diagram

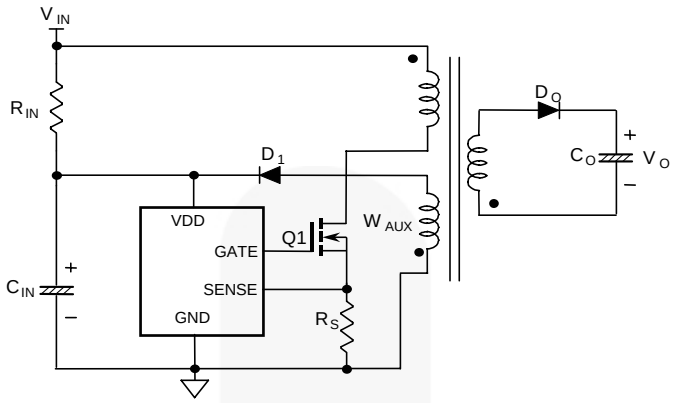

Figure 3. Typical Application

Internal Block Diagram

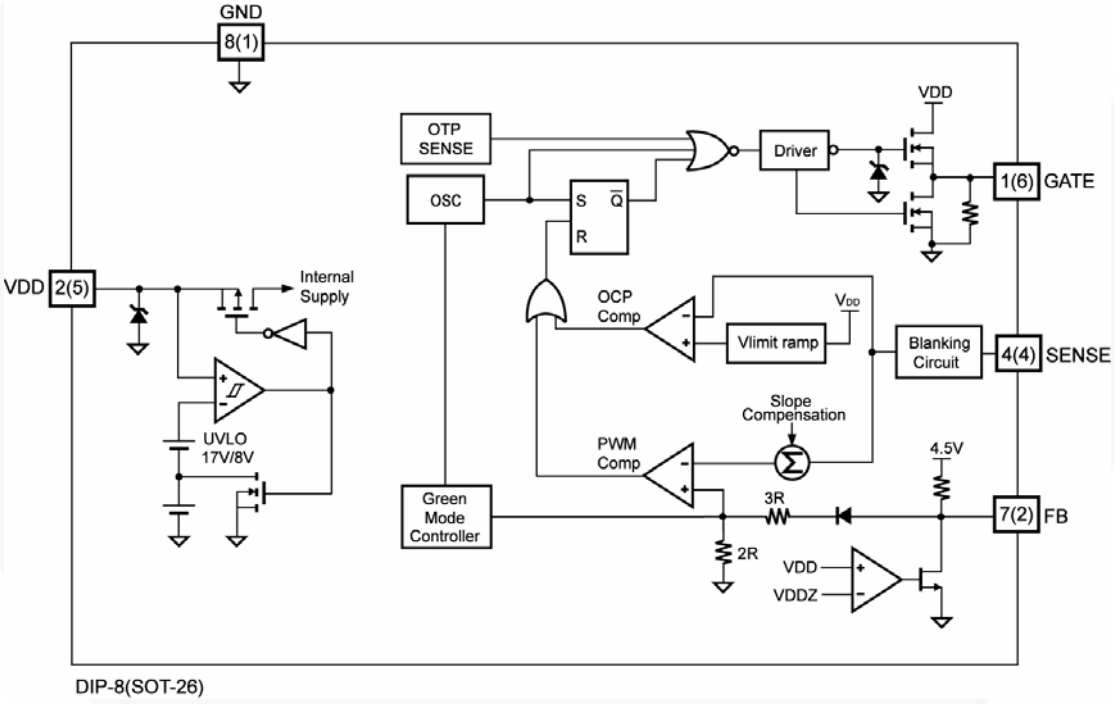

Figure 4. Functional Block Diagram

Start-up Circuitry

When the power is turned on, the input rectified voltage V_{DC} charges the hold-up capacitor C1 via a startup resistor R_{IN}. As the voltage of the VDD pin reaches the start threshold voltage V_{DD-ON}, the FAN400A activates and drives the entire power supply.

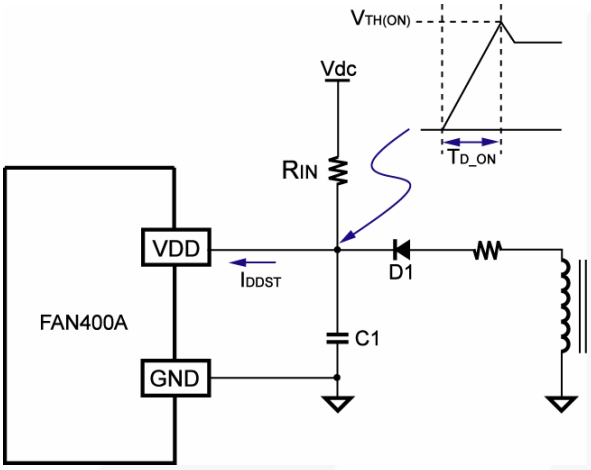

Figure 5. Circuit Providing Power to FAN400A

The maximum power-on delay time is determined as:

$$V_{DD\text{-}ON} = (V_{DC} - I_{DD-ST} \cdot R_{IN}) \left[1 - e^{-\frac{t_{D\_ON}}{R_{IN} \cdot C1}} \right] \quad (1)$$

where I_{DD_ST} is the startup current of FAN400A and t_{D_ON} is the power-on delay time of the power supply.

Due to the low startup current, a large R_{IN}, such as 1.5MΩ, can be used. With a hold-up capacitor of 10μF/50V, the power-on delay t_{D_ON} is less than 2.8s for 90V_{AC} input.

Constant Voltage (CV) Operation

The FAN400A can regulate the output voltage without secondary-side feedback signal. As shown in Figure 6, an internal V_{DD} feedback comparator ($V_{DD\text{-}comp}$) is used to modulate the PWM output pulses when the FB pin is floating. The primary V_{DD} voltage is maintained at 22.7V due to internal feedback compensation circuit. The output voltage is proportional to V_{DD} according to the ratio between transformer auxiliary winding and secondary winding. A typical output characteristic using FAN400A is shown in Figure 7. If more precise output voltage regulation is required, secondary feedback circuitry should be used.

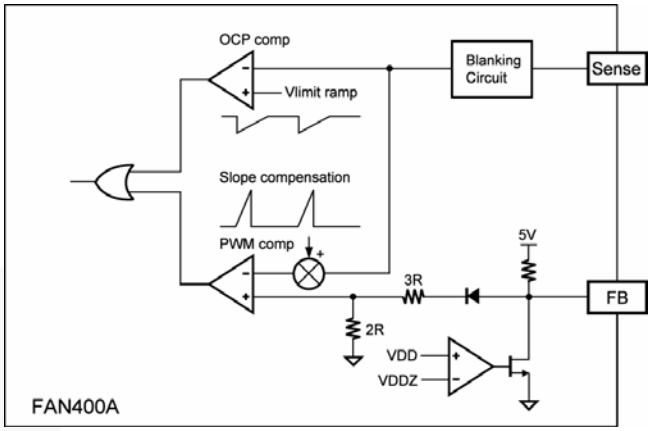

Figure 6. Voltage Regulated by V_{DD} Feedback

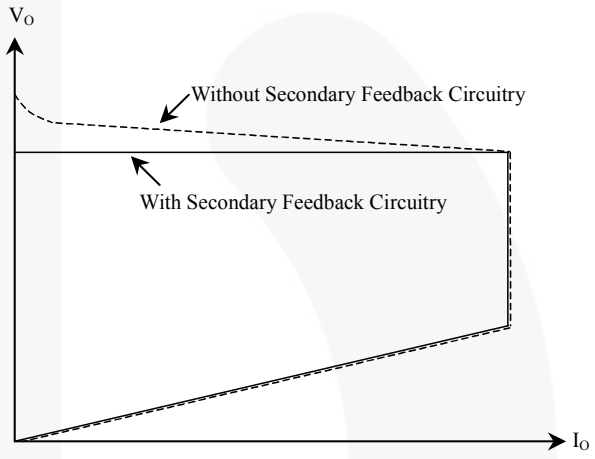

Figure 7. Output Characteristics with and without Secondary Feedback Circuitry

A typical secondary feedback circuit mainly consisting of a shunt regulator and an opto-coupler is shown in Figure 8. R1 and R2 form a voltage divider for the output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47Ω, C_{FB}=1nF) placed from FB pin to GND can increase stability. The maximum sourcing current of the FB pin is 1.4mA. The phototransistor must be capable of sinking this current to pull FB level down at no load. The value of biasing resistor R_B is determined as follows:

$$\frac{V_O - V_D - V_Z}{R_B} \cdot K \geq 1.4mA \quad (2)$$

where:
V_D is the drop voltage of photodiode, about 1.2V;

V_Z is the minimum operating voltage of the shunt regulator (typically 2.5V), and;

K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_O=5V, with CTR=100%, the maximum value of R_B is around 910Ω.

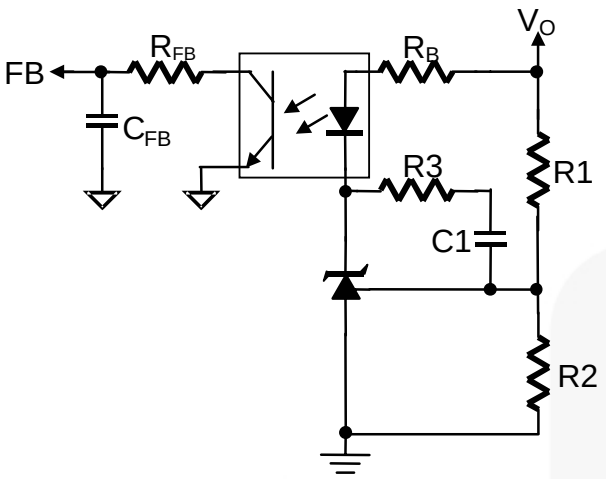

Figure 8. Feedback Circuit

Using secondary feedback circuitry, the primary V_{DD} voltage should be maintained lower than 20V. Otherwise, the internal V_{DD} feedback circuitry may activate with heavy output loading. The transformer auxiliary turn number should be reduced compared with primary feedback application. When the secondary feedback circuitry is open loop, the primary feedback circuitry acts as a back-up protection to prevent the V_{DD} exceeding 22.7V.

Constant Current (CC) Operation

For a discontinuous-current mode flyback converter in constant current operation, the output power is proportional to the square of the peak primary current, and to the output voltage. When the output voltage reduces to half, the primary current drops to 0.707 times the original.

Inside the FAN400A, the V_{DD} voltage is used to modulate the level of the saw current limiting threshold voltage. As shown in Figure 9, the valley voltage of the saw current limiting curve reduces to 0.707 times of the original when the V_{DD} voltage reduces to half. With a good coupling of the transformer, the ratio of the V_{DD} voltage to the output voltage is almost constant. A constant current operation is therefore achieved.

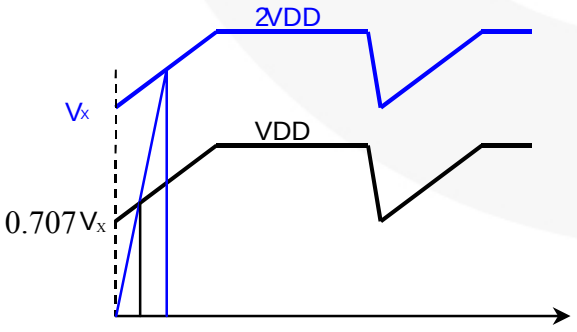

Figure 9. Voltage Controlled SAW Current Limiting Curves

Oscillator & Green Mode Operation

The proprietary green-mode function provides off-time modulation to reduce the PWM frequency at light-load and in no-load conditions. The feedback voltage of the FB pin is taken as a reference. When the feedback voltage is lower than about 2.6V, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the PWM frequency, the off-time modulation reduces the power consumption of the power supply at light-load and no-load conditions. The PWM frequency is 65KHz at nominal load and decreases to 17KHz at light load. The power supply enters "adaptive off-time modulation" in zero-load conditions.

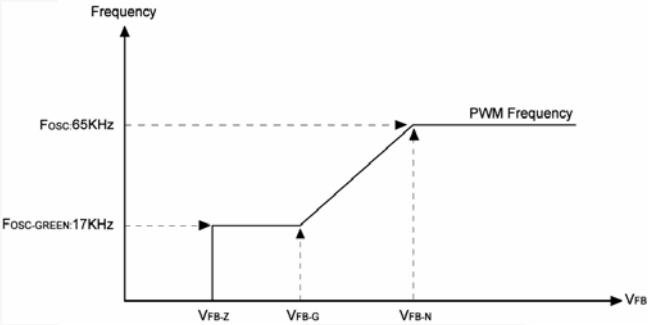

Figure 10.PWM Frequency vs. FB Voltage

Built-in Slope Compensation

A flyback converter can be operated in either discontinuous current mode (DCM) or continuous current mode (CCM). There are many advantages to operating in CCM. With the same output power, a converter in CCM exhibits smaller peak inductor current than in DCM. Therefore, a small-sized transformer and a low-rating MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice that of CCM. Larger wire gauge and output capacitors with larger ripple current rating are required. DCM operation also results in a higher output voltage spike. A large LC filter has to be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern – stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current is controlled. This causes the well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. FAN400A introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. The sensed voltage, plus this slope compensation signal (V_{SLOPE}), is fed into the non-inverting input of the PWM comparator. The resulting voltage is compared with the FB signal to adjust the PWM duty cycle such that the output voltage is regulated. Therefore, FAN400A allows design of cost effective, highly efficient, and compact-sized

flyback power supplies operating in CCM without adding external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \bullet D \quad (3)$$

where V_{SL} = 0.33V and D = duty cycle.

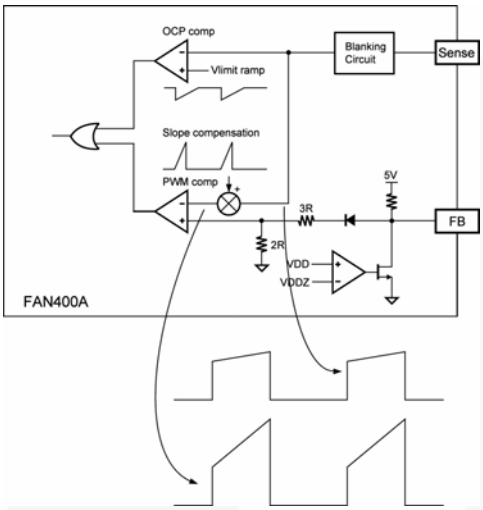

Figure 11.Synchronized Slope Compensation

Over-Temperature Protection (OTP)

A built-in temperature sensing circuit shuts down PWM output once the junction temperature exceeds 140°C. While PWM output is shuts down, the V_{DD} voltage gradually drops to the UVLO voltage (around 8V). Then V_{DD} is charged up to the startup threshold voltage of 17V through the start up resistor until PWM output is restarted. This "hiccup" mode protection occurs repeatedly as long as the temperature remains above 110°C. The temperature hysteresis window for the OTP circuit is 30°C.

Constant Output Power Limit

The maximum output power of a flyback converter can be generally designed by the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. When the output current arrives at the protection value, the OCP comparator dominates the current control loop. OCP occurs when the current-sense voltage reaches the threshold value. The output GATE driver is turned off after a small propagation delay, t_D. The delay time results in unequal power-limit level under universal input. In FAN400A, a sawtooth power-limiter is designed to solve the unequal power-limit problem. As shown in Figure 12, the power limiter is designed as a positive ramp signal fed to the non-inverting input of OCP comparator. This results in a lower current limit at high-line input than at low-line. However, with fixed propagation delay t_D, the peak primary current would be the same for various line input voltage. Therefore, the maximum output power can almost be limited to a constant value within a wide input voltage range without adding external circuits.

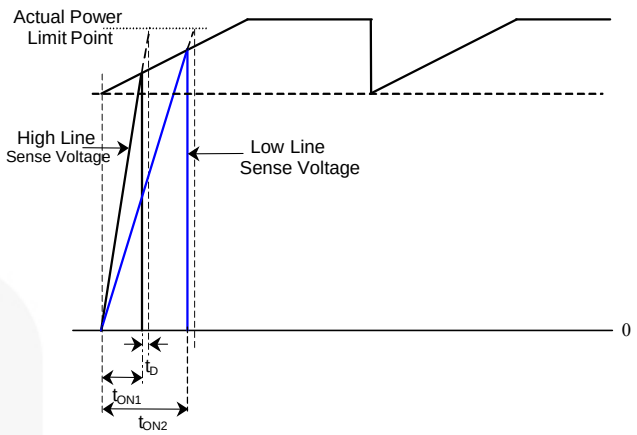

Figure 12.Constant Power Limit Compensation

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET turns on, a spike induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, appears on the sensed signal. A leading-edge blanking time about 310ns is introduced to avoid premature termination of MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω + 47pF) is required between the SENSE pin and R_S. A non-inductive resistor for the R_S is recommended.

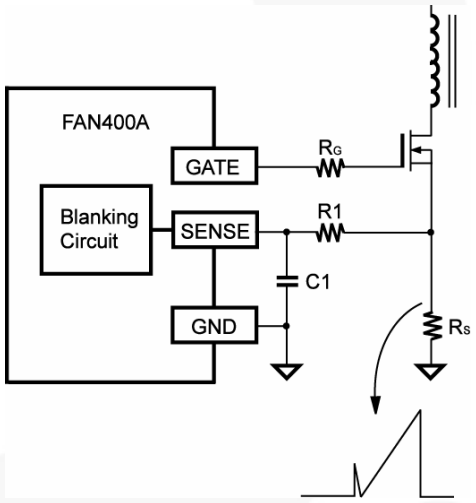

Figure 13.Turn-on Spike

Gate Drive

FAN400A's output stage is a fast totem-pole driver that can directly drive MOSFET gate. It is equipped with a voltage clamping Zener diode to protect MOSFET from damage caused by undesirable over-drive voltage. The output voltage is clamped at 17V. An internal pull-down resistor is used to avoid floating state of gate before startup. A gate drive resistor in the range of 47 to 100Ω is recommended to limit the peak gate drive current and provide damping to prevent oscillations at the MOSFET gate terminal.

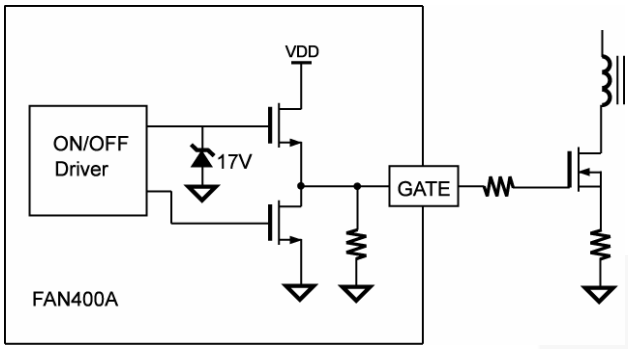

Figure 14.Gate Drive

Lab Note

Before rework or solder/desolder on the power supply, discharge primary capacitors by external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during solder/desolder.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board Layout

High-frequency switching current / voltage make printed circuit board layout a very important design issue. Good PCB layout minimizes excessive EMI helps the power supply survive during surge/ESD tests.

Guidelines:

To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.

- The high frequency current loop is in C1 – Transformer – MOSFET – R_S – C1. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage traces related the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If heatsink is used for MOSFET, connect this heatsink to ground.
- As indicated by 3, the ground of control circuits should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by transformer auxiliary winding, D1, and C2 should also be kept small. Place C2 close to FAN400A for good decoupling.

Two suggestions with different pro and cons for ground connections are recommended.

- GND3→2→4→1: This could avoid common impedance interference for the sense signal.
- GND3→2→1→4: This could be better for ESD tests where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary, through the transformer stray capacitance, to GND2 first. Then the charges go from GND2 to GND1 and back to mains. It should be noted that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the positive terminal of C1 (V_{DC}). If this Y-cap is connected to primary GND, it should be connected to the negative terminal of C1 (GND1) directly. Point discharge of this Y-cap also helps for ESD. However, the creepage between these two pointed ends should be at least 5mm according to safety requirements.

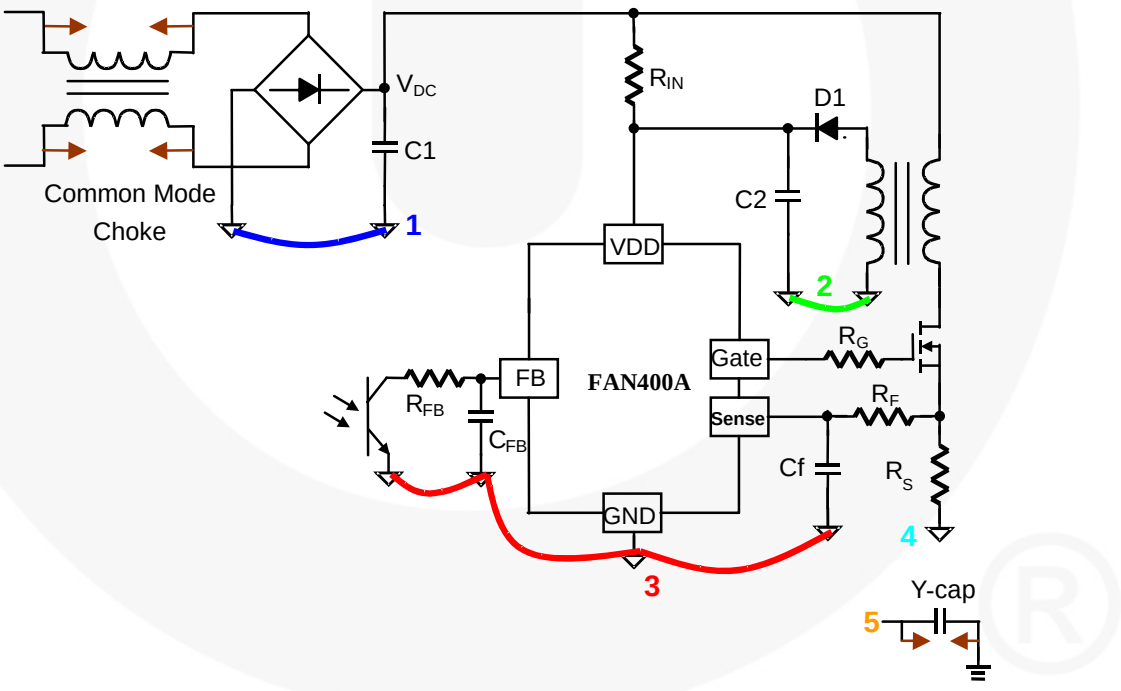

Figure 15. Layout Considerations