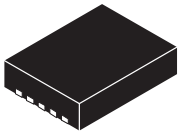

Li-Ion AND Li-Pol BATTERY GAS GAUGE IC FOR PORTABLE APPLICATIONS (bqJUNIOR)

FEATURES

- **HDQ (bq27010) or I²C (bq27210) Communication**
- **Reports Accurate *Time-to-Empty* At Both Measured and Host-Requested Load Values**
- **Reports Available Capacity Compensated for Discharge Rate, Temperature, and Age**
- **End-of-Discharge Voltage Compensated for Discharge Rate and Temperature**
- **Automatic Capacity Reduction with Age**
- **Reports Temperature, Voltage, and Current**
- **High Accuracy Charge and Discharge Current Integration with Automatic Offset Calibration**
- **Requires No User Calibration**
- **Programmable Input/Output Port**
- **Internal User EEPROM Configuration Memory**
- **Uploadable Coefficients Allows Host-Side Use with Multiple Pack Characteristics**
- **Stable Oscillator Without External Components**
- **Dynamic End-of-Discharge Detection Delay to Allow Use in a High-Dynamic Load Environment**
- **Automatic Sleep Mode When Communication Lines are Low**
- **Available in a Small 3 mm x 4 mm QFN Package**
- **Five Low-Power Operating Modes**
  - **Active: < 90 µA**
  - **Sleep: < 2.5 µA**
  - **Ship: < 2 µA (bq27010 only)**
  - **Hibernate: < 1.5 µA**
  - **Data Retention: < 20 nA**

APPLICATIONS

- **PDA**
- **Smart Phones**
- **MP3 Players**
- **Digital Cameras**
- **Internet Appliances**
- **Handheld Devices**

DESCRIPTION

The bqJUNIOR™ series are highly accurate stand-alone single-cell Li-Ion and Li-Pol battery capacity monitoring and reporting devices targeted at space-limited, portable applications. The IC monitors a voltage drop across a small current sense resistor connected in series with the battery to determine charge and discharge activity of the battery. Compensations for battery age, temperature, self-discharge, and discharge rate are applied to the capacity measurments to provide available time-to-empty information across a wide range of operating conditions. Battery capacity is automatically recalibrated, or learned, in the course of a discharge cycle from full to empty. Internal registers include current, capacity, time-to-empty, state-of-charge, cell temperature and voltage, status, and more.

The bqJUNIOR can operate directly from single-cell Li-Ion and Li-Pol batteries and communicates to the system over a HDQ one-wire or I²C serial interface.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

bqJUNIOR is a trademark of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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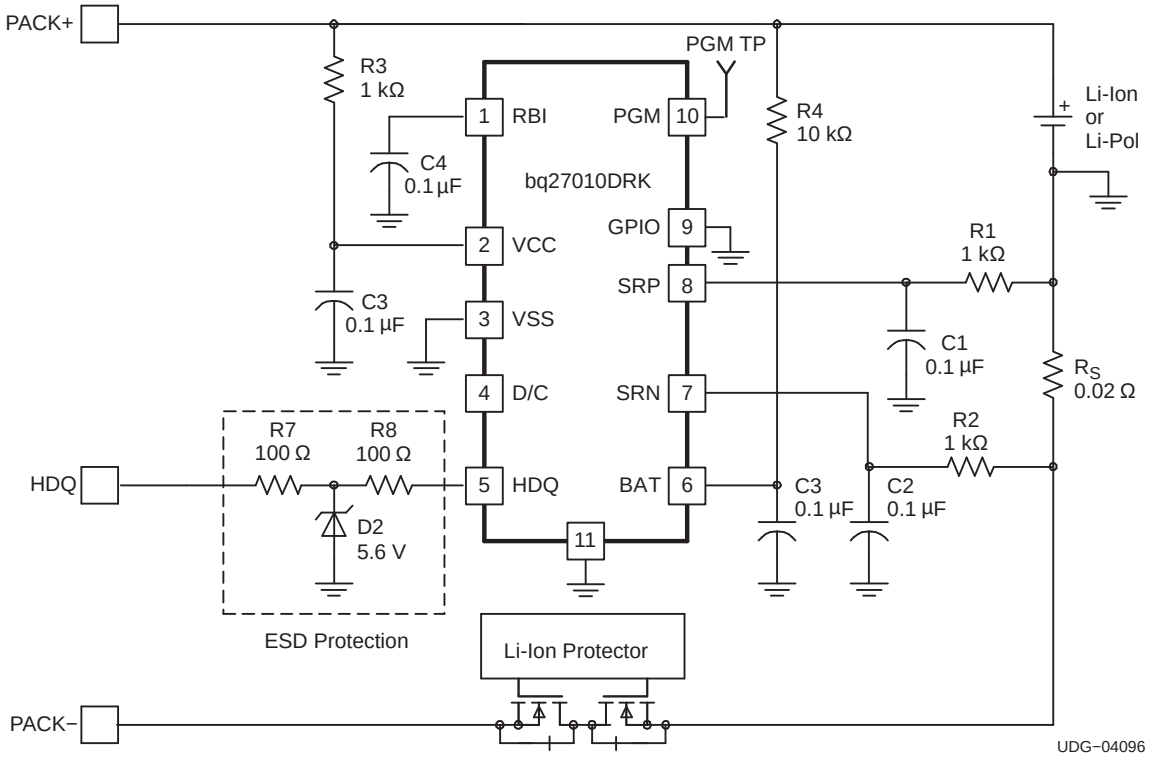
TYPICAL APPLICATION



ORDERING INFORMATION

TA	COMMUNICATION INTERFACE	PACKAGED DEVICES(1)	MARKINGS
-20°C to 70°C	HDQ	bq27010DRKR	27010
	I^2C	bq27210DRKR	27210

(1) The DRK package is available taped and reeled only. Quantities are 2,000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)

			bq27010 bq27210	UNITS
V_{CC}	Supply voltage	(with respect to V_{SS})	–0.3 to 7	V
V_{IN}	Input voltage	SRP, SRN, RBI, BAT (all with respect to V_{SS})	–0.3 to V_{CC}+0.3	
		HDQ, SCL, SDA, GPIO (all with respect to V_{SS})	–0.3 to 7	
		PGM (with respect to V_{SS}) during EEPROM programming	–0.3 to 22	
I_{SINK}	Output sink current	GPIO, SCL, SDA, HDQ	5	mA
T_A	Operating free-air temperature range		–20 to 70	°C
T_{stg}	Storage temperature range		–65 to 150	
T_J	Operating junction temperature range		–40 to 125	
	Lead temperature (soldering, 10 sec)		300	

ONDITIONS

S

TIMING DIAGRAMS

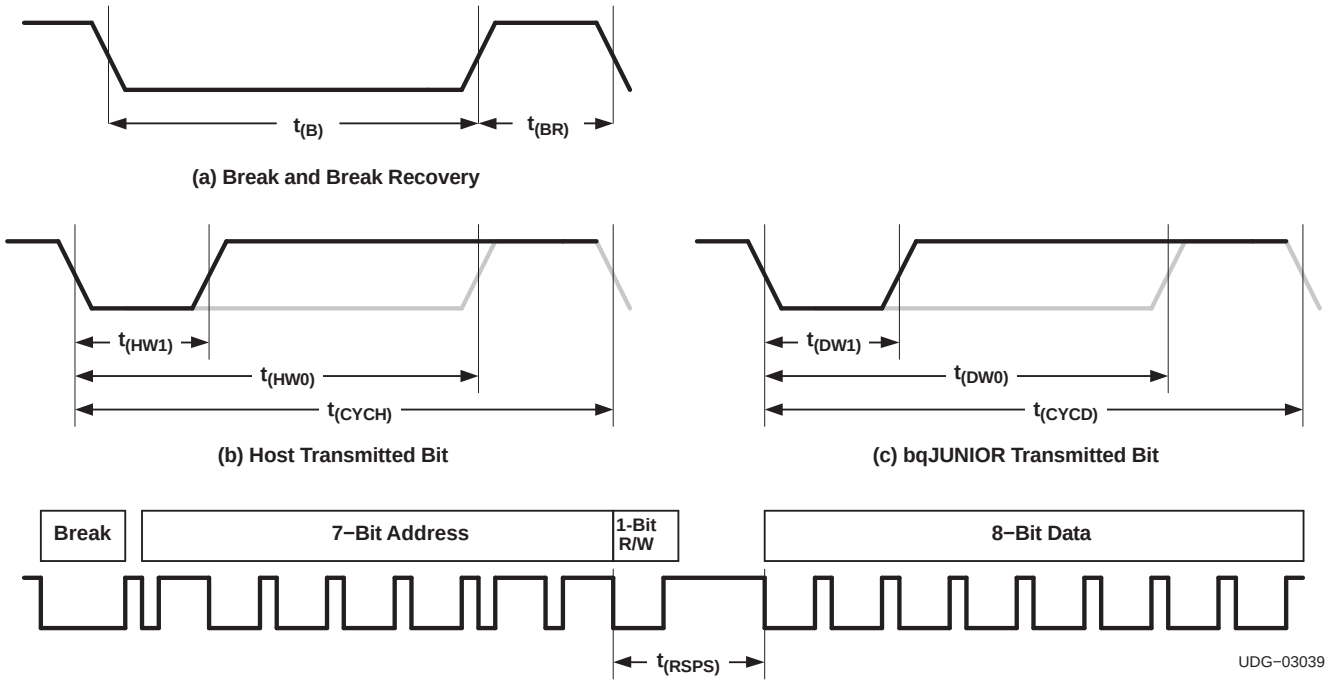


Figure 1. HDQ Bit Timing Diagram

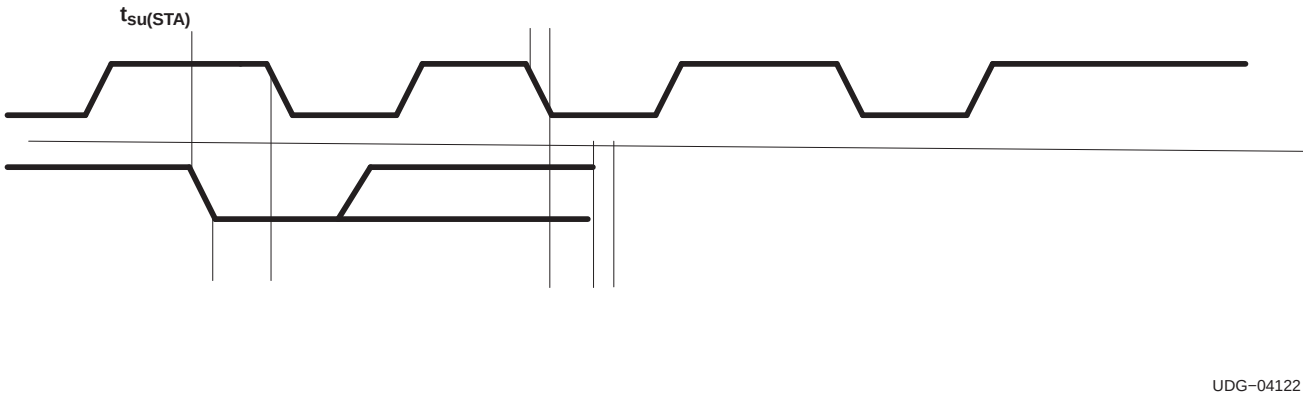
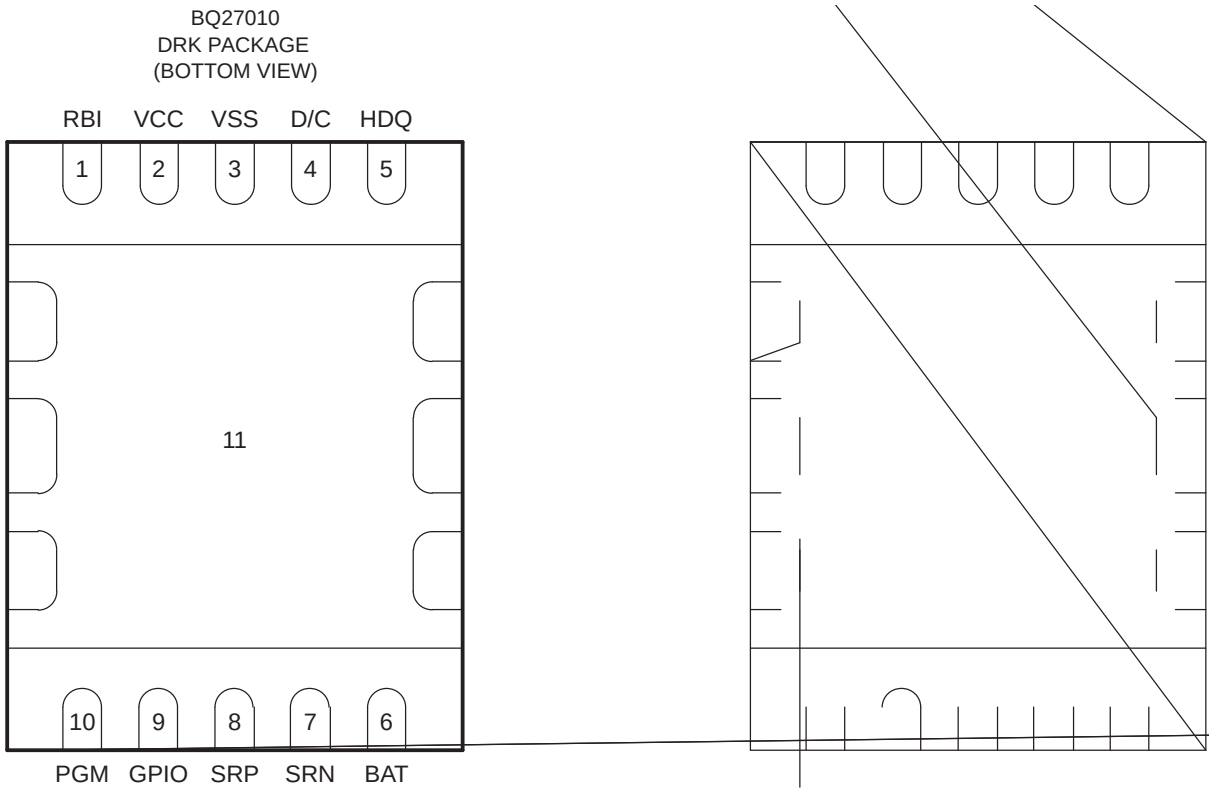


Figure 2. I^2C Timing Diagram

TIMING DIAGRAMS (continued)

BQ27010
DRK PACKAGE
(BOTTOM VIEW)

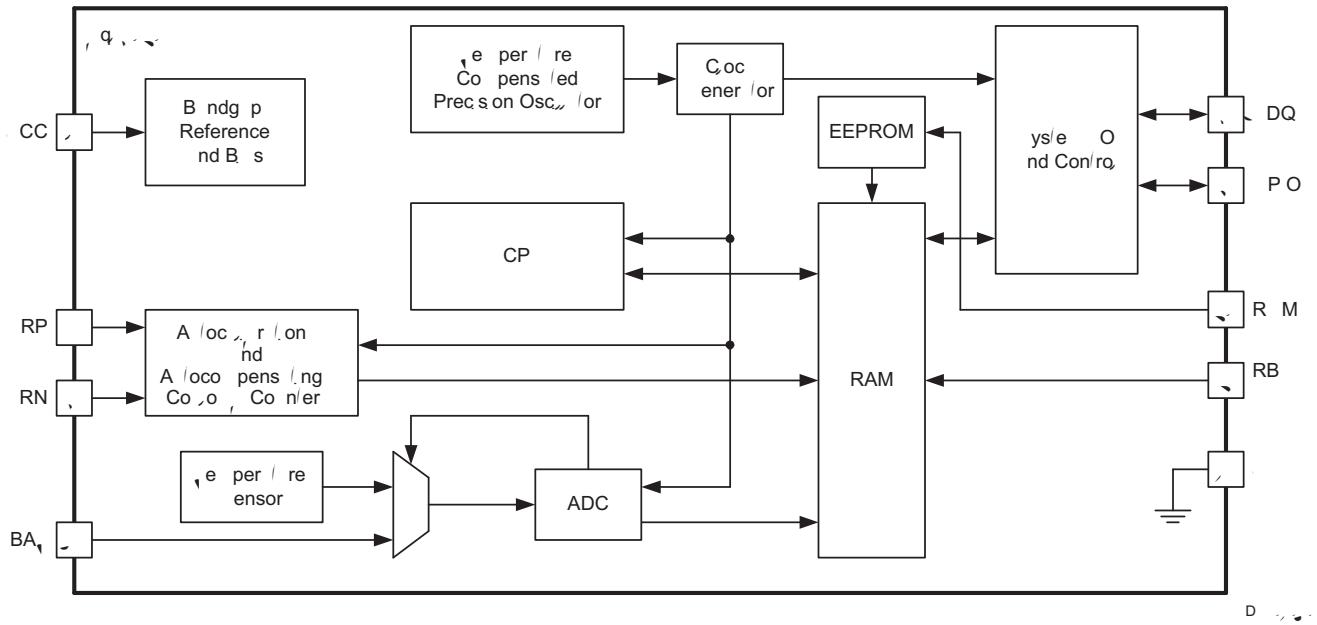


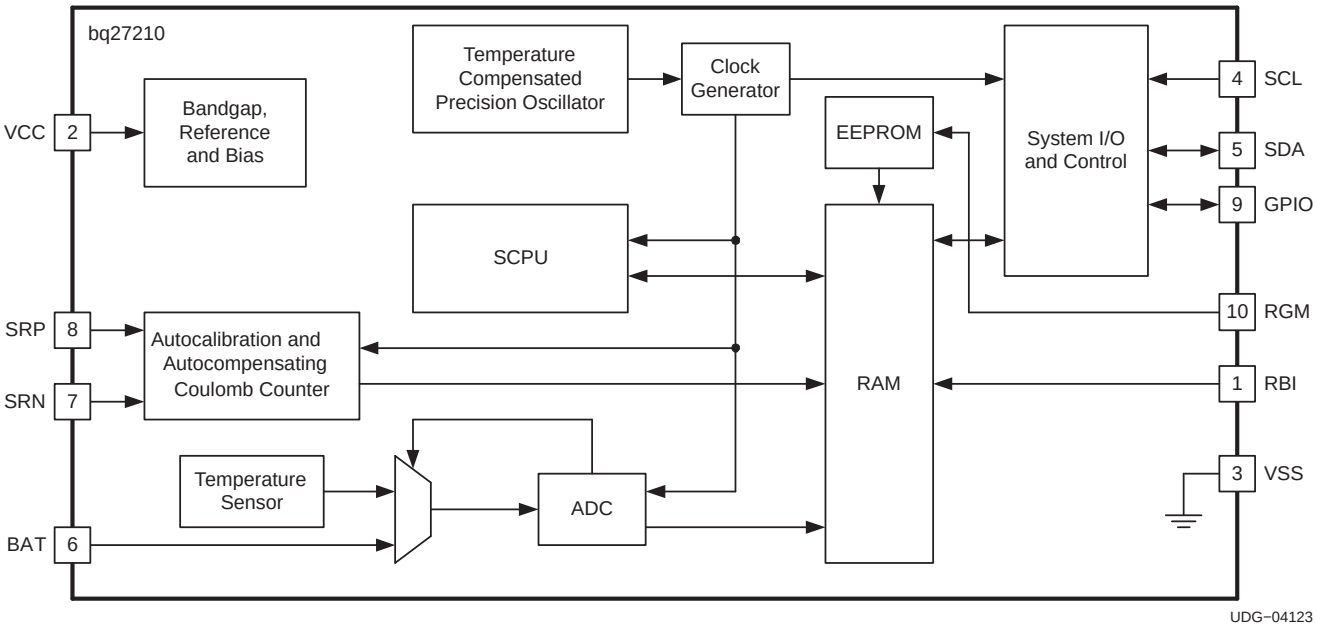
DEVICE INFORMATION

TERMINAL FUNCTIONS

TERMINAL			I/O	DESCRIPTION
NAME	bq27010	bq27210 (Preview)		
BAT	6	6	I	Battery voltage sense input
D/C	4	-	-	Do

FUNCTIONAL BLOCK DIAGRAMS



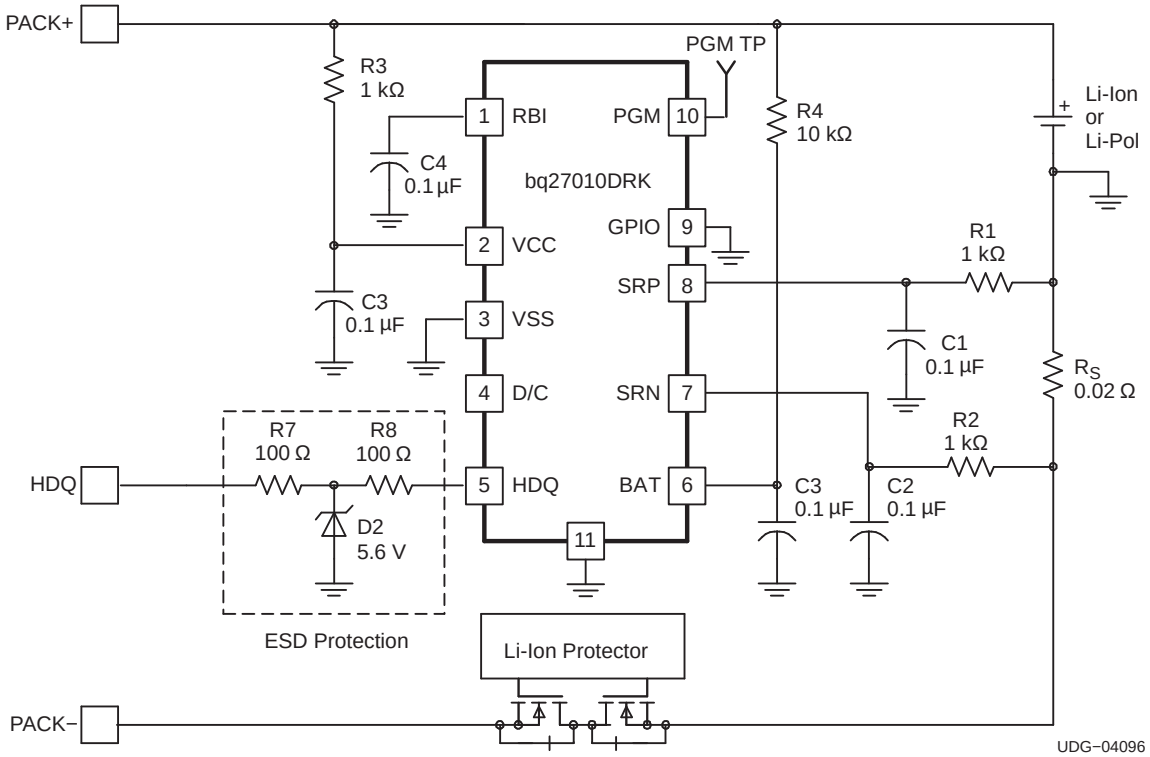


FUNCTIONAL DESCRIPTION

The bqJUNIOR determines battery capacity by monitoring the amount of charge input to or removed from a Li-Ion or Li-Pol battery. The bqJUNIOR measures discharge and charge currents, monitors the battery for low voltage thresholds, and compensates for self-discharge, aging, temperature, and discharge rate. Current is measured across a small value series resistor between the negative terminal of the battery and the pack ground (see R_S in Figure 3). Available capacity is reported with a resolution of 3.57 µVh. Time-To-Empty reporting in minutes at standby, actual, and at-rate currents allows the requirements for host-based calculations to be greatly reduced or eliminated; reading a single register pair provides useful and meaningful information to the end user of the application.

FUNCTIONAL DESCRIPTION (continued)

Figure 3 shows a typical application circuit. Differential sense of the voltage across the current sense resistor, R_S, improves device performance, leading to an improvement in reported time-to-empty accuracy. An internal 3-µA pull-down on the HDQ or SDA and SCL lines ensures that the device detects a logic *0* on the communication lines and allows the device to automatically enter the low-power sleep mode when the system power is switched off or the pack is removed. A 100 kΩ pullup to V_{CC} can be added to the communication lines if this feature needs to be disabled. The bqJUNIOR can operate directly from a single



Measurements

Charge and Discharge Coulometric and Current Measurements

Offset Calibration

Digital Magnitude Filter

Voltage

Temperature

RBI

FUNCTIONAL DESCRIPTION (continued)

Register Initialization and Data Integrity Checks

Checksums of critical internal register data are continually checked during operation of the bqJUNIOR. A failed checksum comparison will force a hardware reset. After a reset, the bqJUNIOR examines a checksum containing LMD, CYCL, CYCT, and other critical data. If the checksum is incorrect, NAC, CYCL, and CYCT are cleared, LMD and other parameters are initialized from EEPROM, the CI bit in FLAGS is set, and the INIT bit in MODE is set. This process constitutes a full reset. If the checksum is correct, NAC, LMD, CYCL, and CYCT are retained. In addition, a second checksum containing all user-updateable EEPROM coefficients is checked. If the second checksum is incorrect, the values are all initialized from the EEPROM, the CI bit in FLAGS is set, and the INIT bit in MODE is set. The INIT bit is used to inform the host that it may need to reinitialize these values if the default values are not satisfactory. If the second checksum is correct, the INIT bit in MODE will not be set, the CI bit in FLAGS will remain unchanged, and the register data that may have been updated by the host will be retained. This process constitutes a partial reset. It is the host responsibility to clear the INIT bit in MODE after any updates by the host are completed. See CTRL description for more on host updates. Other register values not specifically retained are reinitialized on all resets.

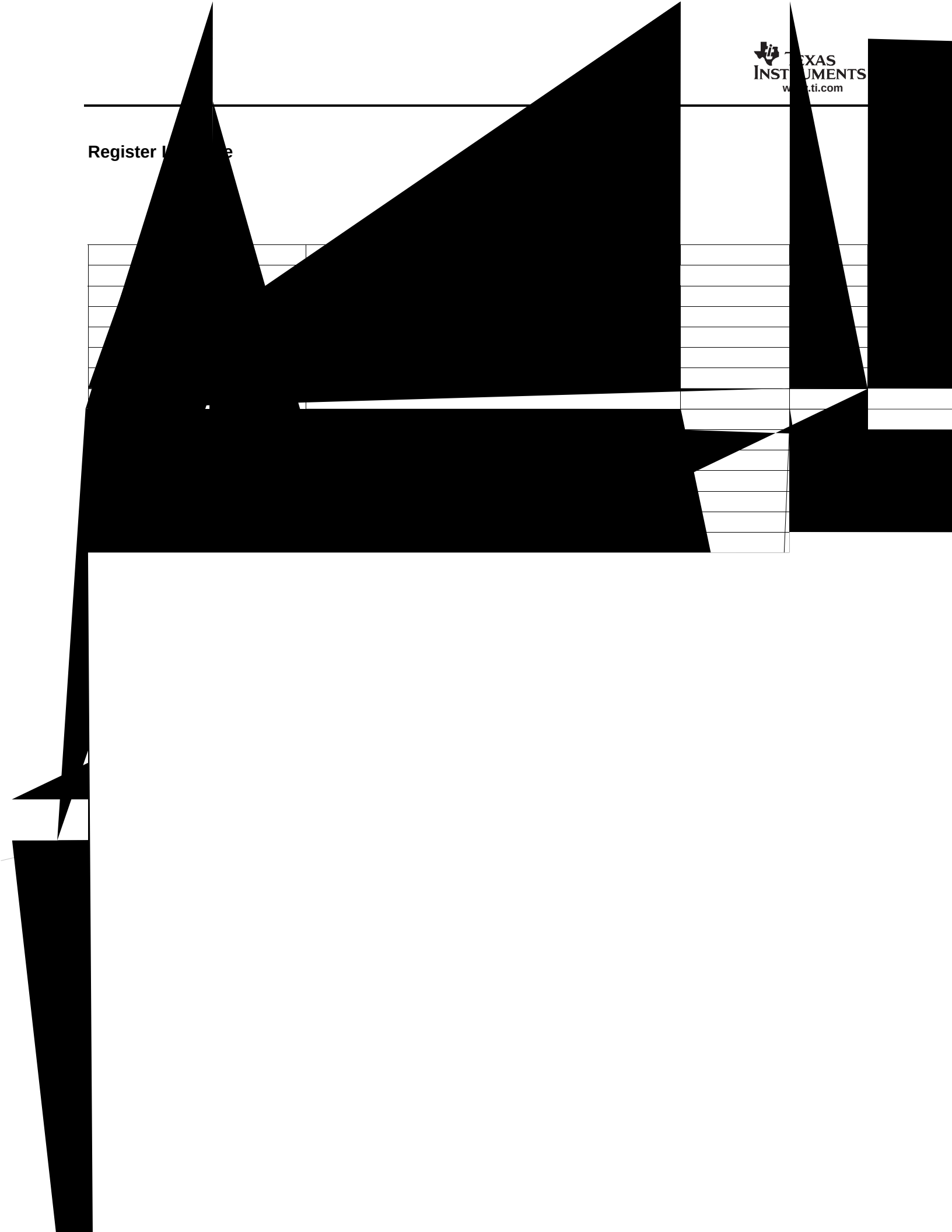
GPIO

The GPIO pin can be used as an input or an

Layout Considerations

Gas Gauge Operation

Register M[illegible]e



APPLICATION INFORMATION

Control and MODE Registers (CTRL/MODE) — Address 0x00/0x01

The device control register is used by the host system to request special operations by the bqJUNIOR. The highest priority command set in the MODE register is performed when the host writes data 0xA9, 0x56, or 0xC5 as indicated to the control register. The CTRL register and MODE bits 5, 4, 3, 1, and 0 are cleared when the command is accepted. The host must set the appropriate command bit in MODE before sending the command key to CTRL.

Mode Register (MODE) — Address 0x01

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
COMMAND KEY = 0xA9	GPIEN	GPSTAT	WRTNAC	DONE	PRST	INIT	FRST	SHIP(1)
COMMAND KEY = 0x56	GPIEN	GPSTAT	CEO	CIO	WNACCI	INIT	WRTCYC	WRTLMD
COMMAND KEY = 0xC5	GPIEN	GPSTAT	UPDC	UPEDVI	UPDMF	INIT	UPCFG	UPCOMP

(1) bq27010 only

GPIEN GPIEN sets the state of the GPIO pin. A *1* configures the GPIO pin as input, while a *0* configures the GPIO pin as an open-drain output. This bit is initialized to the value of bit 7 of the PKCFG register in the EEPROM. The user should keep this bit set or cleared as desired when other bits in this register are written.

GPSTAT GPSTAT sets the state of the open drain output of the GPIO pin (GPIEN = 0). A *1* turns off the open drain output, while a *0* turns the output on. This bit is set to *1* on POR. When the GPIO pin is an input (GPIEN=1), this bit returns the logic state of the GPIO pin. The user should keep this bit set or cleared as desired when other bits in this register are written.

WRTNAC WRTNAC is used to transfer data from the AR registers to NAC. Other registers are updated as appropriate. This command is useful during the pack manufacture and test to initialize the gauge to match the estimated battery capacity.

DONE DONE is used to write NAC equal to LMD. Useful if the host uses a charge termination method that does not allow the monitor to detect the taper current. The host system could use this command when the charging is complete to force update of internal registers to a full battery condition.

PRST Partial reset. This command requests a reset of all RAM registers except NAC, LMD, and the CI bit in FLAGS. This command is intended for manufacturing use.

INIT The INIT status bit is set to *1* by the bqJUNIOR if there is a full reset or if data corruption is detected in the internal memory containing EEPROM coefficients. Either of these events will cause the bqJUNIOR to update internal memory values. If NAC, LMD, CYCT, or EEPROM-initialized coefficients need to be modified from their original values, the host should first update the values and then clear the INIT bit. The INIT bit is not cleared by the bqJUNIOR.

FRST Full reset. This command bit requests a full reset. A full reset reinitializes all RAM registers, including the NAC, LMD, and FLAGS registers. This command is intended for manufacturing use.

SHIP This command bit requests that the device (bq27010 only) should be put in ship mode. See the *Power Mode* section for a description of the ship mode. This command is intended for manufacturing use.

CEO This command bit requests that the external offset value is measured. Care should be taken to insure that no charge or discharge current flows during the time this measurement is made. The external offset value is the total offset of the DSCC plus any external PCB affects. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use. The CIO offset value may be subtracted from the CEO offset value to determine the external board offset. This value can be programmed into PKCFG[4:2] in the EEPROM for automatic compensation of this external offset value.

CIO This command bit requests that the internal offset value is measured. The internal offset value is

the offset of the DSCC with an internal short applied from SRP to SRN. The result can be read in 0x5f-5e. The result is a signed number with an LSB value of 1.225 µV. The command takes approximately 5.5 seconds to make the measurement. This command is intended for manufacturing use, along with the CEO command, to determine the external board offset..

WNACCI WNACCI is used to transfer data from the AR registers to NAC. It is identical to the WRTNAC command, but the CI bit in FLAGS is also cleared

The following commands are intended for use by a host-side gauge if the battery pack is changed and the host can determine that the new pack requires different values loaded into the gauge. They can also be used with a pack-side gauge if the default EEPROM values in the bqJUNIOR do not match the required values. If the host only desires to change one of the bytes, the value for the unchanging byte will still have to be read and placed in the appropriate AR byte, as both bytes will be updated when the command is issued. The EEPROM values used by the bq27x010 firmware are located in addresses 0x46 to 0x4F. These addresses are a mirror of the EEPROM values programmed in addresses 0x76 to 0x7F after a full reset, unless DCOMP and/or TCOMP default values are selected by PKCFG[1:0]. Update commands for the EEPROM coefficients will update the appropriate value in the 0x46 to 0x4F address space, but will not affect the value in the 0x76 to 0x7F addresses.

WRTCYC WRTCYC is used to transfer data from the AR registers to CYCT.

WRTLMD WRTLMD is used to transfer data from the AR registers to LMD.

UPDC UPDC is used to simultaneously update the ILMD value (DC) from the ARL register and to update the EDVF value from the ARH register.

UPEDV1 UPEDV1 is used to simultaneously update the EDV1 value from the ARL register and to update the ISLC/EDVT value from the ARH register.

UPDMF UPDMF is used to simultaneously update the DMFSD value from the ARL register and to update the TAPER value from the ARH register.

UPCFG UPCFG is used to simultaneously update the PKCFG value from the ARL register and to update the GAF/DEDV value from the ARH register.

UPCOMP UPCOMP is used to simultaneously update the DCOMP value from the ARL register and to update the TCOMP value from the ARH register.

At-Rate Registers (ARL/ARH) — Address 0x02/0x03

The host can write the current in units of 3.57 µV per bit to this register for predictive calculation time-to-empty. The part uses this value to predict the time-to-empty at any desired current; it does not affect the time-to-empty calculation based on the actual current. The value in AR is always assumed to be a discharge current.

This register is also used during pack manufacturing to input a nominal available-charge value to set NAC to the approximate initial pack capacity value, and to update other values as described in the CTRL register description.

At Rate Time-to-Empty Registers (ARTTEL/ARTTEH) — Address 0x04/0x05

This is predicted time-to-empty in minutes at user-entered discharge rate. The discharge current used in the

Reported Temperature Registers (TEMPL/TEMPH) — Address 0x06/0x07

Reported Battery Voltage Registers (VOLTL/VOLTH) — Address 0x08/0x09

The VOLTH and the VOLTL low-byte registers contain the reported battery voltage measured on the BAT pin. Voltage is expressed in mV with an LSB resolution of 1 mV. Reported voltage cannot exceed 5000 mV. The host system has read-only access to this register pair. Voltage is updated every 2.56 seconds.

Status Flag Register (FLAGS) — Address 0x0A

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	CHGS	NOACT	IMIN	CI	CALIP	VDQ	EDV1	EDVF
POR STATUS	0	0	0	1	0	0	0	0

CHGS Charge State flag. A *1* in the CHGS indicates a charge current ($V_{SRP} > V_{SRN}$). A *0* indicates a lack of charge activity. This bit should be read when the host system reads the Average Current register pair to determine the sign of the average current magnitude. This bit is cleared to *0* on all resets.

NOACT No Activity flag. A *1* indicates that the voltage across R_S is less than the digital magnitude filter. See the *Digital Magnitude Filter* section for more information. This bit is cleared to *0* on all resets.

IMIN Li-ion taper current detection flag. A *1* indicates that the charge current has tapered to less than the value set in EEPROM and that the battery voltage is greater than or equal to the value selected by the QV0 and QV1 bits in the PKCFG register (see EEPROM Data Register description for more details). Taper current detection is disqualified if AI < 8 (28.6 µV across sense resistor). The taper detection conditions must be maintained for 4 successive average current measurements (20-25 s) to qualify as a valid taper current detection. This bit is cleared to *0* on all resets.

CI Capacity Inaccurate flag. A *1* indicates that the firmware has not been through a valid learning cycle and is basing all calculations on initial design values programmed into EEPROM or that there have been at least 32 cycle-count increments since the last learning cycle. This bit is cleared only on a LMD update following a learning cycle. This bit is set to *1* on a full reset. The previous value is retained if no RAM corruption is detected after a reset.

CALIP Calibration-In-Progress flag. This flag is set whenever an automatic or commanded offset calibration measurement is being made. This bit is set to *0* on all resets.

VDQ Valid Discharge flag. A *1* indicates that the bqJUNIOR has met all necessary requirements for the firmware to learn the battery capacity. This bit clears to *0* on a LMD update or condition that disqualifies a learning cycle. This bit is cleared to *0* on all resets.

EDV1 First End-of-Discharge-Voltage flag. A *1* indicates that the voltage on the BAT pin is less than or equal to the EDV1 threshold voltage. LMD updates immediately if the VDQ bit is set when this bit transitions from *0* to 1. This bit is cleared when charging and on all resets.

EDVF Final End-of-Discharge-Voltage flag. A *1* indicates that the voltage on the BAT pin is less than or equal to the EDVF threshold voltage. This bit is cleared when charging and on all resets.

The host system has read-only access to this register.

Relative State-of-Charge (RSOC) — Address 0x0B

RSOC reports the nominal available capacity as a percentage of the last measured discharge value (LMD). The equation is:

RSOC (%) = 100 * NAC/LMD

The host system has read-only access to this register.

Nominal Available Capacity Registers (NACL/NACH) — Address 0x0C/0x0D

This register pair reports the light-load, or uncompensated, capacity available from the battery. NAC increments during charge ($V_{SRP} > V_{SRN}$) if Voltage > EDVF threshold and decrements during discharge ($V_{SRP} < V_{SRN}$). The NAC registers are cleared by a reset if RAM corruption is detected. The register value is retained after a reset if RAM corruption is not detected. The host system has read-only access to this register pair. NAC is reported in units of 3.57 µVh per count.

Last Measured Discharge Registers (LMDL/LMDH) – Address 0x0E/0x0F

This register pair reports the light load, or uncompensated, capacity available from the battery when fully charged. This value is updated after a valid learning cycle, which occurs when the battery is discharged from fully charged (NAC = LMD) until the EDV1 voltage threshold is detected (EDV1 = 1) without any learning cycle disqualifying event (VDQ = 1 during entire discharge). LMD will be updated with the measured capacity removed from the battery during the discharge until the EDV1 threshold is reached plus 6.25% of design capacity (the unmeasured capacity from EDV1 until the EDVF zero capacity threshold voltage) plus the computed capacity compensation reduction due to discharge rate, temperature, and age. The host system has read-only access to this register pair. LMD is reported in units of 3.57 µVh per count.

Compensated Available Capacity (CACL/CACH) – Address 0x10/0x11

This register pair reports the available capacity in the battery at the present discharge rate, temperature, and age. CAC is equal to NAC minus the capacity compensation reduction based on the compensation coefficients programmed in DCOMP (discharge compensation coefficients), TCOMP (temperature compensation coefficients), and GAF/DEDV (gain age compensation coefficient). All compensations are impedance-based and CAC will equal NAC at very low currents. However, CAC is not allowed to increase as long as there is no charging current. If the discharge load is reduced, CAC may stop decrementing even though NAC continues to decrement. When NAC drops sufficiently that the NAC minus CAC difference is equal to the discharge compensation at the reduced load current, CAC will again start decrementing. CAC will equal NAC when charging. The host system has read-only access to this register pair. CAC is reported in units of 3.57 µVh per count.

Fully-Charged Compensated Available Capacity (FCACL/FCACH) – Address 0x12/0x13

This register pair reports the fully-charged capacity of the battery at the present

Average Current Registers (AIL/AIH) — Address 0x14/0x15

Time-to-Empty Registers (TTEL/TTEH) — Address 0x16/0x17

Time-to-Full Registers (TTFL/TTFH) — Address 0x18/0x19

This register pair reports calculated time-to-full at the measured charge rate. The time computed at the average current charge rate is extended by 50% to estimate the effect of the current taper. TTF is reported in minutes. The equation for TTF is:

TTF = 60 * 1.50 * (LMD-NAC) / AI

The host system has read-only access to this register pair.

Standby Current Registers (SIL/SIH) — Address 0x1A/0x1B

This register pair reports measured standby current through the sense resistor. The standby current is an adaptive measurement. Initially, the register pair reports the standby current programmed in EEPROM and after spending some time in standby, the register pair reports the measured standby current. The register value is updated every 5.12 seconds when the measured current is above the DMF threshold and is less than or equal to 2x the initial programmed standby current value. Each new SI value is computed as follows:

SI_{NEW} = (15/16) * SI_{OLD} + (1/16) * AI

This filter function allows the

Standby Time-to-Empty Registers (STTEL/STTEH) — Address 0x1C/0x1D

Compensated End-of-Discharge Registers (CEDVL/CEDVH) – Address 0x20/0x21

Time-to-Empty at Constant Power Registers (TTECPL/TTECPH) – Address 0x26/0x27

Cycle Count Since Learning Cycle Registers (CYCLL/CYCLH) — Address 0x28/0x29

Cycle Count Total Registers (CYCTL/CYCTH) — Address 0x2A/0x2B

Compensated State-of-Charge (CSOC) — Address 0x2C

Reserved Registers

EEPROM Enable Register (EE_EN) — Address 0x6E

EEPROM Data Registers (EE_DATA) — Address 0x76 — 0x7F

Initial Last Measured Discharge High Byte (ILMD) — Address 0x76

Scaled EDVF Threshold (SEDVF) — Address 0x77

Scaled EDV1 Threshold (SEDV1) — Address 0x78

This register contains the scaled value of the voltage when the battery has 6.25% remaining capacity at a very light load. DEDV and EDVT coefficients can be programmed to reduce the EDVI threshold at heavier loads and at cold temperatures. When the battery reaches this threshold during a valid discharge, the device learns the full battery capacity, including the remaining unmeasured 6.25%. See the *bqJUNIOR Capacity Learning* section for more information on the learning cycles of the device. To calculate the value to program, use the following equation:

SEDV1 =

Initial Standby Load Current and EDV1 Temperature Compensation (ISLC/EDVT) – Address

Digital Magnitude Filter and Self-Discharge Values (DMFSD) — Address 0x7A

Taper Current (TAPER) — Address 0x7B

This register contains the enable bit for the capacity aging estimate and the charge taper current value. The taper current value, in addition to battery voltage, is used to determine when the battery has reached a full charge state. The equation for programming the taper current is:

TAPER[6-0] = Design Taper Current (mA) * R_S(mΩ) / 228 µV

where R_S is the value of the sense resistor used in the system.

TAPER[7] should be set to *1* to enable the automatic aging of the LMD full capacity value when there are no learning cycles. If this feature is enabled, LMD is reduced by Design Capacity / 1024 every time CYCL increments by 2 and every time that a cumulative NAC self-discharge estimate reduction of 1.56% has been made without charging the battery to full. If TAPER[7] is set to 0, there is no LMD reduction with cycle count or self-discharge.

Pack Configuration (PKCFG) — Address 0x7C

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GPIEN	QV1	QV0	BOFF(2)	BOFF(1)	BOFF(0)	DCFIX	TCFIX

GPIEN Allows the pack manufacturer to set the state of the GPIO pin on initial power up. If the bit is 0, the GPIEN bit is cleared on re1 0 0 1 349.82 2Tm /F2 -10 Tf (re1 06165.49 287.6 T13F2 -10 Tf (re1 0 0 1 3116.6 23

DCFIX Fixed discharge compensation. Normal discharge rate compensation (DCOMP register) is used if this bit is set to 0. If this bit is set to 1, the device assumes a fixed value of 0x6C for DCOMP, giving a discharge rate compensation gain (DCGN) of 5.08% with a compensation offset threshold of C/2. Setting the bit to *1* frees the EEPROM location of 0x7E for use as a programmable identification byte.

TCFIX Fixed temperature compensation. Normal temperature compensation (TCOMP register) is used if this bit is set to 0. If this bit is set to 1, the device assumes a fixed value of 0x46 for TCOMP, which will increase DCGN by 25% per °C below 12°C. Setting this bit to *1* frees the EEPROM location of 0x7F for use as a programmable identification byte.

Gain Age Factor and EDV1 Discharge Rate Compensation (GAF/DEDV) – Address 0x7D

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	GAF[1]	GAF[0]	DEDV[5]	DEDV[4]	DEDV[3]	DEDV[2]	DEDV[1]	DEDV[0]

Discharge Rate Compensation Coefficients (DCOMP) – Address 0x7E

Discharge Rate Compensation Threshold

DCOFF[2:0]	DCOFF Threshold (1)
0	0
1	(DCGN / 256) * 1C / 8
2	(DCGN / 256) * 2C / 8
3	(DCGN / 256) * 3C / 8
4	(DCGN / 256) * 4C / 8
5	(DCGN / 256) * 5C / 8
6	(DCGN / 256) * 6C / 8
7	(DCGN / 256) * 7C / 8

(1) C = ILMD * 256

The discharge compensation capacity reduction (DCMP) is a function of discharge rate, temperature, and age (cycle count). There is no compensation if the DCGN factor increased for age and temperature times AI is less than the DCOFF threshold (DCMP ≥ 0). The following is the combined equation for the DCMP reduction:

DCMP = AI * (ADCGN / 256) * (1 + TCGN * (273 + TOFF – T) / 32) – DCGN * DCOFF * ILMD / 8

ADCGN = DCGN * (1 + TCGN * (CYCT / 16) * GAF / 32)

If PKCFG[1] = 1, the bqJUNIOR assumes a fixed value of 0x6C for DCOMP, giving a discharge rate compensation gain of 5.08% with a compensation offset threshold of C/2. This frees the EEPROM location of 0x7E for use as a programmable identification byte. If DCOMP is updated using the UPCOMP host command (see Device Control section), the value written by the host for DCOMP will be used regardless of the bit 1 value in PKCFG.

Temperature Compensation Coefficients (TCOMP) – Address 0x7F

This register is used to set the compensation coefficients for temperature. These coefficients are used to scale the aged discharge rate compensation for improved accuracy of predicted available capacity at cold temperatures.

	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
NAME	TCGN[4]	TCGN[3]	TCGN[2]	TCGN[1]	TCGN[0]	TOFF[2]	TOFF[1]	TOFF[0]

TCGN[4:0] The temperature compensation gain coefficient is used to scale DCGN when temperature drops below the T_{off} threshold. TCGN will increase the ADCGN value in increments of 3.125% (TCGN / 32) for each degree that temperature is below the T_{off} threshold.

TOFF[2:0] The temperature compensation offset threshold sets the temperature above which there is no temperature compensation applied to DCGN. This threshold is also used as the threshold for application of cold temperature compensation of EDV1 (see GAF/EDVT section) and the threshold to allow the NAC = LMD capacity adjustment to be made at IMIN detection (see Functional Description section). The T_{off} threshold in degrees Celsius is equal to 2 * TOFF.

If PKCFG[0] = 1, the bqJUNIOR assumes a fixed value of 0x46 for TCOMP. This will increase the DCGN factor by 25% per degree below T_{off} of 12°C. This frees the EEPROM location of 0x7F for use as a programmable identification byte. If TCOMP is updated using the UPCOMP host command (see Device Control section), the value written by the host for TCOMP will be used regardless of the bit 0 value in PKCFG.

Power Modes

The bqJUNIOR has

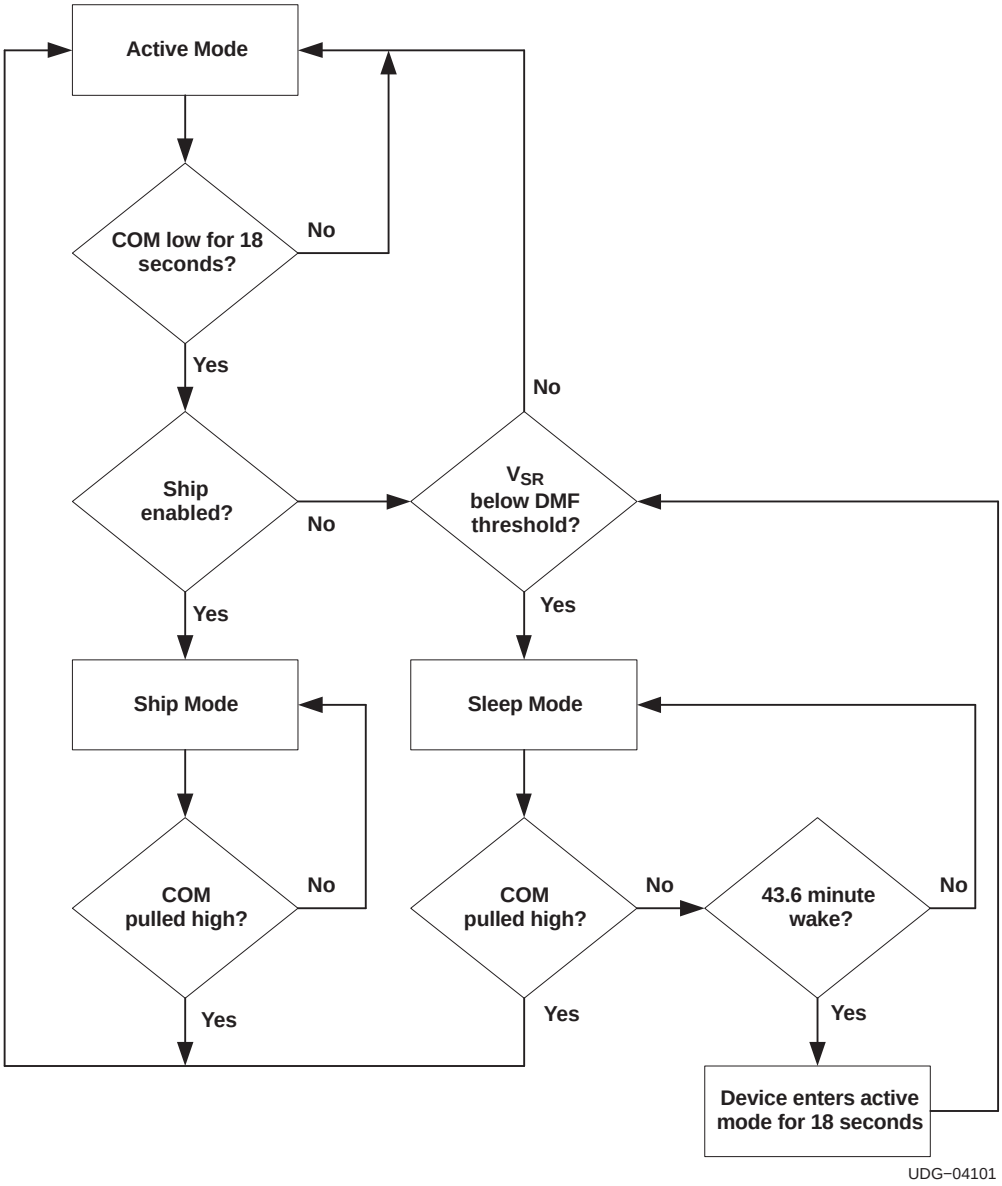


Figure 5. Power Mode Flow Chart

Active Mode

During normal operation, the device is in active mode, which corresponds to the highest power consumption. Normal gas gauging is performed in this mode. If system requirements mandate that bqJUNIOR should not enter Sleep or Ship modes, then an external pullup resistor from V_{CC} to keep HDQ or CLK and DTA at a logic *1* is required on the bqJUNIOR side of the system. The resistor value chosen should be small enough to force a logic *1* even with the internal pulldown current and any external ESD protection circuitry loading.

Sleep Mode

This low power mode is entered when the HDQ or CLK and/or DTA line is pulled low for at least 18 seconds and the charge or discharge activity is below the DMF threshold. Normal gas gauging ceases, but battery self-discharge, based on the temperature when the device entered sleep mode, is maintained internally. The device wakes every 43.6 minutes to update the temperature measurement and goes back to sleep after about 18 seconds if the HDQ or CLK and/or DTA line is still low and the charge or discharge activity is still below the DMF threshold. The bqJUNIOR has an internal 3 μA pulldown current on each communication line, eliminating the need to add external pulldown resistors to force a logic *0* on open communication lines.

When the device wakes, it stays in active mode long enough to confirm that the charge or discharge activity is still below the digital magnitude filter threshold. This is meant to minimize possible error if the battery pack is removed from the end equipment for a short period of time and then reinserted, and there is not a transient on the communication lines to pull the device into the active mode. This is an issue only if the system has some current drain from the battery even though the communication lines are low. The gauge reenters sleep mode when the charge or discharge activity falls below the digital magnitude filter threshold.

When all communication lines are pulled high, the device leaves the sleep mode. If the DMF threshold is set to zero and a communication line is pulled low, the device does not enter sleep mode until the average current value is less than 3.57 μV/Rsr.

If the battery pack can be removed and placed on an external charger, the charger should have a pull-up resistor on the HDQ or SCL and SDA lines to wake the part from sleep. A 100 kΩ pullup resistor from communication line(s) to V_{CC} can be added in the battery pack to disable the sleep function.

Ship Mode (bq27010 only)

This low power mode is to be used when the pack manufacturer has completed assembly and test of the pack. The ship mode is enabled by setting the SHIP bit in the MODE register and issuing the control command (data 0xA9 to register 0x00). Ship mode is entered only when the ship mode is enabled and the HDQ or CLK and/or DTA line has been pulled low for at least 18 seconds. This allows the pack manufacturer to enable the ship mode and pull the pack from the test equipment without any additional overhead. Transients on a communication line after the ship mode has been enabled but before the device has entered ship mode, do not cause the device to stay in active mode. Transients on a communication line, after the device has entered ship mode can wake the part from ship mode, but if there is no charge or discharge activity above the DMF threshold, the part automatically enters the Sleep mode as previously described.

All device functionality stops in ship mode and it does not start again until the communication lines are pulled high or the battery voltage drops below and then rises above the $V_{(POR)}$ threshold. A full reset is forced when the part leaves ship mode. If the current NAC value must be retained after waking, ship mode should not be used.

Hibernate Mode

The device enters hibernate mode when V_{CC} drops below $V_{(POR)}$. V_{CC} must be raised above $V_{(POR)}$ in order to exit the hibernate mode. If RBI voltage does not drop below 1.3 V, RAM content is maintained and allows retention of NAC, LMD, CYCL, CYCT, and the CI flag after V_{CC} is raised above $V_{(POR)}$.

Programming the EEPROM

The bqJUNIOR has 10 bytes of EEPROM that are used for firmware control and application data (see the *bqJUNIOR Register Descriptions* section for more information). Programming the EEPROM should take place during pack manufacturing because a 21 V pulse is needed on the PROG pin. The programming mode must be enabled prior to writing any values to the EEPROM locations. The programming mode is enabled by writing to the EE_EN register (address 0x6E) with data 0xDD. Once the programming mode is enabled, the desired data can be written to the appropriate address. Figure 6 shows the method for programming all locations.

Communicating with the bq27210 (I²C interface - Product Preview)

The bq27210 supports the standard I²C read, incremental read, quick read, and one byte write functions. The 7-bit device address (ADDR) is the most significant 7 bits of the hex address and is fixed as 1010101. The 8-bit device address is therefore 0xAA or 0xAB for write or read, respectively. (S = Start, Sr = Repeated Start, A = Acknowledge, N = No Acknowledge, and P = Stop)

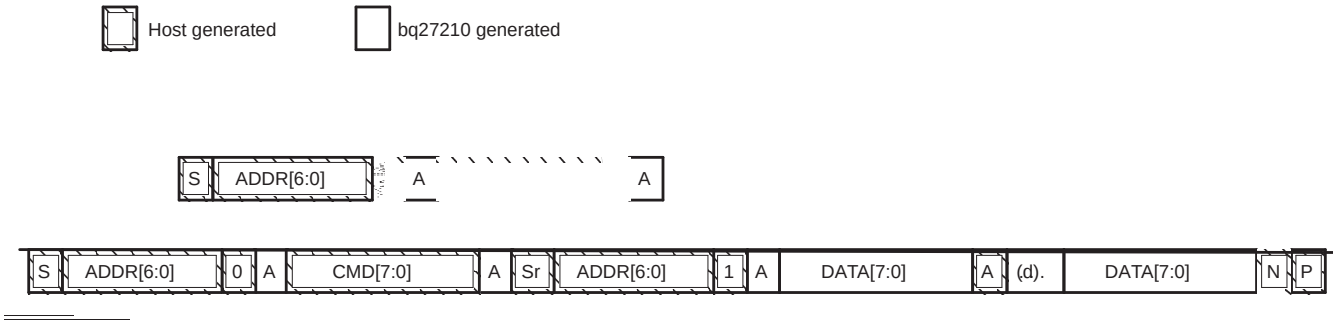
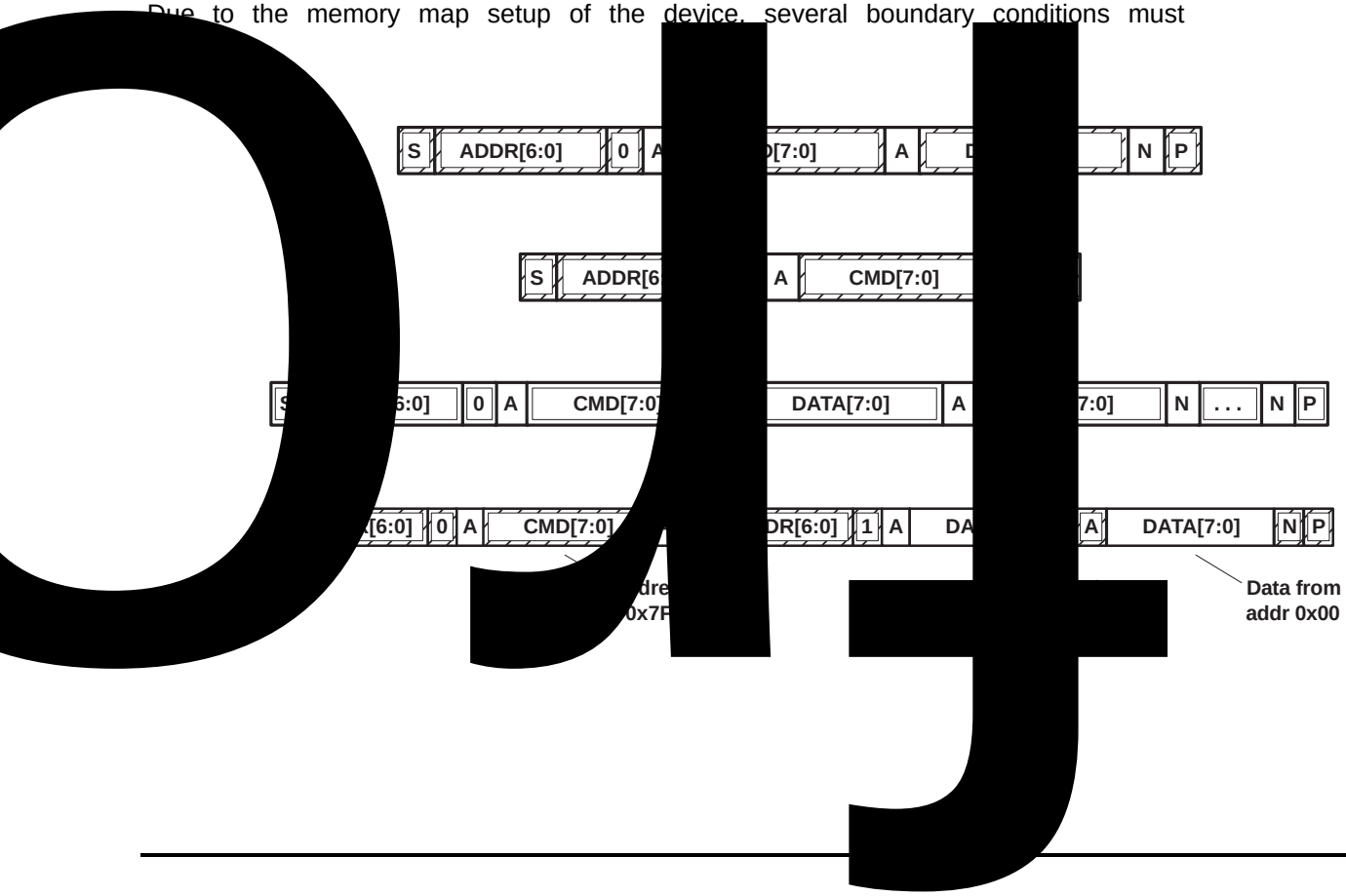


Figure 7. Supported I2C formats :
(a) 1-byte write; (b) quick read; (c) 1-byte read; (d) incremental read

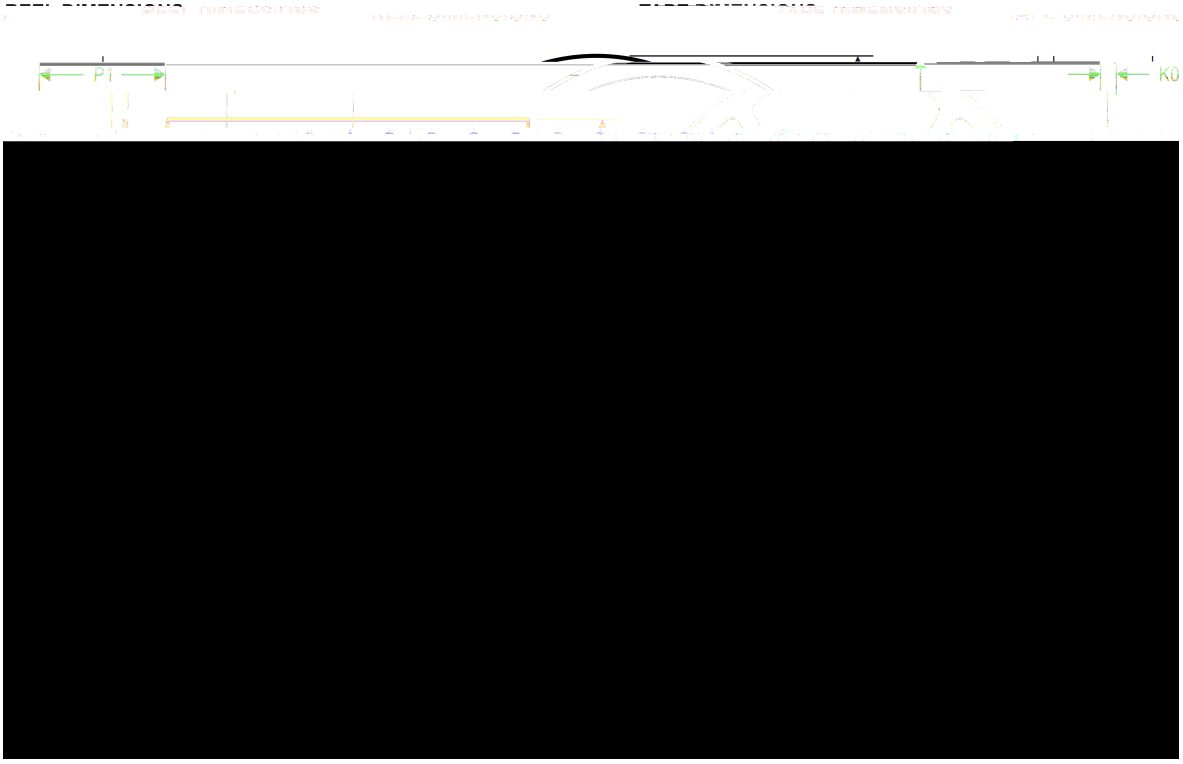
The incremental read protocol is recommended for reading all 16-bit values, as this ensures that the 16-bit value is not updated during the time interval between reading the two bytes of data (see previous section on reading 16-bit values). The quick read returns data at the address indicated by the internal address pointer. The address pointer is incremented after each data byte is read or written. Reading an even address causes the communication engine to simultaneously capture the data byte from the requested even address and the data byte from the next odd address, and the address pointer is incremented twice. The data byte captured from the next odd address is output if the communication continues, without a stop, after the host acknowledges the even address byte.

Due to the memory map setup of the device, several boundary conditions must



PACKAGING INFORMATION

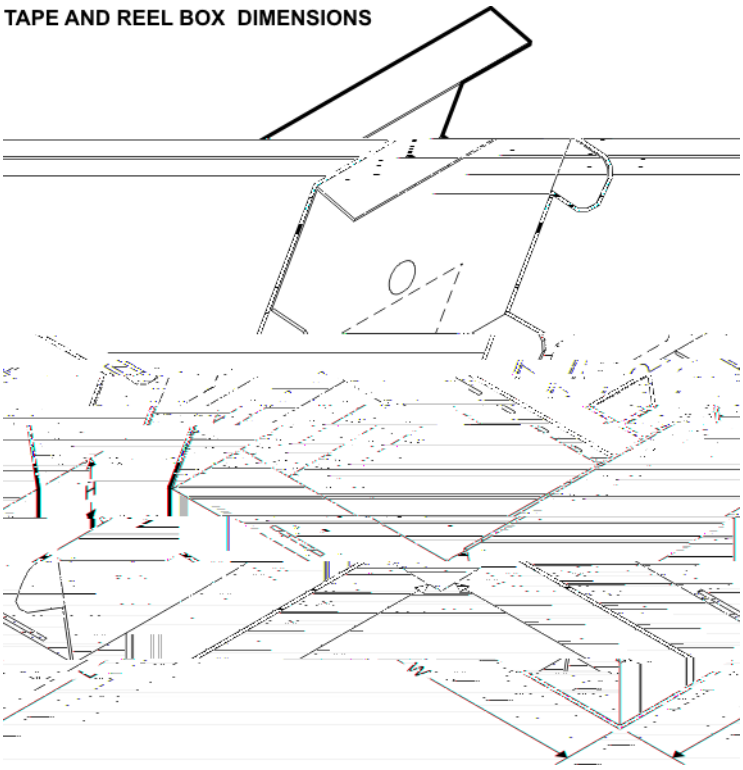
TAPE AND REEL INFORMATION



*All dimensions are nominal

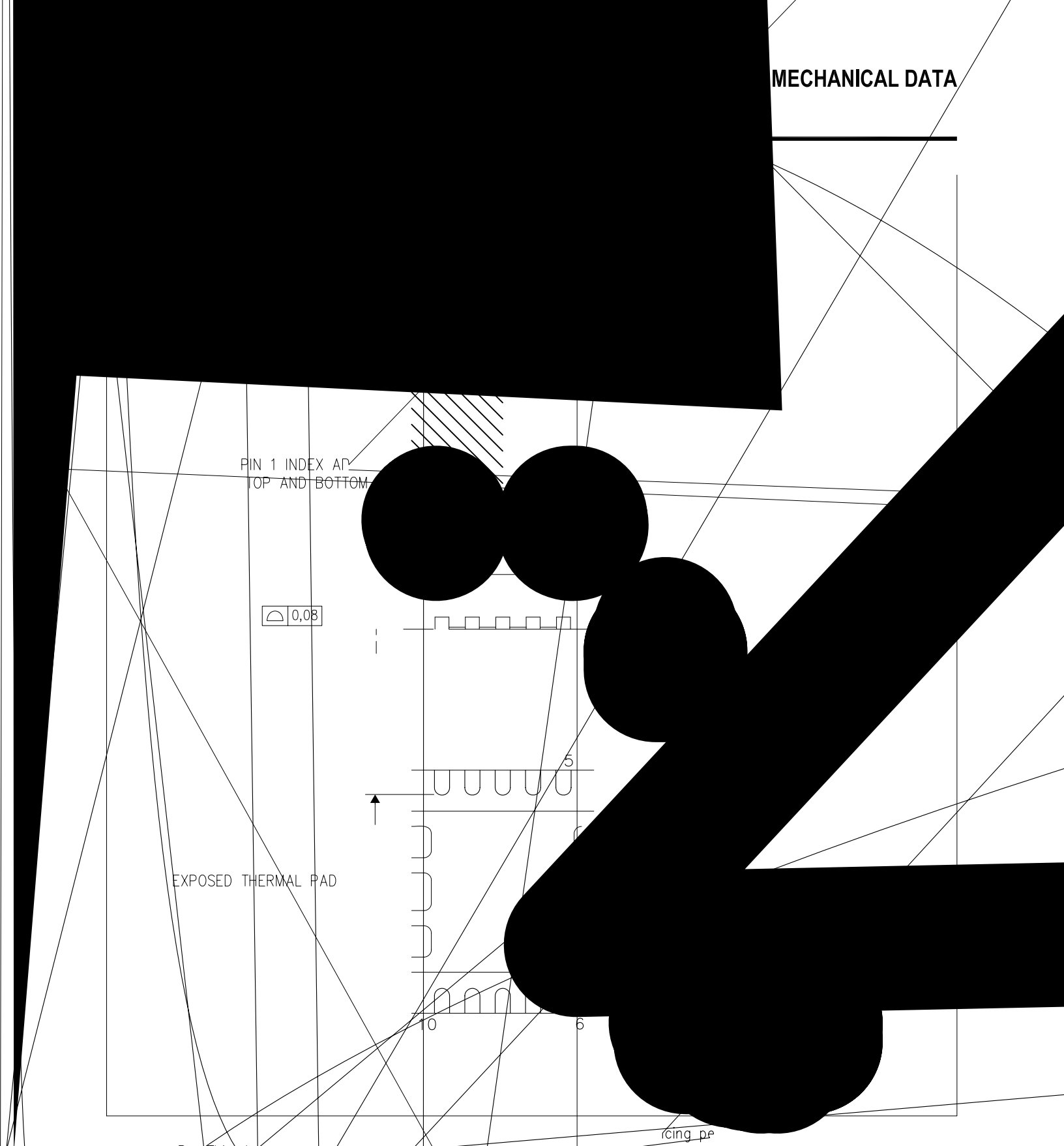
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ27010DRKR	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q2
BQ27210DRKR	VSON	DRK	10	3000	330.0	12.4	3.3	4.3	1.6	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ27010DRKR	VSON	DRK	10	3000	338.1	338.1	20.6
BQ27210DRKR	VSON	DRK	10	3000	338.1	338.1	20.6



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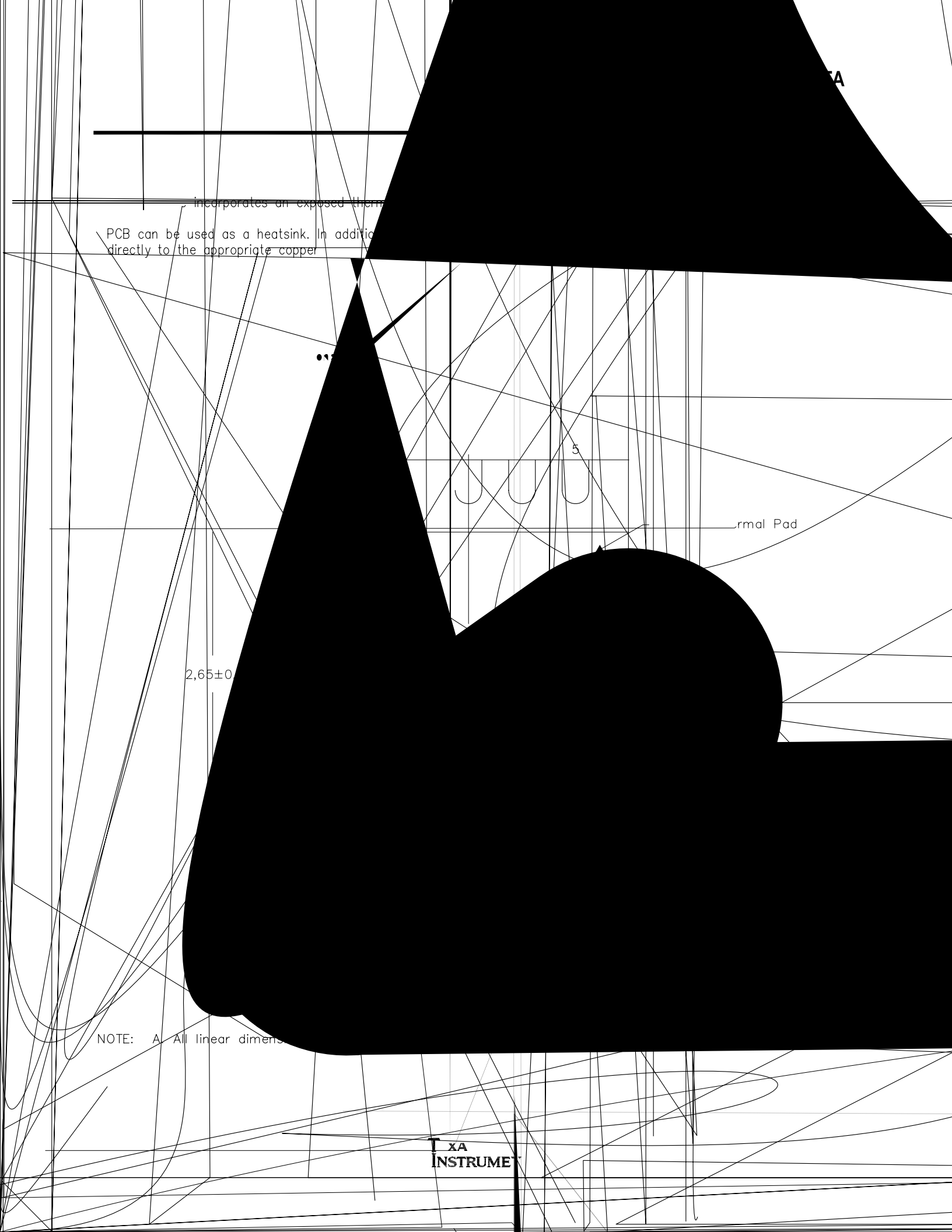
B. This dr
C. Small Outline No-Lead (SON) package configuration.
ckage thermal pad must be soldered to the board for thermal and mechanical performance.


PCB can be used as a heatsink. In addition
directly to the appropriate copper
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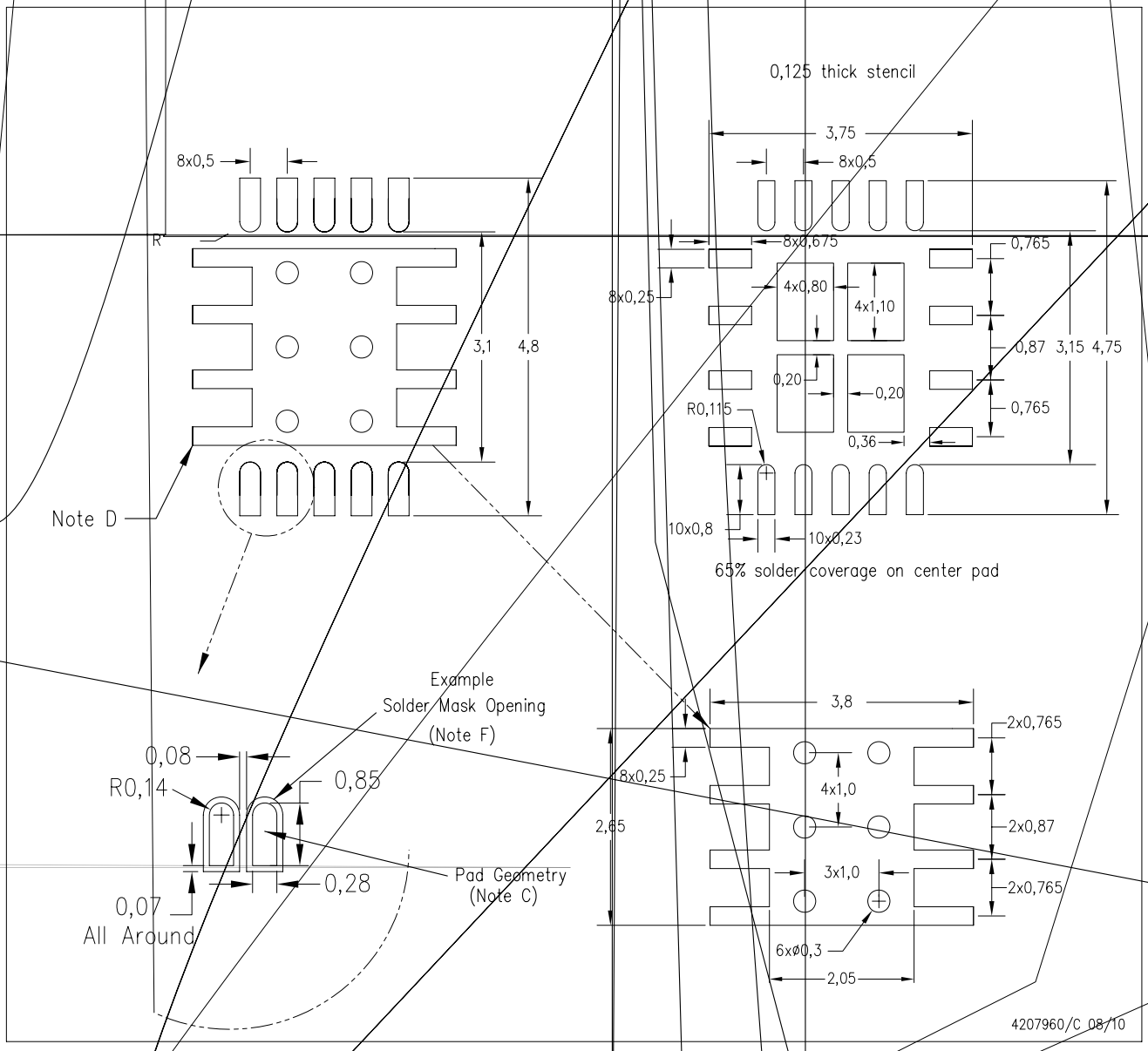
2,65±0
NOTE: A. All linear dimens
TEXAS INSTRUMENTS

DRK (S–PVSON–N10) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sh
for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. ers will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web nces between signal pads.

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