UNITRODE

bq2054

Lithium Ion Fast-Charge IC

Features

- Safe charge of Li hi m Ion ba - er packs
- Vol age-reg la ed c rren - limi ed charging
- Fas charge ermina ed b selec able minim m c rren ; safe back p ermina ion on ma im m ime
- Charging con in o sl q alified b empera re and ol age limi s
- P lse- id h mod la ion con rol ideal for high-efficienc s i ch-mode po er con ersion
- Direc LED con rol o p s displa charge s a s and fa l condi ions

General Description

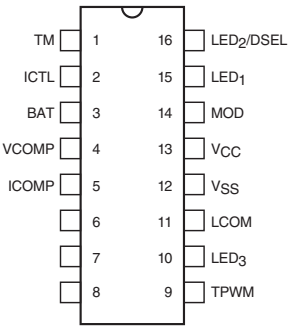
The bq2054 Li hi m Ion Fas - Charge IC is designed o op imi e charging of li hi m ion (Li-Ion) chemis r ba eries. A fle ible p lse- id h mod la ion reg la or allo s he bq2054 o con rol ol age and c rren d ring charging. The reg la or freq enc is se b an e - ernal capaci or for design fle ibili . The s i ch-mode design keeps po er dissipa ion o a minim m.

The bq2054 meas res ba er empera re sing an e ernal hermis- or for charge q alifica ion. Charging begins hen po er is applied or on ba er inser ion.

For safe , he bq2054 inhibi s charging n il he ba er ol age and empera re are i hin con- fig red limi s. If he ba er ol age is less han he lo - ol age hresh- old, he bq2054 pro ides lo -c rren condi ioning of he ba er .

A cons an c rren -charging phase replenishes p o 70% of he charge capaci , and a ol age-reg la ed phase re rns he ba er o f ll. The charge c cle ermina es hen he charging c rren falls belo a ser-selec able c rren limi . For safe , charging ermina es af er ma im m ime and is s spended if he empera re is o - side he preconfig red limi s.

The bq2054 pro ides s a s indica- ions of all charger s a es and fa l s for acc ra e de ermina ion of he ba er and charge s s em condi- ions.



16-Pin Narrow
DIP or SOIC

PN205401.eps

TM	Time-out programming input
$\overline{\text{ICTL}}$	Inrush current control output
BAT	Battery voltage input
VCOMP	Voltage loop comp input
ICOMP	Current loop comp input
I_{TERM}	Minimum current termination select input
SNS	Sense resistor input
TS	Temperature sense input

Pin Descriptions

TM **T**

This inp se s he ma im m charge ime. The resis or and capaci or al es are de ermined sing Eq a ion 5. Fig re 7 sho s he resis or/capaci or connec ion.

$\overline{\text{ICTL}}$ **I**

$\overline{\text{ICTL}}$ is dri en lo d ring he fa l or charge-comple e s a es of he chip. I is sed o disconnec he capaci or across he ba er pack erminals, pre en ing inr sh c rren s from ripping o erc rren pro ec ion fea- res in he pack hen a ne ba er is inser ed.

BAT **Ba**

BAT is he ba er ol age sense inp . This po en ial is generall de eloped sing a high-impedance resis or di ider ne ork connec ed be een he posi i e and he nega i e erminals of he ba er . See Fig- re 4 and Eq a ion 1.

VCOMP **V**

This inp ses an e ernal R-C ne ork for ol age loop s abili .

I_{TERM} **M**

This hree-s a e inp is sed o se I_{MIN} for fas charge ermina ion. See Table 2.

ICOMP **C**

This inp ses an e ernal R-C ne ork for c rren loop s abili .

Charge Algorithm

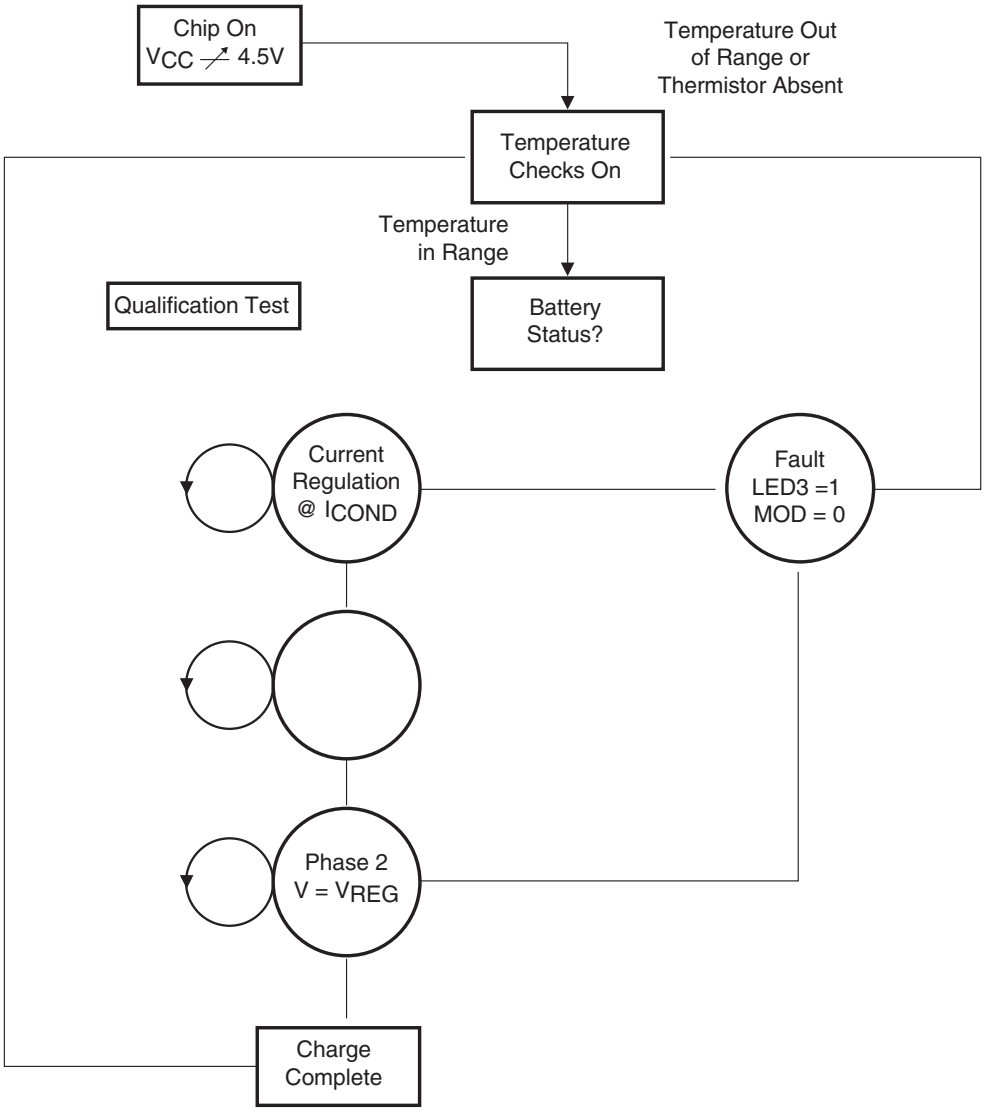
The bq2054 ses a o-phase fas charge algori hm. In phase 1, he bq2054 reg la es cons an c rren (I_{SNS} = I_{MAX}) n il V_{CELL} (= V_{BAT} - V_{SNS}) rises o V_{REG}. The bq2054 hen ransi ions o phase 2 and reg la es cons an ol age (V_{CELL} = V_{REG}) n il he charging c rren falls belo he programmed I_{MIN} hreshold. The charging c rren m s remain belo I_{MIN} for 120 40ms before a alid fas charge ermina ion is de ec ed. Fas charge hen ermina es, and he bq2054 en ers he Charge Comple e s a e. See Fig res 1 and 2.

Charge Qualification

The bq2054 s ar s a charge c cle hen po er is applied hile a ba er is presen or hen a ba er is inser ed. Fig re 2 sho s he s a e diagram for pre-charge q alifica ion and empera re moni oring. The bq2054 firs checks ha he ba er empera re is i hin he allo ed, ser-config rable range. If he empera re is o of range, he bq2054 en ers he Charge Pending s a e and ai s n il he ba er empera re is i hin he allo ed range. Charge Pending is en ncia ed b LED_3 flashing.

Thermal moni oring con in es hro gho he charge c cle, and he bq2054 en ers he Charge Pending s a e hen he empera re o of range. (There is one e ception; if he bq2054 is in he Fa l s a e see belo he o -of-range empera re is no recogni ed n il he bq2054 lea es he Fa l s a e.) All imers are s spended (b no rese) hile he bq2054 is in Charge Pending. When he empera re comes back in o range, he bq2054 re rns o he poin in he charge c cle here he o -of-range empera re as de ec ed.

When he empera re is alid, he bq2054 hen reg la es c rren o I_{COND} (=I_{MAX}/5). Af er an ini ial holdoff period $_{HO}$ (hich pre en s he chip from reac ing o ransien ol age spikes ha ma occ r hen charge c rren is firs applied), he chip begins moni oring V_{CELL}. If V_{CELL} does no rise o a leas V_{MIN} before he e pira ion of ime-o limi $_{MTO}$ (e.g. he cell has failed shor), he bq2054 en ers he Fa l s a e. If V_{MIN}


Chip On
VCC ↗ 4.5V
Temperature Out
of Range or
Thermistor Absent
Temperature
Checks On
Temperature
in Range
Qualification Test
Battery
Status?
Current
Regulation
@ ICOND
Fault
LED3 =1
MOD = 0
Phase 2
V = VREG
Charge
Complete

Charge Status Display

Charge s a s is en ncia ed b he LED dri er o p s LED1 LED2 LED3. Three displa modes are a ailable in he bq2054; he ser selec s a displa mode b config ring pin DSEL. Table 1 sho s he hree displa modes.

The bq2054 does no dis ing ish be een an o er- ol age fa l and a ba er absen condi ion. The bq2054 en ers he Fa l s a e, en ncia ed b rning on LED3, hene er he ba er is absen . The bq2054, herefore, gi es an indica ion ha he charger is on e en hen no ba er is in place o be charged.

Configuring the Display Mode and I_{MIN}

DSEL/LED2 is a bi-direc ional pin i h o f nc ions; i is an LED dri er pin as an o p and a programming pin as an inp . The selec ion of p ll- p, p ll-do n, or no p ll resis or programs he displa mode on DSEL per Table 1. The bq2054 la ches he programming da a sensed on he DSEL inp hen an one of he follo ing hree e en s occ rs:

1. V_{CC} rises o a alid le el.
2. The bq2054 lea es he Fa l s a e.
3. The bq2054 de ec s ba er inser ion.

The LEDs go blank for appro ima el 750ms (pical) hile ne programming da a is la ched.

Table 1. bq2054 Display Output Summary

Mode	Charge Action State	LED_1	LED_2	LED_3
DSEL = 0 (Mode 1)	Ba er absen or o er- ol age fa l	Lo	Lo	High
	Pre-charge q alifica ion	Flash	Lo	Lo
	Fas charging	High	Lo	Lo
	Charge comple e	Lo	High	Lo
	Charge pending (empera re o of range)	X	X	Flash
	Charging fa l	X	X	High
DSEL = 1 (Mode 2)	Ba er absen or o er- ol age fa l	Lo	Lo	High
	Pre-charge q alifica ion	High	High	Lo
	Fas charge	Lo	High	Lo
	Charge comple e	High	Lo	Lo
	Charge pending (empera re o of range)	X	X	Flash
	Charging fa l	X	X	High
DSEL = Floa (Mode 3)	Ba er absen or o er- ol age fa l	Lo	Lo	High
	Pre-charge q alifica ion	Flash	Flash	Lo
	Fas charge: c rren reg la ion	Lo	High	Lo
	Fas charge: ol age reg la ion	High	High	Lo
	Charge comple e	High	Lo	Lo
	Charge pending (empera re o of range)	X	X	Flash
	Charging fa l	X	X	High

N : 1 = V_{CC}; 0 = V_{SS}; X = LED s a e hen fa l occ rred; Flash = ⅙ sec. lo , ⅙ sec high.

Fas charge ermina es hen he charging c rren drops belo a minim m c rren hreshold programmed b he al e of I_{TERM} (see Table 2) and remains belo ha le el for 120 40ms.

Fig re 3 sho s he bq2054 config red for displa mode 2 and $I_{MIN} = I_{MAX}/10$.

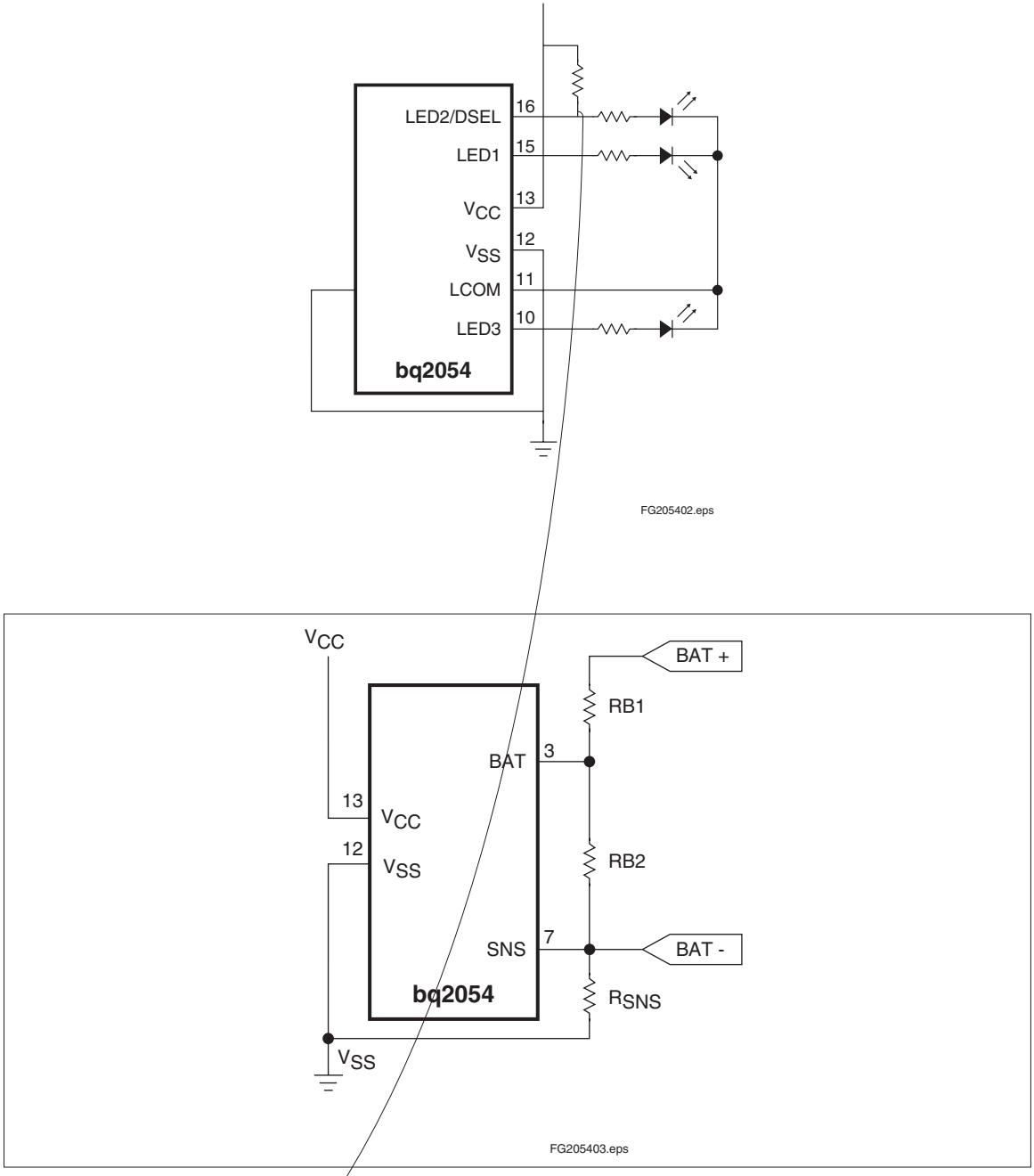


Figure 4. Configuring the Battery Divider

Battery Insertion and Removal

V_{CELL} is in erpre ed b he bq2054 o de ec he presence or absence of a ba er . The bq2054 de ermines ha a ba er is presen hen V_{CELL} is be een he High-Vol age C off (V_{HCO} = V_{REG} + 0.25V) and he Lo -Vol age C off (V_{LCO} = 0.8V). When V_{CELL} is o side his range, he bq2054 de ermines ha no ba er is presen and ransi ions o he Fa l s a e. Transi ions in o and o of he range be een V_{LCO} and V_{HCO} are rea ed as ba er inser ions and remo als, respec i el . The V_{HCO} limi also implici l ser es as an o er-ol age charge ermina ion.

Inrush Current Control

Whene er he bq2054 is in he fa l or charge-comple e s a e, he $\overline{ICTL}$ o p is dri en lo . This o p can be sed o disconnec he capaci or s all presen in he charger across he posi i e and nega i e ba er erminals, pre en ing he cap from s ppl ing large inr sh c rren s o a ne l inser ed ba er . S ch inr sh c rren s ma rip he o erc rren pro ec ion circ i r s all presen in Li-Ion ba er packs.

Temperature Monitoring

The bq2054 moni ors empera re b e amining he ol age presen ed be een he TS and SNS pins b a resis or ne ork ha incl des a Nega i e Tempera re Coefficien (NTC) hermis or. Resis ance aria ions aro nd ha al e are in erpre ed as being propor ional o he ba er empera re (see Fig re 6).

The empera re hresholds sed b he bq2054 and heir corresponding TS pin ol age are:

- TCO (Tempera re C off): Higher limi of he empera re range in hich charging is allo ed. V_{TCO} = 0.4 * V_{CC}
- HTF (High-Tempera re Fa l): Threshold o hich empera re m s drop af er empera re c off is e ceeded before charging can begin again. V_{HTF} = 0.44 * V_{CC}
- LTF (Lo -Tempera re Fa l): Lo er limi of he empera re range in hich charging is allo ed. V_{LTF} = 0.6 * V_{CC}

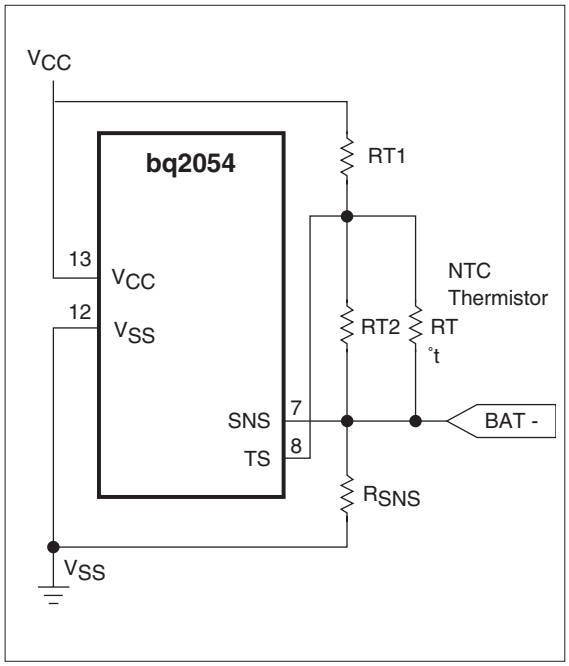


Figure 5. Configuring Temperature Sensing

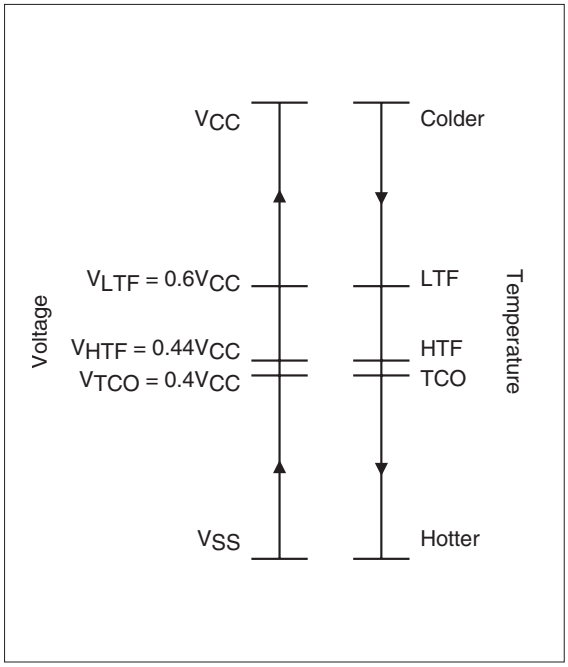


Figure 6. Voltage Equivalent of Temperature

A resis or-di ider ne ork can be implemen ed ha presen s he defined ol age le els o he TS pin a he desired empera res (see Fig re 6).

Absolute Maximum Ratings

Symbol	Parameter	Minimum	Maximum	Unit	Notes
V_{CC}	V_{CC} rela i e o V_{SS}	-0.3	+7.0	V	
V_T	DC ol age applied on an pin e - cl ding V_{CC} rela i e o V_{SS}	-0.3	+7.0	V	
T_{OPR}	Opera ing ambien empera re	-20	+70	C	Commercial
T_{STG}	S orage empera re	-55	+125	C	
T_{SOLDER}	Soldering empera re	-	+260	C	10 sec. ma .

N : Permanen de ice damage ma occ r if **Ab Ma Ra .** are e ceeded. F nc ional operation sho ld be limi ed o he Recommended DC Opera ing Condi ions de ailed in his da a shee . E posre o condi ions be ond he opera ional limi s for e ended periods of ime ma affec de ice reliabili .

DC Thresholds ($T_A = T_{OPR}$; V_{CC} = 5V 10%)

Symbol	Parameter	Rating	Unit	Tolerance	Notes
V_{REF}	In ernal reference ol age	2.05	V	1%	T_A = 25 C
	Tempera re coefficien	-0.5	mV/ C	10%	
V_{LTF}	TS ma im m hreshold	0.6 * V_{CC}	V	0.03V	Lo - empera re fa l
V_{HTF}	TS h s eresis hreshold	0.44 * V_{CC}	V	0.03V	High- empera re fa l
V_{TCO}	TS minim m hreshold	0.4 * V_{CC}	V	0.03V	Tempera re c off
V_{HCO}	High c off ol age	2.3V	V	1%	
V_{MIN}	Under- ol age hreshold a BAT	0.2 * V_{CC}	V	0.03V	
V_{LCO}	Lo c off ol age	0.8	V	0.03V	
V_{SNS}	C rren sense a SNS	0.250	V	10%	I_{MAX}
		0.050	V	10%	I_{COND}

Impedance

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
R_{BATZ}	BAT pin inp impedance	50	-	-	M	
R_{SNSZ}	SNS pin inp impedance	50	-	-	M	
R_{TSZ}	TS pin inp impedance	50	-	-	M	
R_{PROG1}	Sof -programmed p ll- p or p ll-do n resis or al e (for programming)	-	-	10	k	DSEL
R_{PROG2}	P ll- p or p ll-do n resis or al e	-	-	3	k	I_{TERM}
R_{MTO}	Charge imer resis or	20	-	480	k	

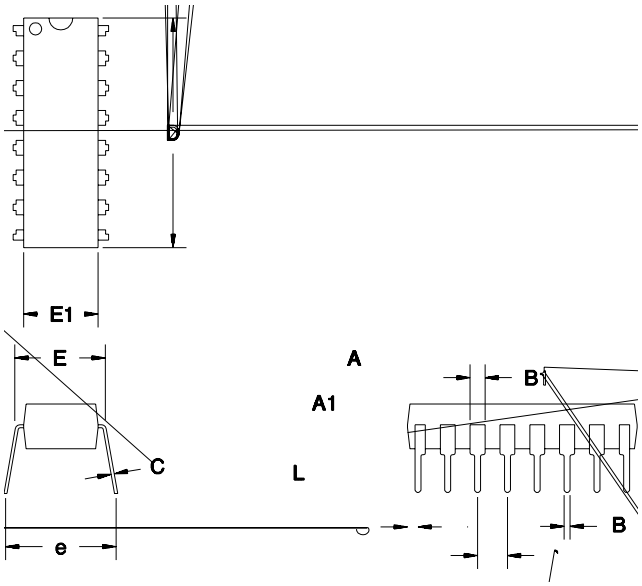
Timing (TA = TOPR; VCC = 5V 10%)

Symbol	Parameter	Minimum	Typical	Maximum	Unit	Notes
MTO	Charge ime-o range	1	-	24	ho rs	See Fig re 7
QT	Pre-charge q al es ime-o period	-	MTO	-	-	
HO	Termina ion hold-off period	1.14	-	1.52	sec.	
IMIN	Min. c rren de ec fil er period	80		160	msec.	
F_{PWM}	PWM reg la or freq enc range	-	100		kH	C_{PWM} = 0.001 F (eq a ion 7)

Capacitance

Symbol	Parameter	Minimum	Typical	Maximum	Unit
C_{MTO}	Charge imer capaci or	-	-	0.1	F
C_{PWM}	PWM R-C capaci ance	-	0.001	-	F

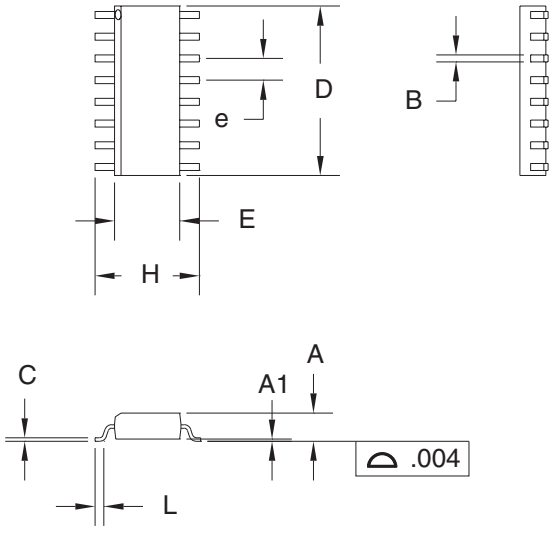
16-Pin DIP Narrow (PN)



16-Pin PN (0.300" DIP)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.160	0.180	4.06	4.57
A1	0.015	0.040	0.38	1.02
B	0.015	0.022	0.38	0.56
B1	0.055	0.065	1.40	1.65
C	0.008	0.013	0.20	0.33
D	0.740	0.770	18.80	19.56
E	0.300	0.325	7.62	8.26
E1	0.230	0.280	5.84	7.11
e	0.300	0.370	7.62	9.40
G	0.090	0.110	2.29	2.79
L	0.115	0.150	2.92	3.81
S	0.020	0.040	0.51	1.02

16-Pin SOIC Narrow (SN)



16-Pin SN (0.150" SOIC)

Dimension	Inches		Millimeters	
	Min.	Max.	Min.	Max.
A	0.060	0.070		

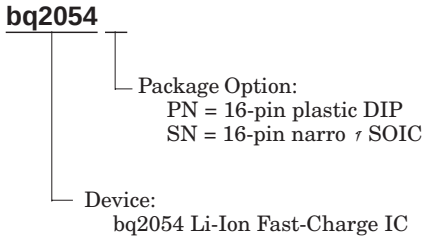
Ma .

Data Sheet Revision History

Change No.	Page No.	Description	Nature of Change
1	5, 7, 8, 10	Value Change	Changed V_{SNS} and I_{MAX}
2	5, 10	Value Change	Changed V_{REF}
3	10	Coefficient Addition	Temperature coefficient added
4	5	Ne r state diagram	Diagram inserted
4	1, 2, 8, 12	NC pin replaced rith $\overline{ICTL}$	
4	3, 5, 13	Termination hold-off period added I_{MIN} detect filtering added	
5	11	V_{HCO} Rating changed to 2.3V V_{HCO} Tolerance changed to 1%	Changed values for V_{HCO}
6	13	t_{QT} in Timing Specifications	t_{QT} changed from (0.16 * t_{MTO}) to t_{MTO}
7	5	I_{TERM} in Table 2	Z changes to Float
7	8	Figure 6	RB1 and RB2 changed to RT1 and RT2
8	10	T_{OPR}	Deleted industrial temperature range.

Notes: Change 3 = April 1996 C changes from Dec. 1995 B.
Change 4 = Sept. 1996 D changes from April 1996 C.
Change 5 = Nov. 1996 E changes from Sept. 1996 D.
Change 6 = Oct. 1997 F changes from Nov. 1996 E.
Change 7 = Oct. 1997 G changes from Oct. 1997 F.
Change 8 = June 1999 H changes from Oct. 1997 G.

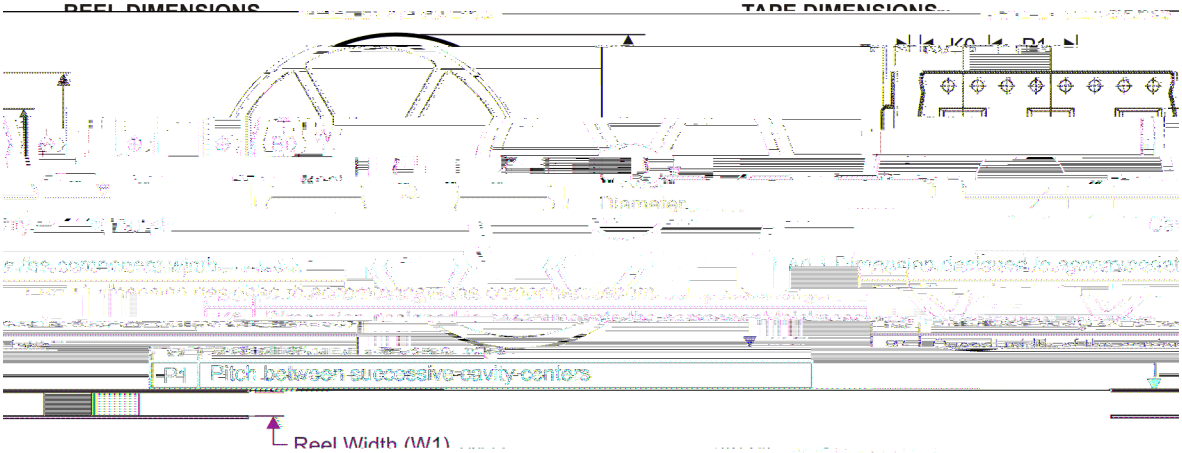
Ordering Information

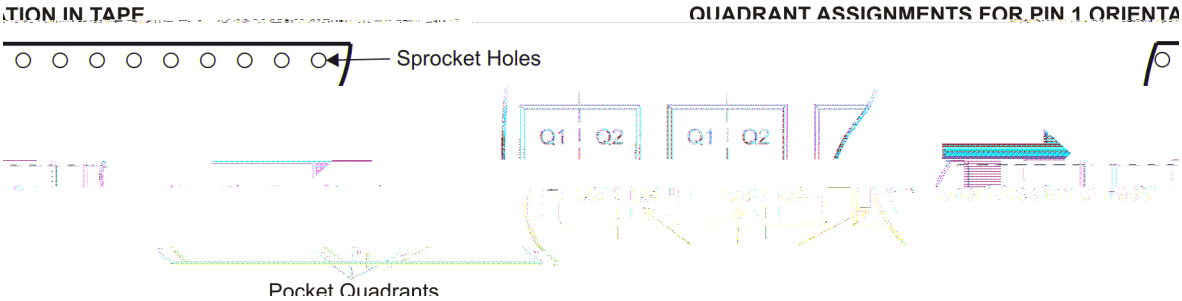


PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty

TAPE AND REEL INFORMATION

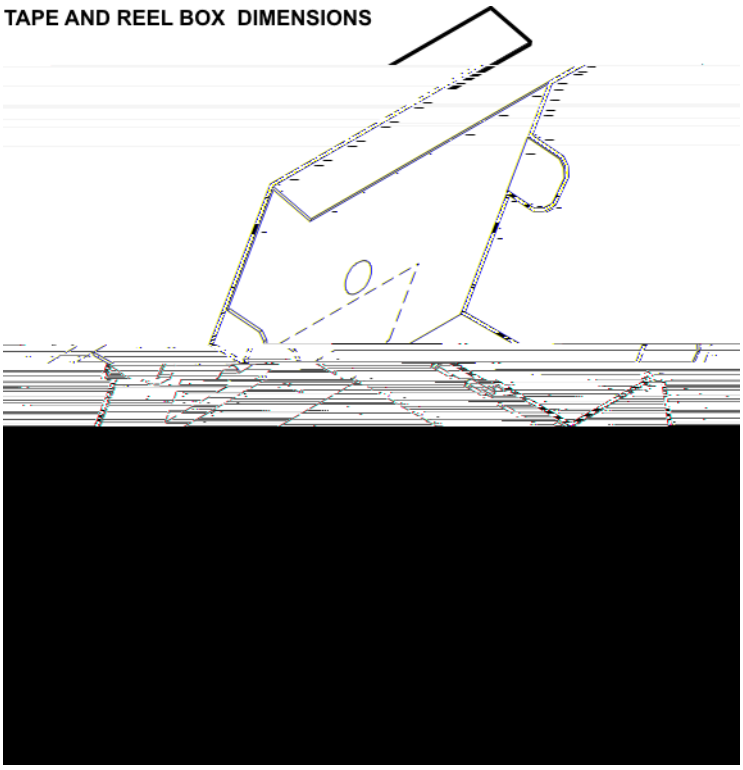




*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ2054SNTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	

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