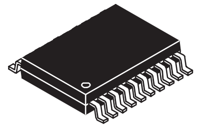
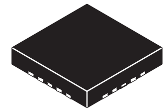




SINGLE-CELL Li-ION CHARGE MANAGEMENT IC WITH TIMER-ENABLE FOR PDAs AND INTERNET APPLIANCES

FEATURES

- **Highly Integrated Solution With FET Pass Transistor and Reverse-Blocking Schottky and Thermal Protection**
- **Timer-Enable Function That Allows Host to Disable Charge Timer and Termination When Charge Current Is Shared With a Load or When Battery Is Absent**
- **Integrated Voltage and Current Regulation With Programmable Charge Current**
- **High-Accuracy Voltage Regulation (±1%)**
- **conditioning, the bq2400x applies a constant-charge current to the battery. An external sense-resistor sets the magnitude of the current. The constant-current phase is maintained until the battery reaches the charge-regulation voltage. The bq2400x then transitionsto the constant voltage phase. The user can configure the device for cells with either coke or graphiteanodes. The accuracy ofthe voltageregulation is better than** ±1% over the operating junction temperature and supply voltage range.

  Charge is terminated by maximum time or minimum taper current detection

  The bq2400x automatically restarts the charge if the battery voltage falls below an internal recharge threshold.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_J	PACKAGE		CHARGE STATUS CONFIGURATION
	20-LEAD HTTSOP PowerPAD™ (PWP)(1)	20-LEAD 5 mm × 5 mm MLP (RGW)(2)	
−40°C to 125°C	bq24007PWP	bq24007RGW	Single LED
	bq24008PWP	Not available	Single bicolor LED

(1) The PWP package is available taped and reeled. Add R suffix to device type (e.g. bq24007PWPR) to order. Quantities 2500 devices per reel.
(2) The RGW package is available taped and reeled. Add R suffix to device type (e.g. bq24007RGWR) to order. Quantities 3000 devices per reel.

PACKAGE DISSIPATION RATINGS

PACKAGE	Θ_{JA}	Θ_{JC}	$T_A \le 25°C$ POWER RATING	DERATING FACTOR ABOVE T_A = 25°C
PWP(1)	30.88°C/W	1.19°C/W	3.238 W	0.0324W/°C
RGW(2)	31.41°C/W	1.25°C/W	3.183 W	0.0318W/°C

(1) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (6,5 × 3,4 mm), internal 1 oz power and ground planes, 8 thermal via underneath the die connecting to ground plane.
(2) This data is based on using the JEDEC high-K board and topside traces, top and bottom thermal pad (3,25 × 3,25 mm), internal 1 oz power and ground planes, 9 thermal via underneath the die connecting to ground plane.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	bq24007 bq24008
Supply voltage (V_{CC} with respect to GND)	13.5 V
Input voltage (IN, ISNS, $\overline{\text{TMR EN}}$, APG/THERM/CR/STAT1/STAT2, VSENSE, TMR SEL, VSEL) (all with respect to GND)	13.5 V
Output current (OUT pins)	2 A
Output sink/source current (STAT1 and STAT2)	10 mA
Operating free-air temperature range, T_A	−40°C to 70°C
Storage temperature range, T_{stg}	−65°C to 150°C
Junction temperature range, T_J	−40°C to 125°C
Lead temperature (Soldering, 10 s)	300°C

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	MAX	UNIT
Supply voltage, V_{CC}	4.5	10	V
Input voltage, VIN	4.5	10	V
Continuous output current		1.2	A
Operating junction temperature range, T_J	−40	125	°C

TEXAS INSTRUMENTS
www.ti.com

ELECTRICAL CHARACTERISTICS CONTINUED

over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

HIGHV (RECHARGE) COMPARATOR, 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		3.80	3.90	4.00	V

OVERV COMPARATOR, 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Start threshold		4.35	4.45	4.55	V
Stop threshold		4.25	4.30	4.35	V
Hysteresis		50			mV

TAPERDET COMPARATOR, 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Trip threshold		12	18.5	25	mV

$\overline{\text{TMR EN}}$ LOGIC INPUT, 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	kΩ

VSEL LOGIC INPUT, 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.25			V
Low-level input voltage				0.8	V
Input pulldown resistance		100		200	kΩ

TMR SEL INPUT 0°C ≤ T_J ≤ 125°C

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage		2.7			V
Low-level input voltage				0.6	V
Input bias current	$V_{I(TMR\ SEL)}$ ≤				

ELECTRICAL CHARACTERISTICS CONTINUED

over recommended operating junction temperature supply and input voltages, and V_I (V_{CC}) ≥ V_I (IN) (unless otherwise noted)

APG/THERM DELAY, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
APG/THERM falling-edge deglitch	See Note 1	25		75	µs

(1) Specified by design, not production tested.

TIMERS, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
User-selectable timer accuracy	T_A = 25°C	−15%		15%	
		−20%		20%	
Precharge and taper timer			22.5		minute

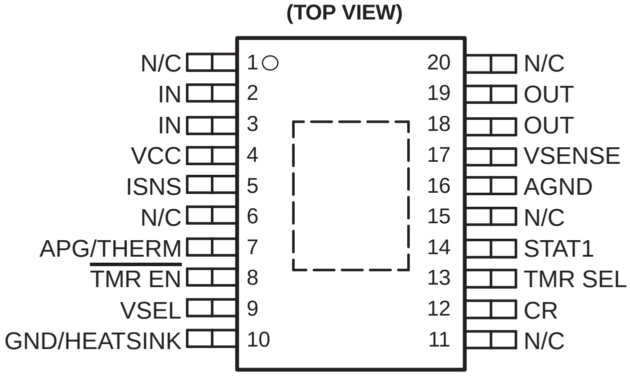
THERMAL SHUTDOWN, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Thermal trip	See Note 1		165		°C
Thermal hysteresis	See Note 1		10		°C

(1) Specified by design, not production tested.

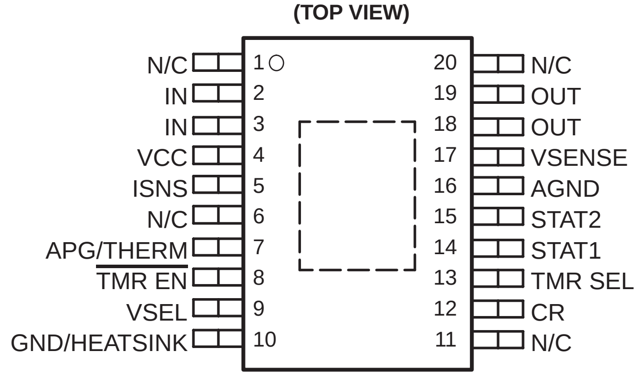
CR PIN, 0°C ≤ T_J ≤ 125°C					
PARAMETER	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Output voltage	0 < $I_{O(CR)}$ < 100 µA, $C_{(CR)}$ = 0.22 µF	2.81	2.85	2.88	V

PIN ASSIGNMENTS

bq24007
PWP PACKAGE
(TOP VIEW)

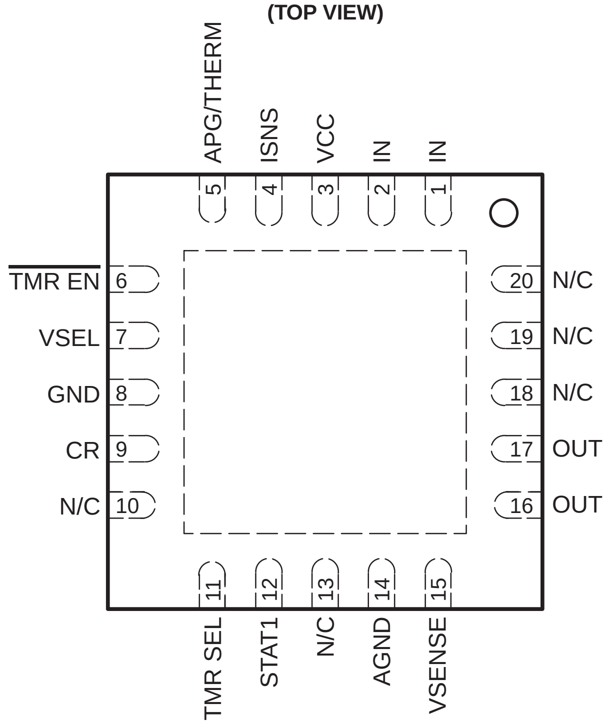


bq24008
PWP PACKAGE
(TOP VIEW)



N/C − Do not connect

bq24007
RGW PACKAGE
(TOP VIEW)

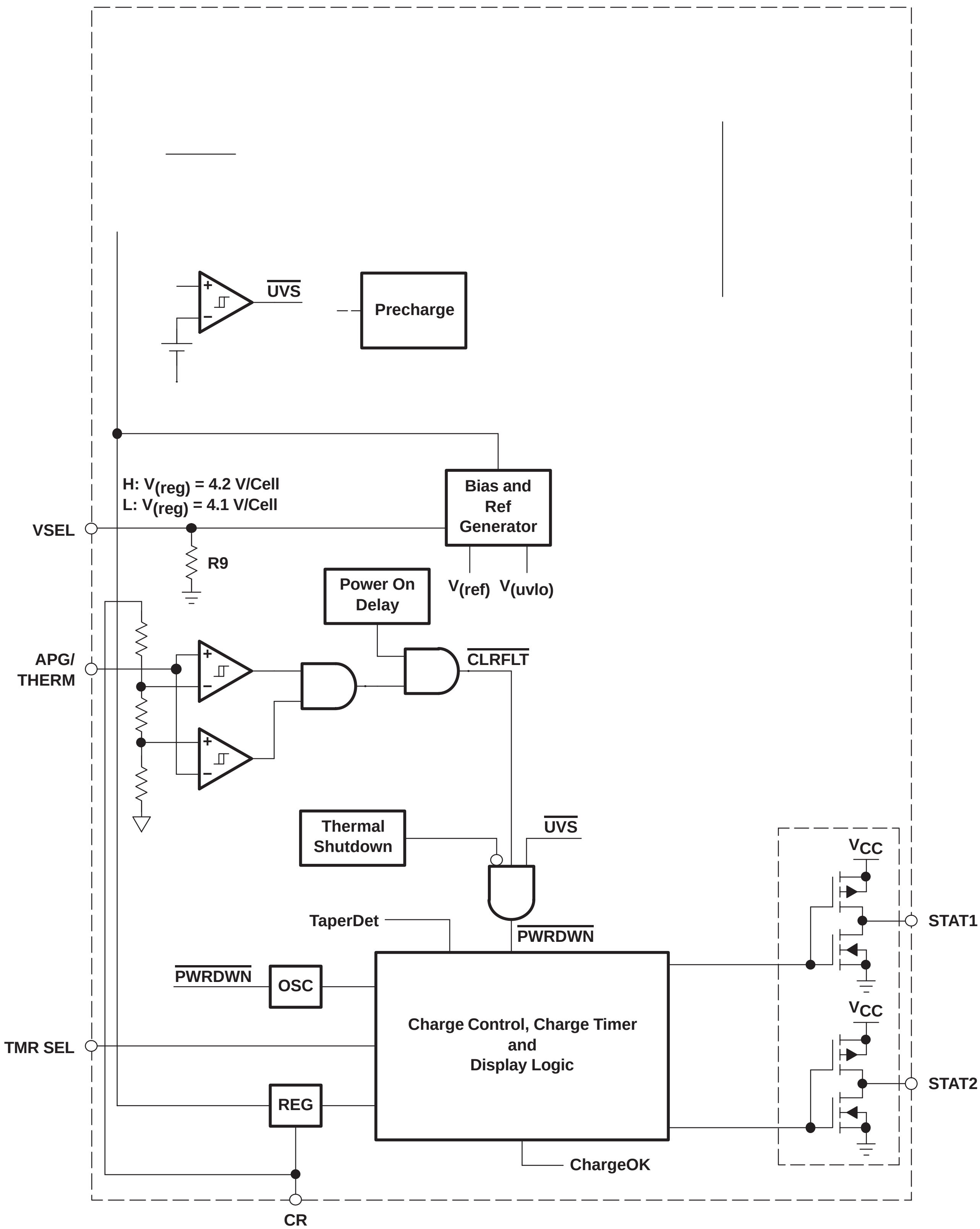


N/C − Do Not Connect

Terminal Functions

TERMINAL			I/O	DESCRIPTION
NAME	NO.			
	PWP	RGW		
AGND	16	14		Ground pin; connect close to the negative battery terminal.
APG/THERM	7	5	I	Adapter power good input/thermistor sense input
CR	12	9	I	Internal regulator bypass capacitor
$\overline{\text{TMR EN}}$	8	6	I	Charge-enable input. Active-high enable input with internal pulldown. Low-current stand-by mode active when EN is low.
GND/HEATSINK	10	8		Ground pin; connect to PowerPAD heat-sink layout pattern.
IN	2, 3	1, 2	I	Input voltage. This input provides the charging voltage for the battery.
ISNS	5	4	I	Current sense input
N/C	1, 6, 11, 15, 20	10, 13, 18−20		No connect. These pins must be left floating. Pin 15 is N/C on bq24007PWP only. Pin 13 is N/C on bq24007RGW only.
OUT	18, 19	16, 17	O	

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

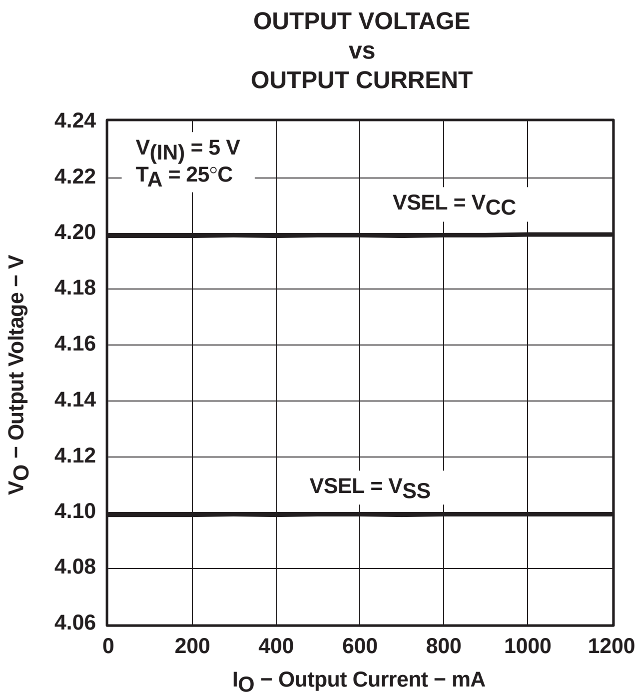


Figure 1

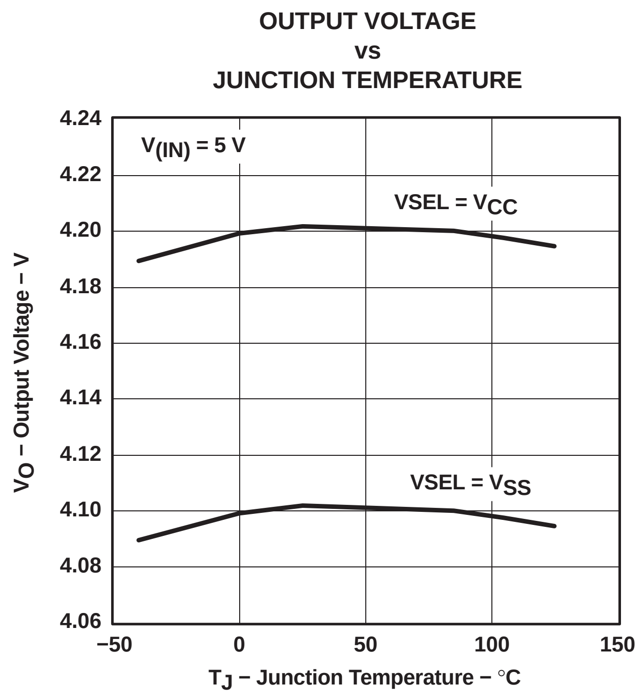


Figure 2

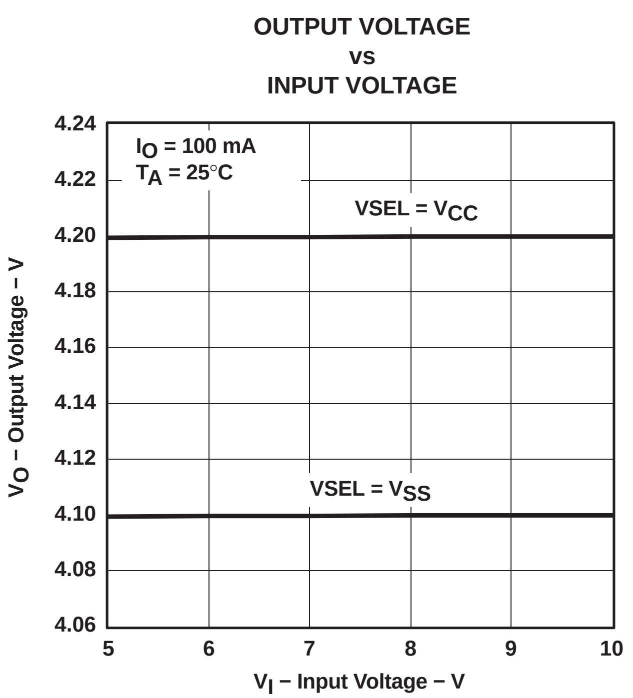


Figure 3

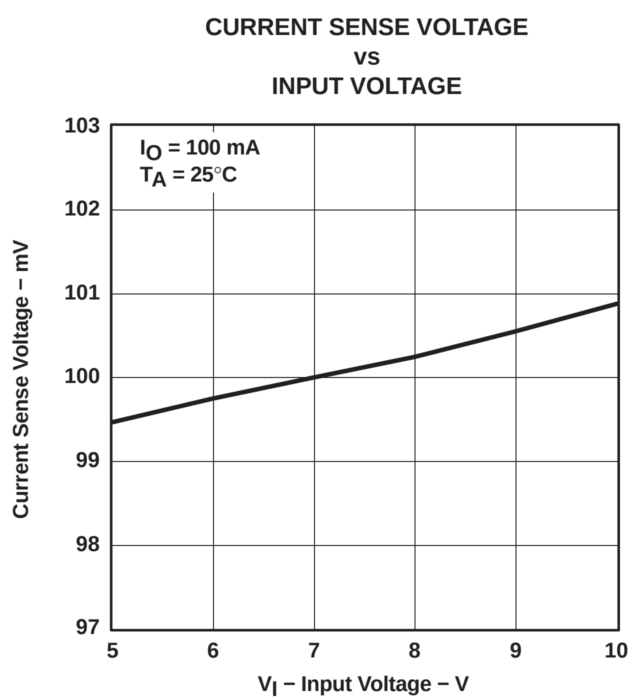


Figure 4

TYPICAL CHARACTERISTICS

CURRENT SENSE VOLTAGE vs JUNCTION TEMPERATURE

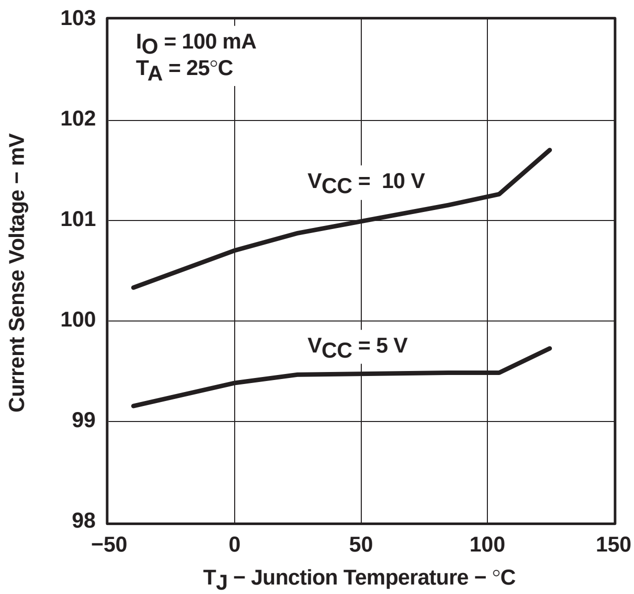


Figure 5

QUIESCENT CURRENT vs INPUT VOLTAGE

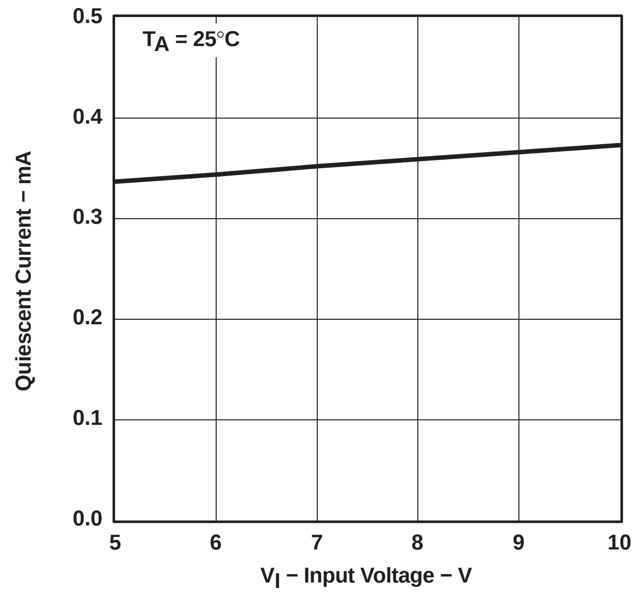


Figure 6

DROPOUT VOLTAGE vs INPUT VOLTAGE

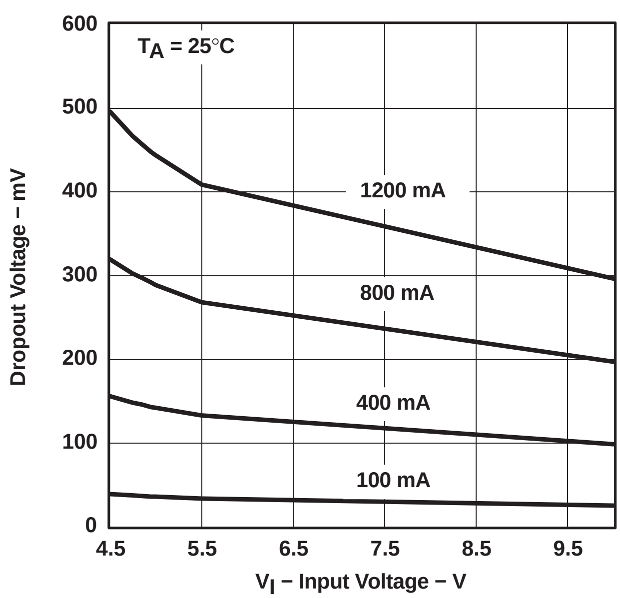


Figure 7

TYPICAL CHARACTERISTICS

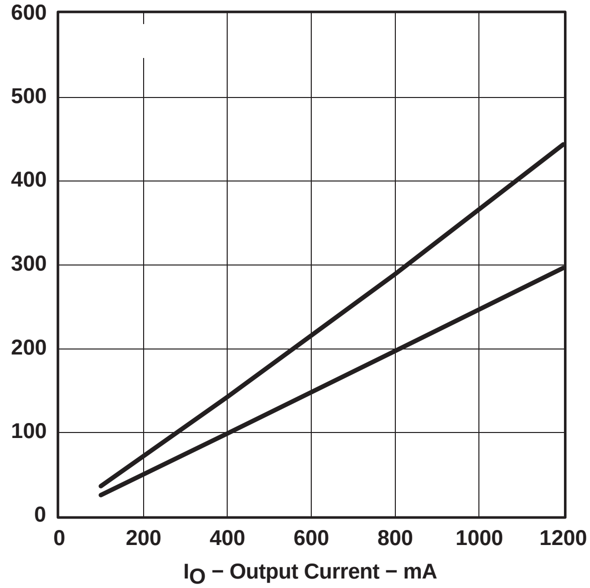


Figure 8

APPLICATION INFORMATION

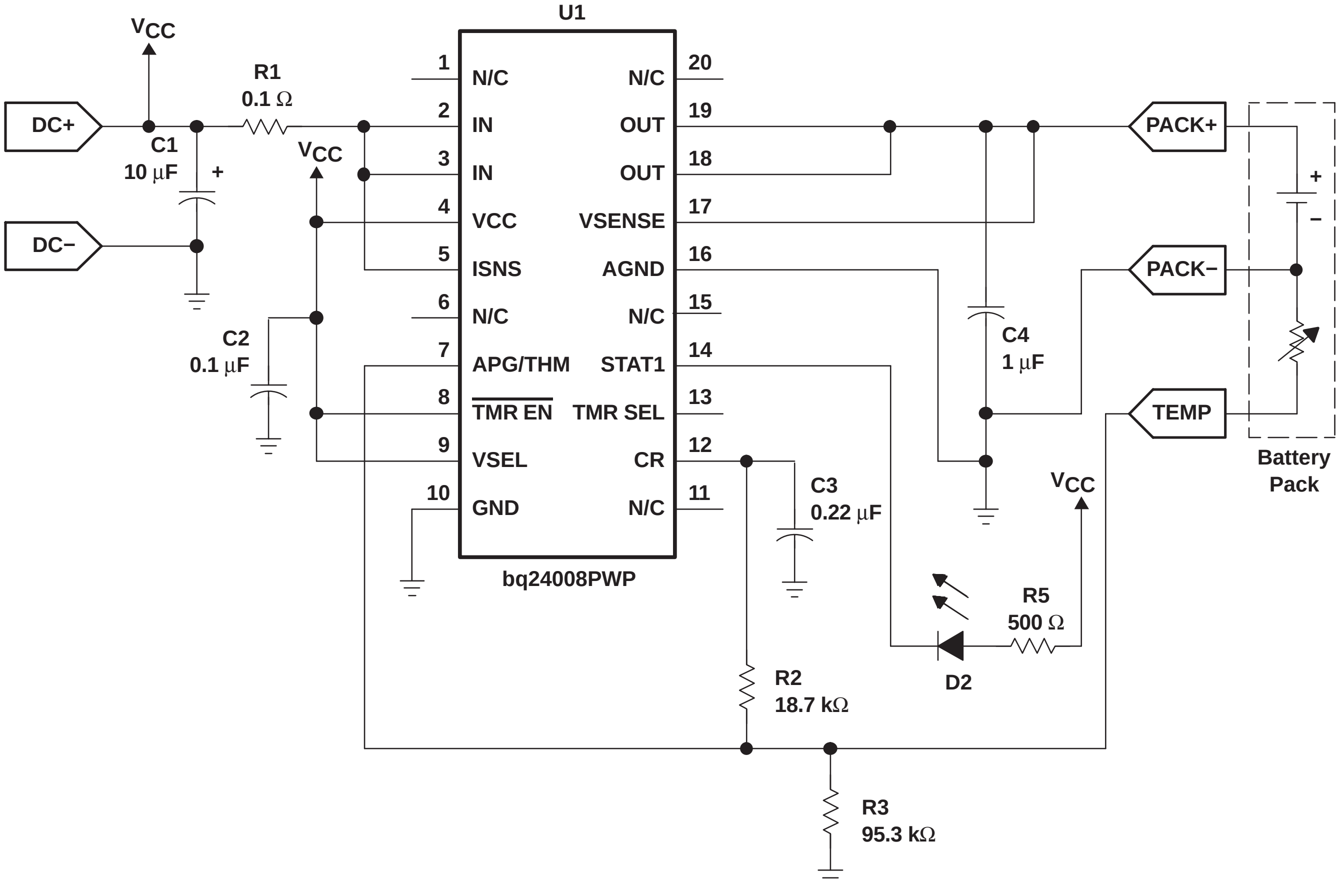


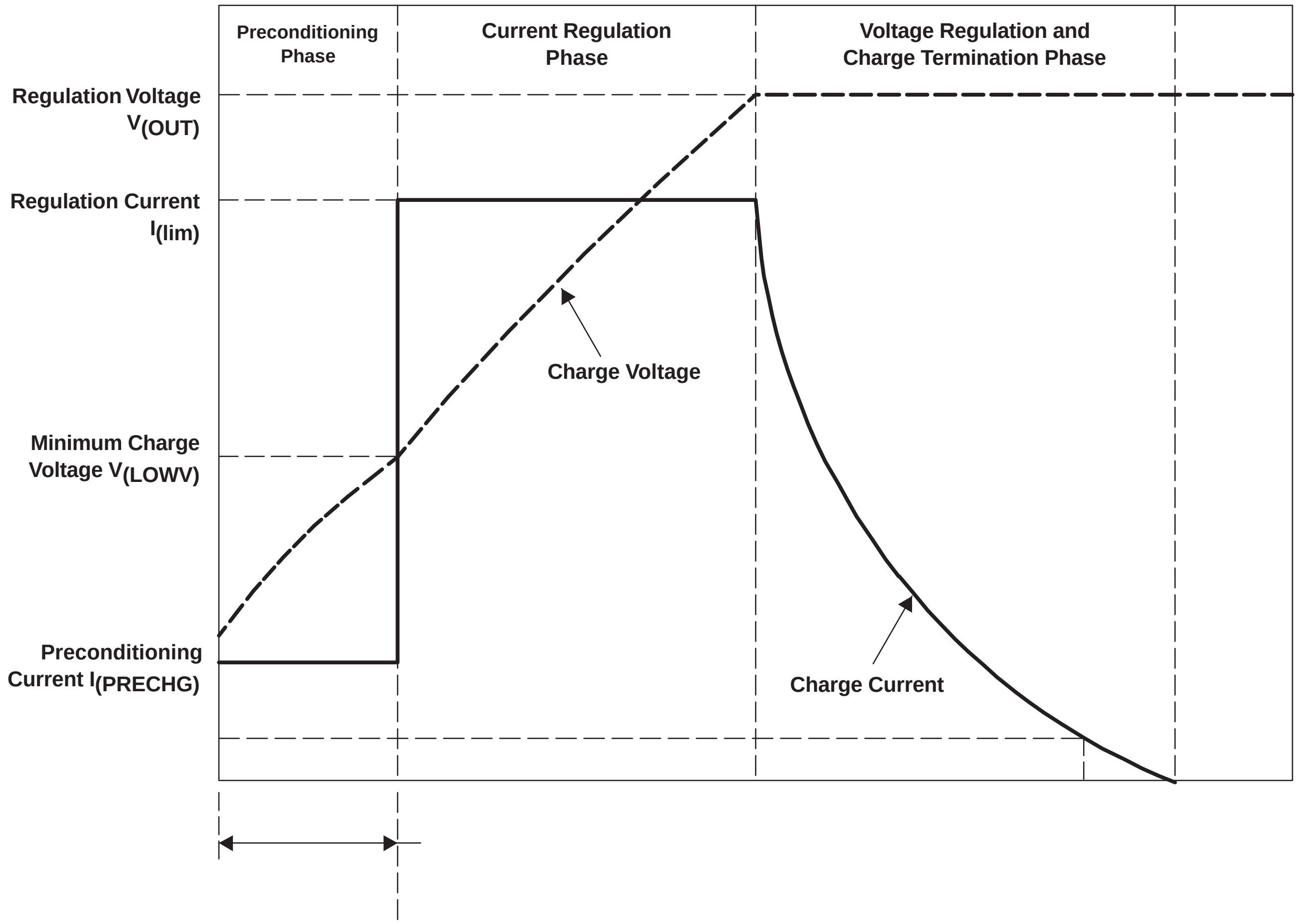
Figure 12. Single-Cell Li-Ion/Li-Pol Charger With Safety Timer Disabled

- If the TMR SEL pin is left floating (3 HR time), a 10-pF capacitor should be installed between TMR SEL and CR.
- If a micro process is monitoring the STAT pins, it may be necessary to add some hysteresis into the feedback to prevent the STAT pins from cycling while crossing the taper detect threshold (usually less than one half second). See SLUU083 EVM or SLUU113 EVM for additional resistors used for the STAT pins.

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The bq2400x supports a precision current- and voltage-regulated Li-Ion charging system suitable for cells with either coke or graphite anodes. See Figure 13 for a typical charge profile and Figures 14 and 15 for an operational flowchart.



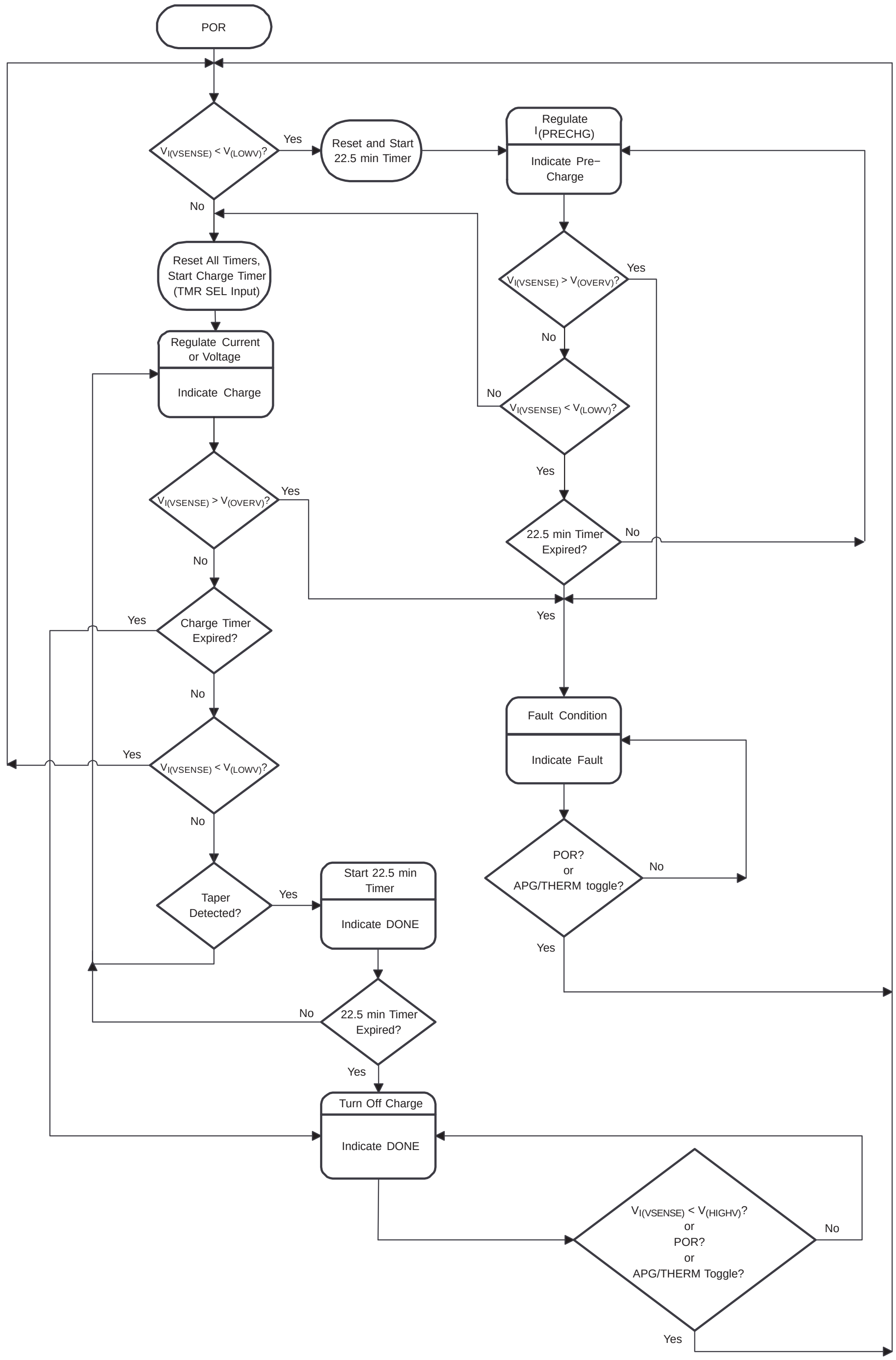


Figure 14. Operational Flow Chart With the Charge Termination Timers Enabled ($\overline{TMR\ EN}$ = 0)

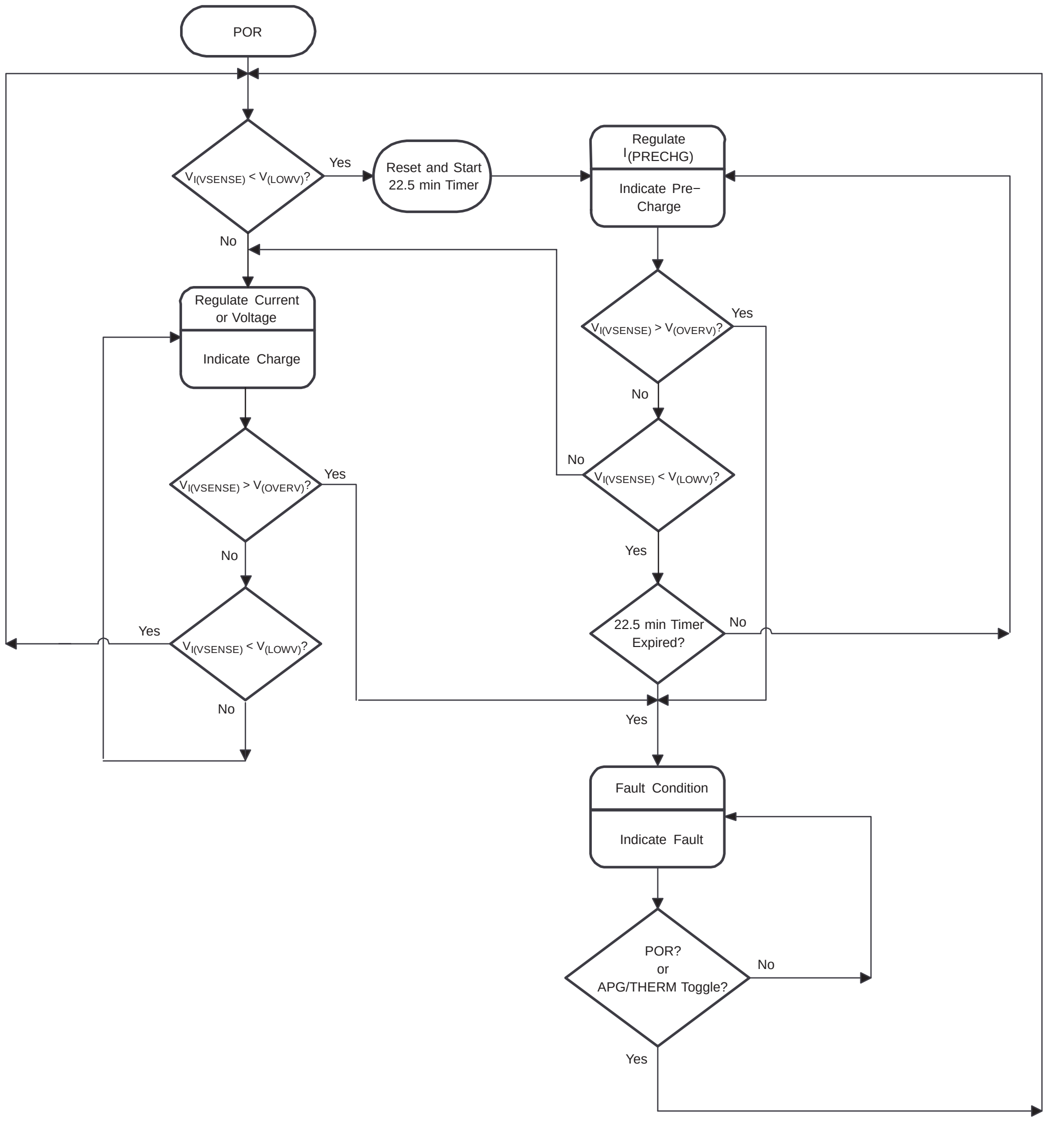


Figure 15. Operational Flow Chart With the Charge Timers Disabled ($\overline{\text{TMR EN}}$ = 1)

Charge Qualification and Preconditioning

The bq2400x starts a charge cycle when power is applied while a battery is present. Charge qualification is based on battery voltage and the APG/THERM input.

As shown in the block diagram, the internal LowV comparator output prevents fast-charging a deeply depleted battery. When set, charging current is provided by a dedicated precharge current source. The precharge timer limits the precharge duration. The precharge current also minimizes heat dissipation in the pass element during the initial stage of charge.

The APG/THERM input can also be configured to monitor either the adapter power or the battery temperature using a thermistor. The bq2400x suspends charge if this input is outside the limits set by the user. Please refer to the APG/THERM input section fo

APG/THERM Input

The bq400x continuously monitors temperature or system input voltage by measuring the voltage between the APG/THERM (adapter power good/thermistor) and GND. For temperature, a negative- or a positive- temperature coefficient thermistor (NTC, PTC) and an external voltage divider typically develop this voltage. (See Figure 16.) The bq2400x compares this voltage against its internal V_{TP1} and V_{TP2} thresholds to determine if charging is allowed. (See Figure 17.)

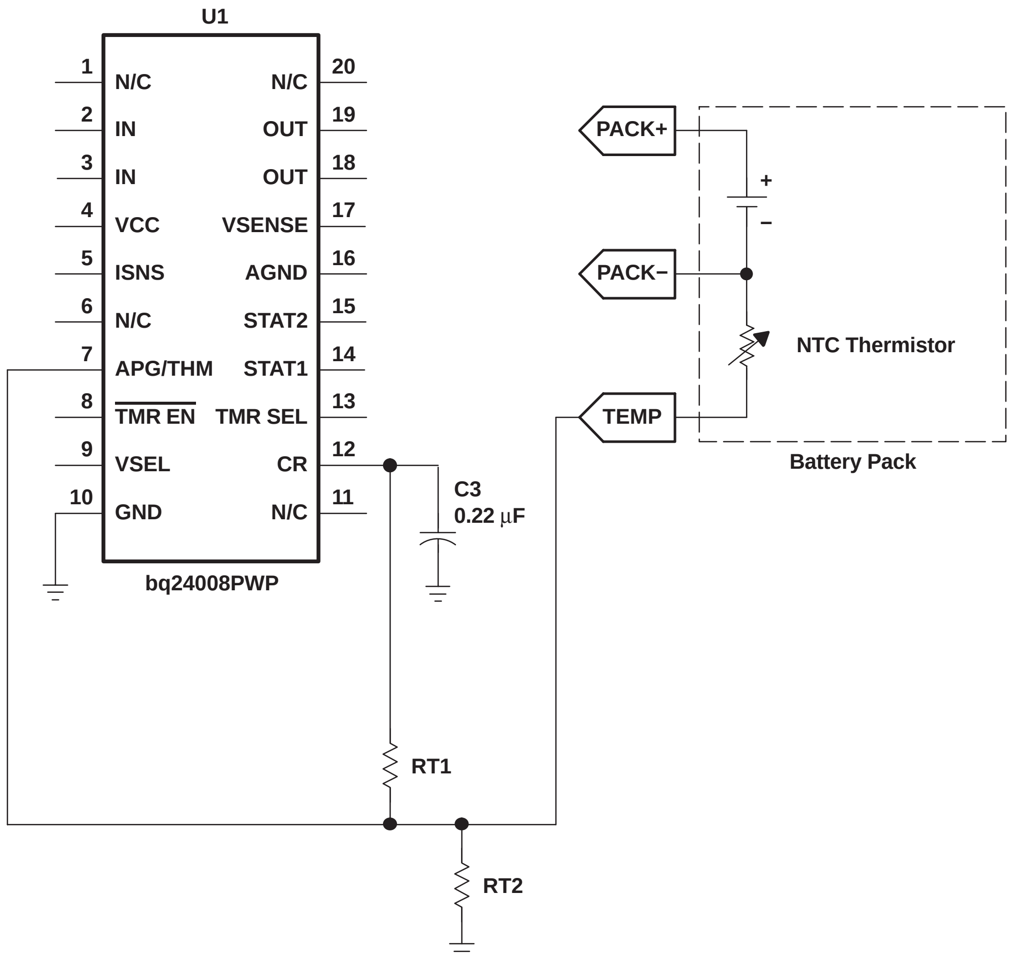


Figure 16. Temperature Sensing Circuit

If the charger designs incorporate a thermistor, the resistor divider RT1 and RT2 is calculated by using the following two equations.

First, calculate RT2.

$$RT2 = \frac{V_B\, R_H\, R_C \left[\frac{1}{V_C} - \frac{1}{V_H}\right]}{R_H \left(\frac{V_B}{V_H} - 1\right) - R_C \left(\frac{V_B}{V_C} - 1\right)}$$

then use the resistor value to find RT1.

$$RT1 = \frac{\frac{V_B}{V_C} - 1}{\frac{1}{RT2} + \frac{1}{R_C}}$$

Where:

$V_B = V_{CR}$ (bias voltage)

R_H = Resistance of the thermistor at the desired hot trip threshold

R_C = Resistance of the thermistor at the desired cold trip threshold

V_H = VP2 or the lower APG trip threshold

V_C = VP2 or the upper APG trip threshold

RT1 = Top resistor in the divider string

RT2 = Bottom resistor in the divider string

Charge current feedback, applied through pin ISNS, maintains regulation around a threshold of Vilim. The following formula calculates the value of the sense resistor:

$$R_{(SNS)} = \frac{V_{(ilim)}}{I_{(REG)}}$$

where I_{REG} is the desired charging current.

Voltage Monitoring and Regulation

Voltage regulation feedback is through pin VSENSE. This input is tied directly to the positive side of the battery pack. The bq2400x supports cells with either coke (4.1 V) or graphite (4.2 V) anode. Pin VSEL selects the charge regulation voltage.

VSEL State (see Note)	CHARGE REGULATION VOLTAGE
Low	4.1 V
High	4.2 V(9.32

DETAILED DESCRIPTION

POWER FET

The integrated transistor is a P-channel MOSFET. The power FET features a reverse-blocking Schottky diode, which prevents current flow from OUT to IN.

An internal thermal-sense circuit shuts off the power FET when the junction temperature rises to approximately 165°C. Hysteresis is built into the thermal sense circuit. After the device has cooled approximately 10°C, the power FET turns back on. The power FET continues to cycle off and on until the fault is removed.

CURRENT SENSE

The bq2400x regulates current by sensing, on the ISNS pin, the voltage drop developed across an external sense resistor. The sense resistor must be placed between the supply voltage (Vcc) and the input of the IC (IN pins).

VOLTAGE SENSE

To achieve maximum voltage regulation accuracy, the bq2400x uses the feedback on the VSENSE pin. Externally, this pin should be connected as close to the battery cell terminals as possible. For additional safety, a 10-kΩ internal pullup resistor is connected between the VSENSE and OUT pins.

TIMER ENABLE

The logic $\overline{\text{TMR EN}}$ enables or disables the charge safety timer. A low-level signal on this pin enables the timers. A high-level input disables the timers and allows the charge to operate continuously. No charge termination is provided when this input is high. Note that the preconditioning timer remains active regardless of the status of this input.

THERMAL INFORMATION

THERMALLY ENHANCED TSSOP-20

The thermally enhanced PWP package is based on the 20-pin TSSOP, but includes a thermal pad (see Figure 20) to provide an effective thermal contact between the IC and the PWB.

Traditionally, surface mount and power have been mutually exclusive terms. A variety of scaled-down TO220-type packages have leads formed as gull wings to make them applicable for surface-mount applications. These packages, however, suffer from several shortcomings: they do not address the very low profile requirements (<2 mm) of many of today's advanced systems, and they do not offer a pin-count high enough to accommodate increasing integration. On the other hand, traditional low-power surface-mount packages require power-dissipation derating that severely limits the usable range of many high-performance analog circuits.

The PWP package (thermally enhanced TSSOP) combines fine-pitch surface-mount technology with thermal performance comparable to much larger power packages.

The PWP package is designed to optimize the heat transfer to the PWB. Because of the very small size and limited mass of a TSSOP package, thermal enhancement is achieved by improving the thermal conduction paths that remove heat from the component. The thermal pad is formed using a lead-frame design (patent pending) and manufacturing technique to provide the user with direct connection to the heat-generating IC. When this pad is soldered or otherwise coupled to an external heat dissipator, high power dissipation in the ultrathin, fine-pitch, surface-mount package can be reliably achieved.

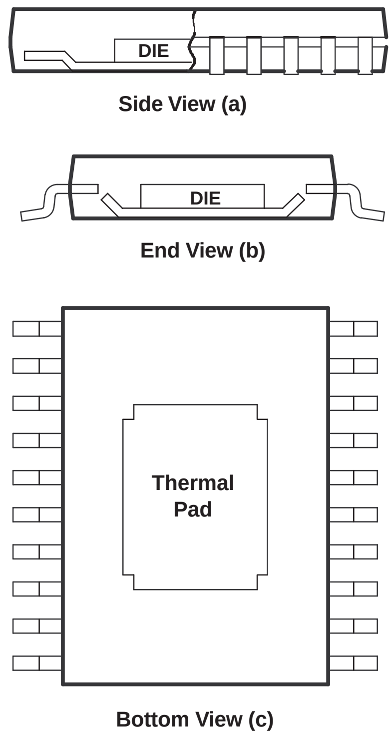


Figure 20. Views of Thermally Enhanced PWP Package

Because the conduction path has been enhanced, power-dissipation capability is determined by the thermal considerations in the PWB design. For example, simply adding a localized copper plane (heat-sink surface), which is coupled to the thermal pad, enables the PWP package to dissipate 2.5 W in free air. (Reference Figure 22(a), 8 cm^2 of copper heat sink and natural convection.) Increasing the heat-sink size increases the power dissipation range for the component. The power dissipation limit can be further improved by adding airflow to a PWB/IC assembly. (See 71 0 TD1(22(a),4.08ermal p TD 0 8 c -0

THERMAL INFORMATION

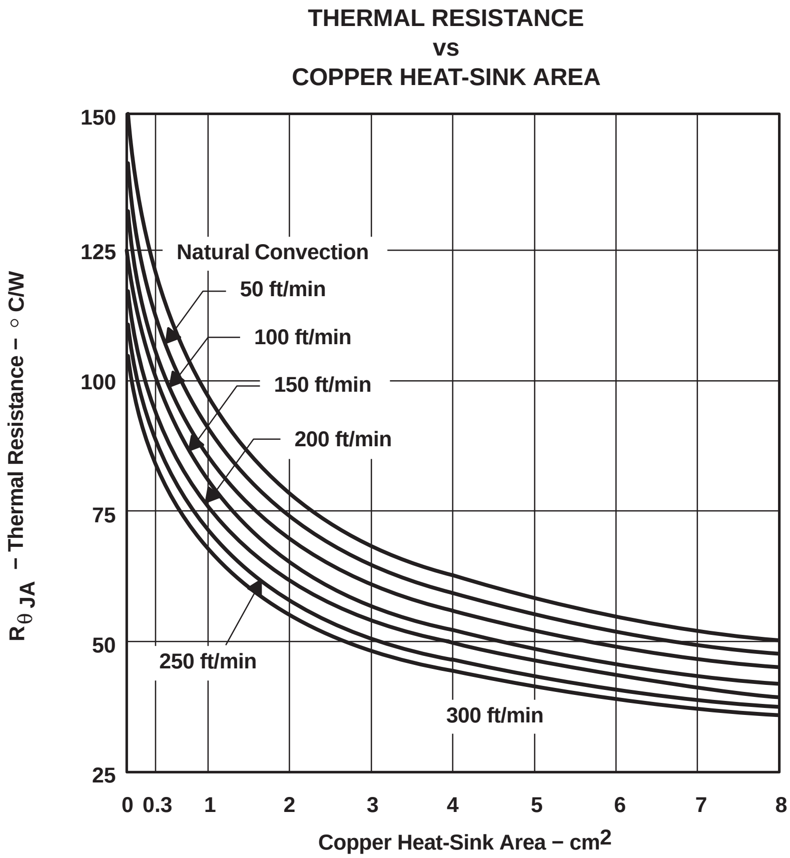


Figure 21

THERMAL INFORMATION

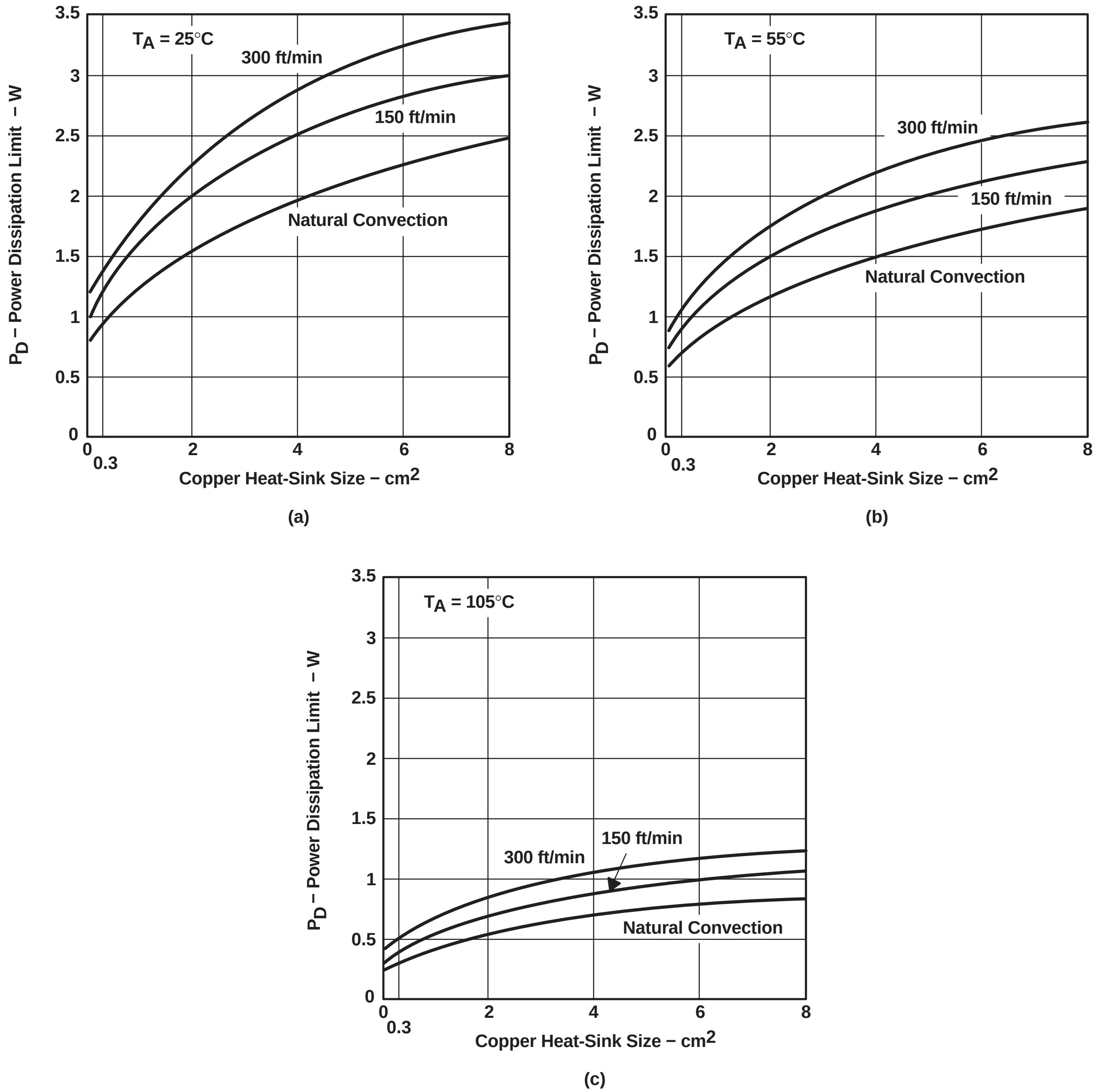


Figure 22. Power Ratings of the PWP Package at Ambient Temperatures of 25°C, 55°C, and 105°C

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24007PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24007PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24007PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24007PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24007RGWR	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24007RGWRG4	ACTIVE	VQFN	RGW	20	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24008PWP	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24008PWPG4	ACTIVE	HTSSOP	PWP	20	70	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24008PWPR	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24008PWPRG4	ACTIVE	HTSSOP	PWP	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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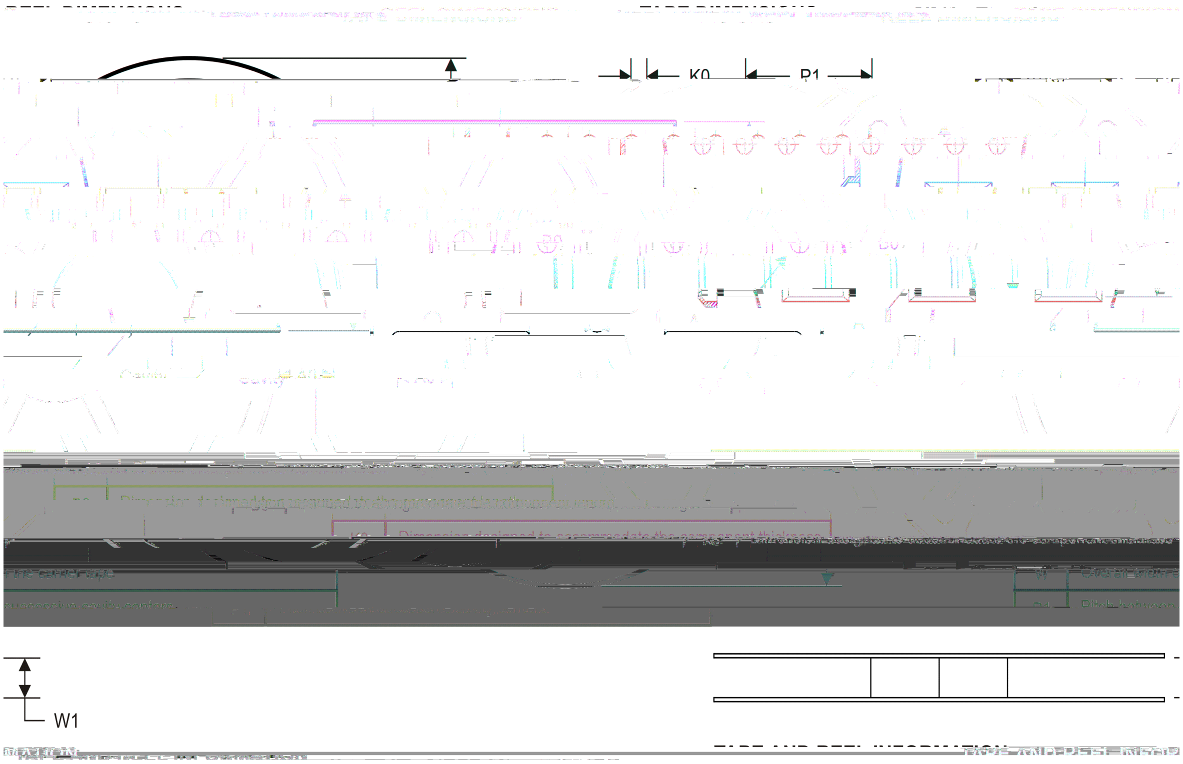
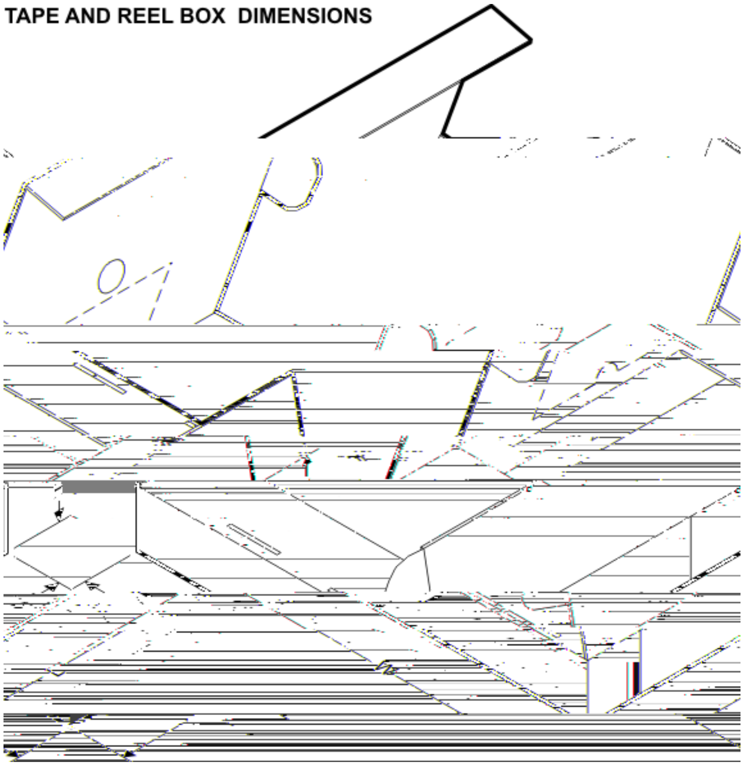
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ24007PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0
BQ24007RGWR	VQFN	RGW	20	3000	367.0	367.0	35.0
BQ24008PWPR	HTSSOP	PWP	20	2000	367.0	367.0	38.0

PowerPAD™ PLASTIC SMALL OUTLINE

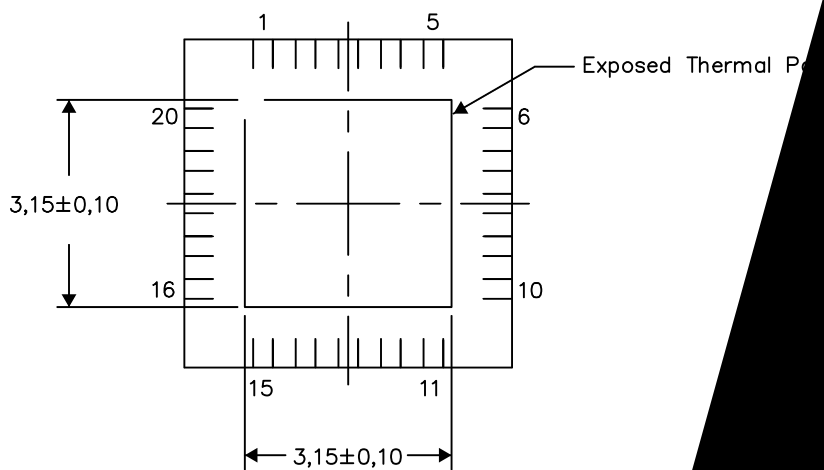
for specific thermal information, via requirements, and recommended board layout. These documents are avail


1.00
0.80
pack, No-leads

This package incorporates an exposed thermal pad that is designed to be attached dir[redacted]
heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB)[redacted]
PCB can be used as a heatsink. In addition, through the use of thermal vias, the the[redacted]

attached to a special heatsink structure designed into the PCB. This design optimize[redacted]

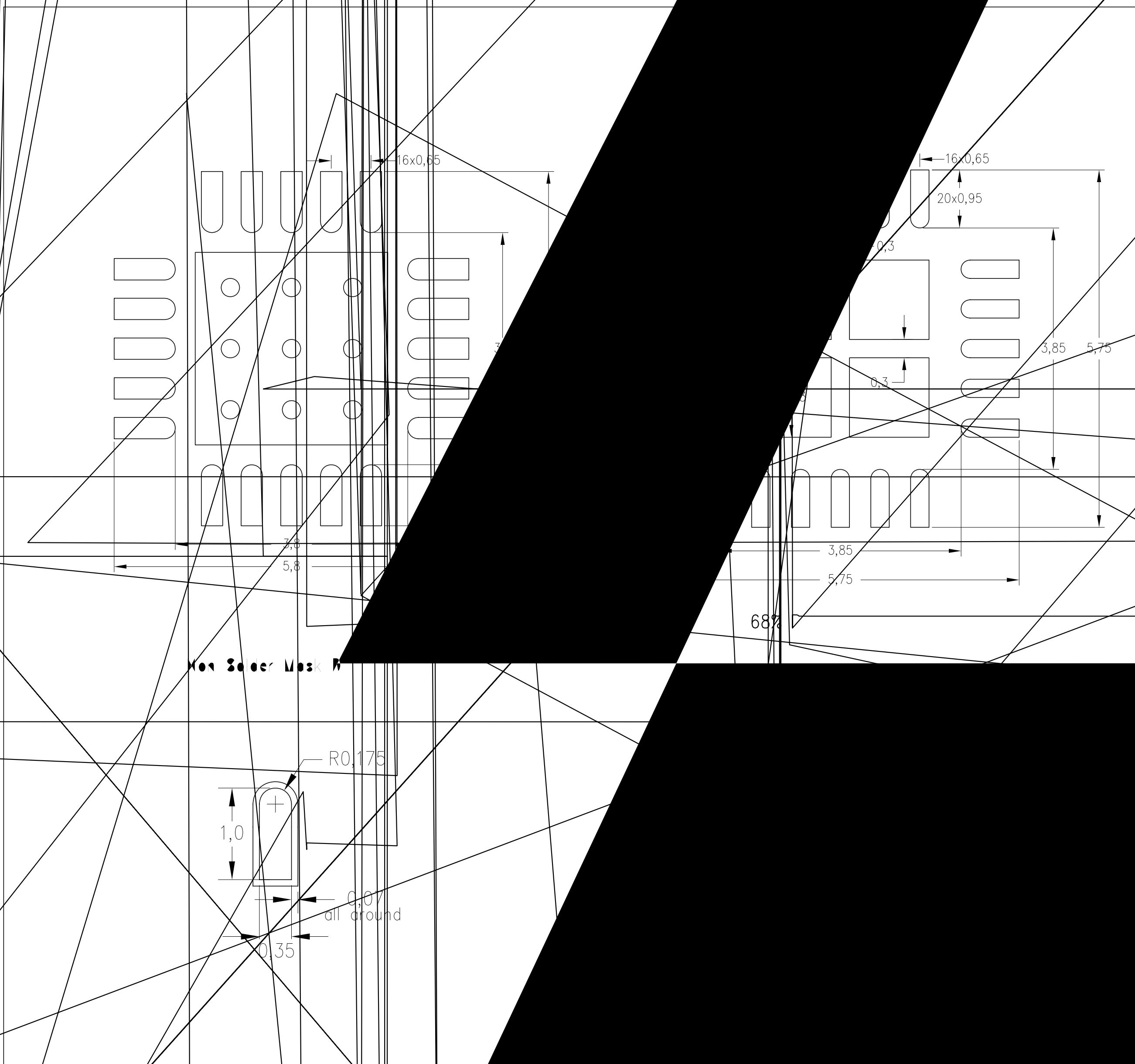
For information on the Quad Flatpack No–Lead (QFN) pack



[redacted]

NOTE: All linear dimensions are in millimeters

hematic for the device, or alte



[redacted]

NOTES:

...commended fo [redacted]

be soldere [redacted] he board. Refer to Application Note, QFN

for specific thermal information, via requ

E. Laser cutting apertures with trapezo

XA
RUME